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Polycrystalline Silicon Thin-Film Transistor Technology for Flexible Large-Area Electronics

by

Yeh-Jiun Tung

B.S. (Massachusetts Institute of Technology, Cambridge, MA) 1995
M.S. (University of California, Berkeley) 1998

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering
and Computer Sciences

in the

GRADUATE DIVISION

of the

UNIVERSITY OF CALIFORNIA, BERKELEY

Committee in charge:

Professor Tsu-Jae King, Chair
Professor Chenming Hu
Professor Costas Grigoropoulos

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Abstract

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Doctor of Philosophy in Engineering –
Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Tsu-Jae King, Chair

The development of a polycrystalline-silicon (poly-Si) thin-film transistor (TFT) technology compatible with plastic substrates will enable information displays and large-area electronics devices that are low power, low cost, lightweight and rugged. Significant challenges exist in the development of a poly-Si TFT fabrication process that is compatible with plastic substrates, since plastic cannot withstand high processing temperatures.

This dissertation addresses two critical issues for the ultra-low temperature ($T \leq 100°C$) fabrication of poly-Si TFTs directly on polymer substrates. The first issue is the formation of the gate dielectric, since thermal oxidation and conventional low-pressure chemical vapor deposition (LPCVD) are not possible at 100°C. At such a low temperature, the quality of the critical gate-dielectric to channel interface is poor. Oxide deposition must be performed using plasma-enhanced CVD (PECVD) or sputter deposition. The work here introduces the use of high-density plasma (HDP) sources,

specifically helicon and electron cyclotron resonance (ECR) PECVD, for TFT gate oxide formation at ultra low temperature. Initial experiments were conducted to determine optimum recipes for SiO_2 deposition through the fabrication and characterization of metal-oxide-semiconductor (MOS) capacitors. Subsequently, high-performance, self-aligned gate poly-Si TFTs were fabricated using a process with a maximum substrate temperature of 100°C. At the time of this work, this process yielded the highest mobility devices reported for any TFT technology compatible with plastic substrates. It is shown that the use of HDP-PECVD tools significantly reduces interfacial oxide defect density compared to conventional parallel-plate PECVD tools.

The second area of emphasis in this dissertation focuses on the poly-Si channel-film formation. Short-pulse excimer laser crystallization (ELC) is necessary to form poly-Si when a polymer substrate is used. (Plastics are incompatible with long, high-temperature crystallization processes.) Unfortunately, the range of laser fluences that yield large-grained poly-Si is very narrow, and often it is necessary to trade off good performance for device-to-device uniformity when ELC is used. This work introduces the use of a patterned anti-reflective (AR) oxide capping layer to control grain location in the channel film during ELC. Results from this new process show an improvement in TFT performance and uniformity. The process is self-aligned and simple, so it can be easily incorporated into existing ELC-based poly-Si TFT process flows.

Two additional areas of work are presented in the latter part of the dissertation. A prototype for an active-matrix organic light-emitting diode (AMOLED) display is presented. A layout and fabrication process was designed for a monochrome 128x64 pixel, 80 dpi display on a 4"x4" square glass substrate. Each pixel contains two

transistors to drive an OLED. AMOLED displays are of great interest because they promise lower power, higher brightness, and wider viewing angle than the pervasive active-matrix liquid crystal display (AMLCD). In addition, the inherently low deposition temperature of organic materials allows for easy processing on flexible plastic substrates.

Lastly, a method is demonstrated for resist-free, direct patterning of thin films using an excimer laser. This technique addresses current problems plaguing the flat panel display manufacturing industry. High costs are associated with large area lithography that uses conventional photoresist coating, exposure and development. We present preliminary results for a direct patterning method that dramatically simplifies the lithography process. Specifically, the Si active layer is patterned by selectively exposing a laser beam onto a sacrificial layer of Si_xGe_{1-x} that sits atop the Si film. The sacrificial film mixes with the underlying Si film and is then removed by a highly selective wet etch.

The dissertation abstract of Yeh-Jiun Tung is approved:

Professor Tsu-Jae King Date

Committee Chair

To my Mom and Dad and brother, for their love and encouragement

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Acknowledgments

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Most importantly, I would like to thank my family. I owe all my achievements to their unconditional love and support.

Chapter 1

Introduction

1.1 Flat-Panel Display Technologies

1.1.1. The Flat-Panel Display Market

Flat panel display (FPD) technologies have long sought to supplant the firmly entrenched cathode ray tube (CRT) as the dominant electronic information display medium. Since 1950, there has been a sustained effort to find a replacement for the CRT. However, the CRT has many virtues for information displays: extremely fast response; high resolution; vivid color and excellent image quality; and both small-size (1-in. diagonal) and large-size (36-in. diagonal) formats for varied applications. As recently as the beginning of the 1980's, the CRT was still the only commercially available device that could display full color TV video. CRT technology has been continuously improving since its inception, but the most significant trend for CRTs is decreasing cost.[1] Because

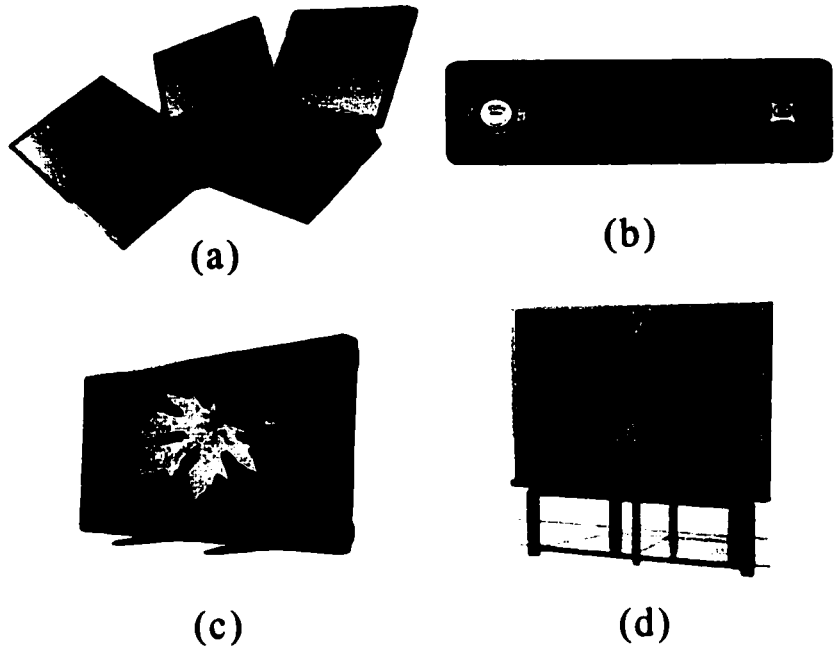

Figure 1.1. Examples of various FPD technologies: (a) LCD screens in laptop computers (*from http://www.dell.com*). (b) Pioneer DEH-P9200R car stereo display featuring an organic electro-luminescent (EL) display (*from http://www.pioneerelectronics.com*). (c) Sony 40-in. plasma display panel (PDP) television (*from http://www.sony.com*). (d) Rear projection Hitachi 55DMX 2000 digital micromirror device (DMD) TV (*from http://www.hitachi.com*).

CRTs are continually getting cheaper and better, the cost challenge is the most difficult for flat-panel technologies. But the CRT does have one drawback that it cannot overcome: it is too bulky. The large volume stems from the depth of the tube, which is required to focus and scan the image and is thus comparable to its diagonal dimension. This depth remains the CRT's Achilles' heel.

In contrast, FPDs are compact, lightweight and consume less power. These features alone have enabled many products and applications, despite the higher costs of FPDs. A wide variety of FPD technologies can be found in commercial electronics nowadays (Figure 1.1). The leading FPD technology is liquid crystal displays (LCDs), which are found in laptop computers, watches, personal digital assistants (PDAs),

handheld computers, mobile phones, pagers, among other applications. An emerging FPD technology is based on organic light-emitting diodes (OLEDs). OLEDs are meant to compete directly with LCDs and are just beginning to be available to consumers. These bright, high-contrast and low-power displays can be found in Pioneer car stereo displays and Motorola and Sanyo cellular phones. Plasma display panels (PDPs) are another commercially available FPD technology. Major electronics companies (e.g. Philips, Panasonic, Fujitsu, Pioneer and Sony) manufacture large-area (50-inch diagonal), high-definition PDP television sets with 4" depths.[2] Though presently expensive, PDP TV sets are expected to be cost competitive with CRT TVs by 2003. In the projection display arena, Texas Instruments has developed an electro-mechanical display technology called the digital micromirror device (DMD). Hitachi, Mitsubishi and Panasonic use these tiny mirror arrays in rear projection displays for desktop monitors and televisions.[3]

These examples demonstrate that a vast array of CRT-alternative display technologies exists. With new technologies constantly being introduced, more mature technologies are forced to improve performance and lower cost. As a result, FPD sales have been rising steadily, particularly in the last decade. It is predicted that FPDs will capture 50% of the worldwide display market by 2003,[4] thus ending nearly a century of the CRT's dominance. Within the FPD market itself, LCDs represent the largest segment by far, comprising the majority of total FPD sales. Figure 1.2 shows the world market for FPDs by technology. LCD dominance is still expected to continue in the coming decade. LCDs enjoy this lofty market position because they are the most mature of the FPD technologies, making them both the highest performance display technology and the lowest cost as well.

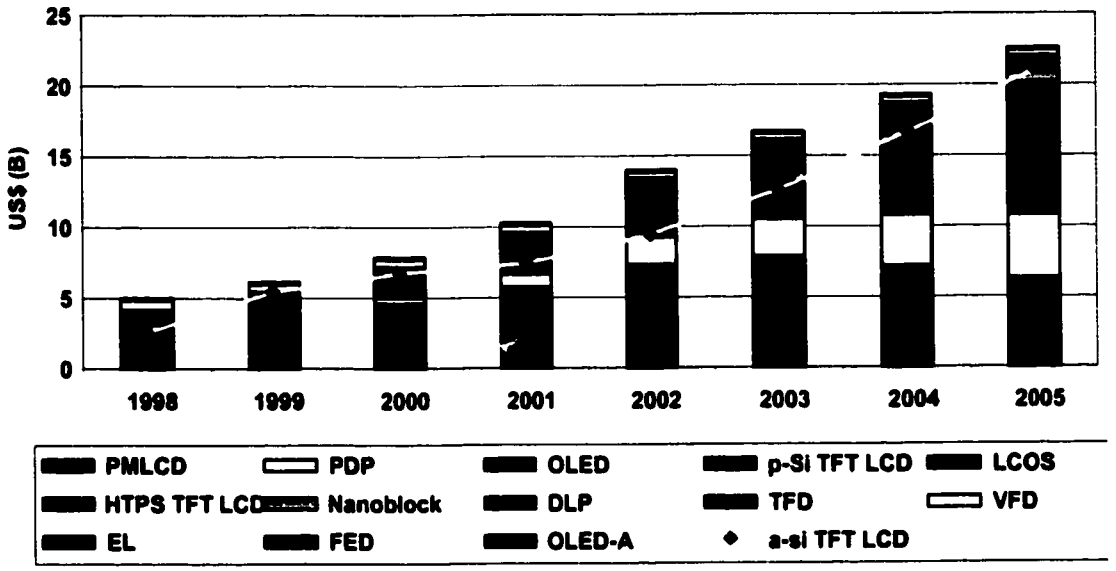

Figure 1.2 World market for FPDs by technology. Improvements in competing display technologies will continue to drive the progress of AMLCDs. (*source: DisplaySearch*)

1.1.2 Passive- vs. Active-Matrix LCDs

LCDs can be categorized into two broad categories: passive-matrix and active-matrix. As background to discussion of these display types, the fundamentals of LC operation are first presented. Then, the basic operation of passive and active displays is described, with an emphasis on the increasing importance of high-performance active-matrix technologies.

Liquid crystal is a state of matter that exists between liquid and solid. LC materials can flow as liquids, but there is some long-range order due to an elongated molecular structure, which leads to the parallel alignment of molecules. This long-range order creates a unique electro-optic characteristic that can be exploited for displays.

Figure 1.3 shows a schematic of a standard twisted nematic (TN) LC cell. The liquid crystal is sandwiched between two glass plates that are each coated with a

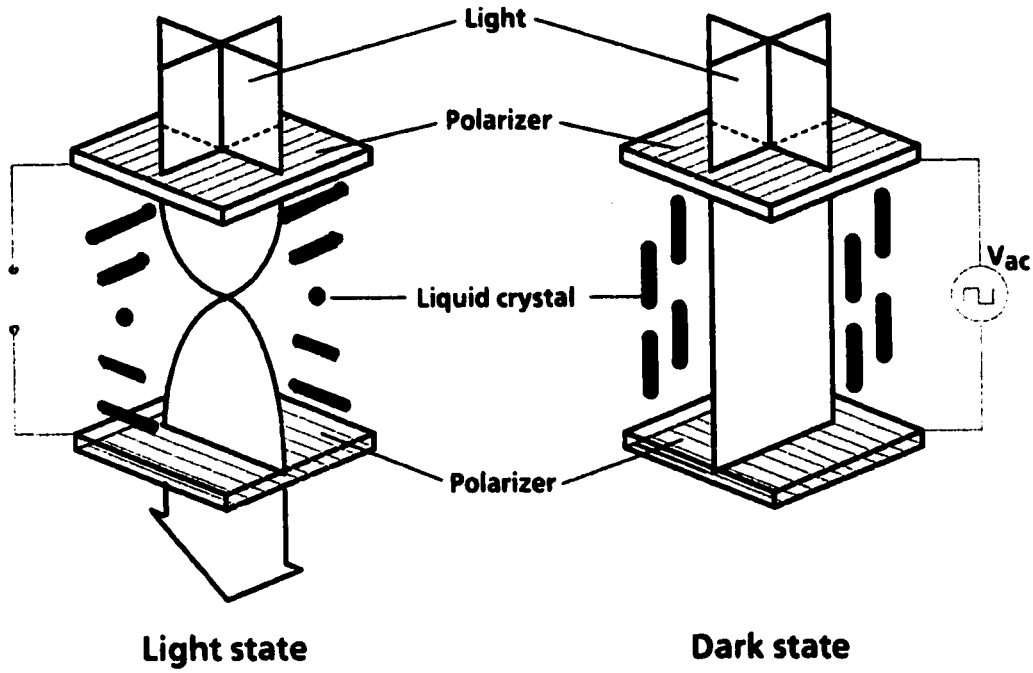

Figure 1.3. Operation of a standard twisted-nematic (TN) liquid-crystal cell. The nematic LC molecules align with the brushed surface of the top and bottom electrodes so that the orientation of the LC molecules undergoes a twist from one electrode to the other. The polarization axis of the light entering the cell is effectively rotated by the twisted LC layer so that it can pass through the second polarizer (light state). Under applied voltage, the LC molecules tend to align with the electric field so that the polarized light cannot pass through the second polarizer (dark state).

transparent conducting material (Indium Tin Oxide or ITO) and an orienting layer. The orienting layer is formed by brushing an organic film in one direction, thus creating grooves. In the figure, these layers on the two plates are oriented perpendicular to each other. The liquid crystal aligns its molecules with the direction of the grooves at the surface of each plate, so that the molecules must then twist 90° from top to bottom.

Liquid crystal is optically anisotropic. It has a different index of refraction for light polarized parallel to its molecular rods (n_e) compared to light polarized perpendicular to its rods (n_o). If the twist is sufficiently gradual, then the polarization of light will twist in the same direction at the LC material. As shown in the figure, light

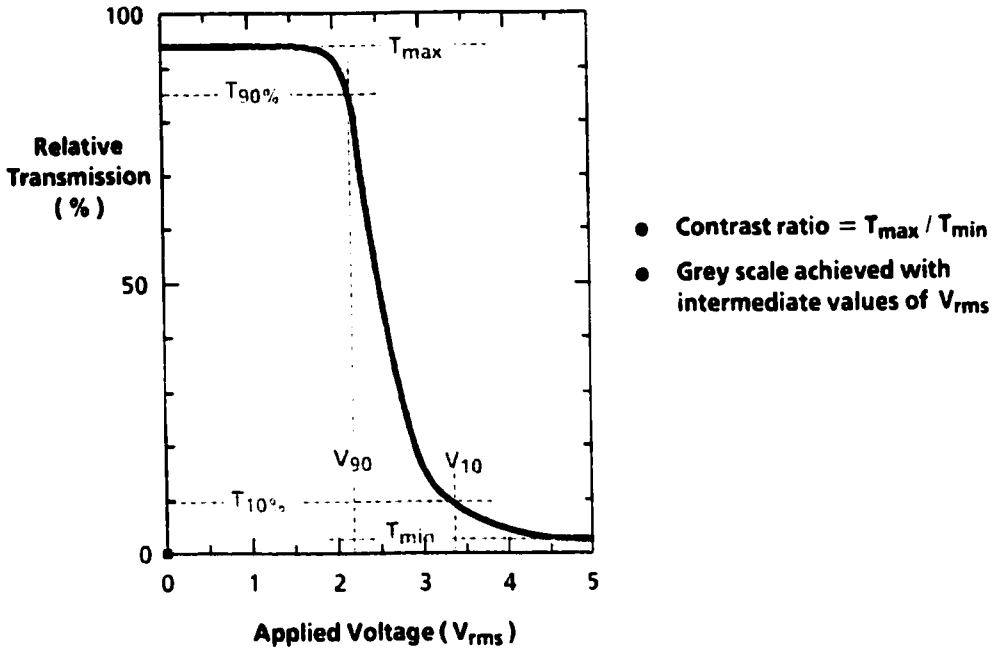

Figure 1.4. Electro-optic response of a TN LC cell. Light transmission varies with applied voltage. Grayscale is achieved by applying voltages between V_{90} and V_{10}, where light transmission varies between 90% and 10% respectively.

enters the cell polarized in the x-direction, slowly rotates polarization as it passes through the cell, and exits polarized in the y-direction. In this case, light is transmitted, so it is the "light state." LC also exhibits dielectric anisotropy, so that the rods tend to align to an applied electric field. When a voltage is applied between the plates, the 90° twist is disturbed and light can longer be transmitted through the cell. This is the "dark state." Essentially, the LC cell acts as a light valve.

The light transmission of an LC cell varies with applied voltage. This curve, shown in Figure 1.4, exhibits varying light transmission as a function of applied AC rms (root mean square) voltage. (An AC signal is required to drive the LC materials to prevent deterioration of the cell.) This LC cell is called "normally white," because light

passes in the normal state, i.e. zero applied voltage. (A "normally black" cell would have the inverse curve.) As the applied voltage is increased, the LC molecules at the center plane begin to align to the electric field and transmission is gradually reduced until near-zero transmission at V_{rms}=5V. Grayscale can be achieved using intermediate V_{rms} values between 90% transmission ($T_{90\%}$) and 10% transmission ($T_{10\%}$). However, high-level grayscale requires precise control of the voltage level in this transition region. For instance, 8-bit grayscale (16.7 million colors) requires 256 distinct voltage levels within a range of roughly 1.2V in this example. Maintaining these fine voltage levels over the refresh time of the cell is critical to achieving good grayscale performance. The contrast ratio of the cell is defined as the ratio between the maximum and minimum transmission (T_{max}/T_{min}).

Passive-matrix displays are constructed using two sets of perpendicular electrodes: horizontal row and vertical column electrodes. Figure 1.5 shows a schematic of the passive-matrix structure. The intersection of these electrodes defines the pixels. Operation consists of sequentially raising the potential of each row electrode to +V, while the data is loaded through the column lines by either applying -V (leading to white cells in a normally black display) or grounding (leading to dark cells). The full voltage only appears across the selected pixels. By repeating this process for all row and column electrodes at a frame rate of ~50Hz or higher, an image is formed. Passive-matrix displays thus have a simple, inexpensive construction and a simple multiplexed addressing scheme.

Passive-matrix addressing suffers from one major drawback: applied voltages also affect non-selected pixels in the selected row and column. This crosstalk is due to "sneak

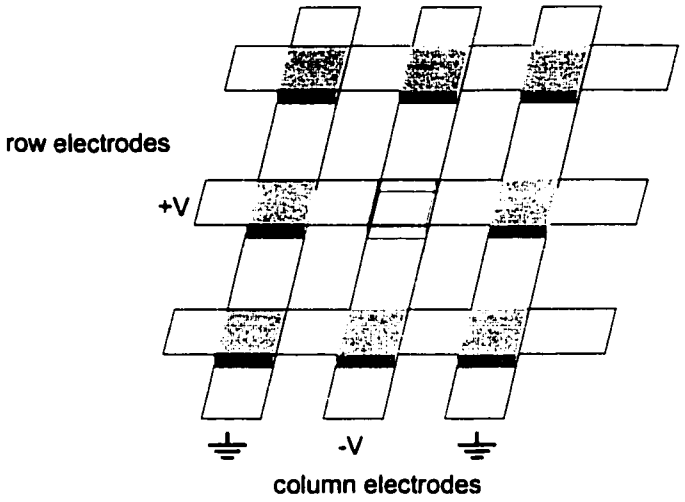

Figure 1.5. Passive-matrix structure schematic. Row and column electrodes consist of perpendicular conducting lines on opposing glass plates, and the intersection of the electrodes define the pixels. In this figure, the LC cells are "normally black." The center pixel is addressed by biasing the row electrode to +V and the corresponding column electrode to –V. The applied voltage allows the cell to pass light.

paths" throughout the matrix and leads to a significant voltage drop across the cells in the selected row and column. The image quality suffers because there is a reduction in the contrast between selected and non-selected pixels. A steep LC electro-optic characteristic is required to ensure that partially selected pixels do not turn on (or off). The problem is exacerbated as the display size and number of pixels increase. The various display metrics (viewing angle, grayscale compatibility, contrast and speed of response) are often comprised for large passive-matrix displays to ensure a narrow transition region in the electro-optic characteristic. High-resolution, high-contrast passive-matrix displays are not be possible due to the Alt-Pleshko limit.[5]

Active-matrix technology provides a solution to this limit for passive-matrix displays. Figure 1.6 shows a schematic of an active-matrix structure and describes the addressing scheme. The active-matrix circuit is similar to a large feature-size VLSI

DRAM with 1-T cells. A thin-film transistor (TFT) is used in each pixel, acting as a switch to store the voltage on the pixel electrode. Addressing is accomplished by driving one row (scan line) at a time, biasing the transistor gates high and loading data into the pixels from the column lines. After one row of data is loaded, the transistors are turned off and the next row is selected. The pixel electrodes are isolated from each other by the TFTs, and a constant voltage is maintained over the refresh cycle time (if the TFT and LC leakage currents are sufficiently low). As a result, the contrast is considerably better than in passive-matrix displays. In addition, the LC electro-optic curve no longer needs to be as abrupt, so other aspects such as viewing angle and response time can be optimized.

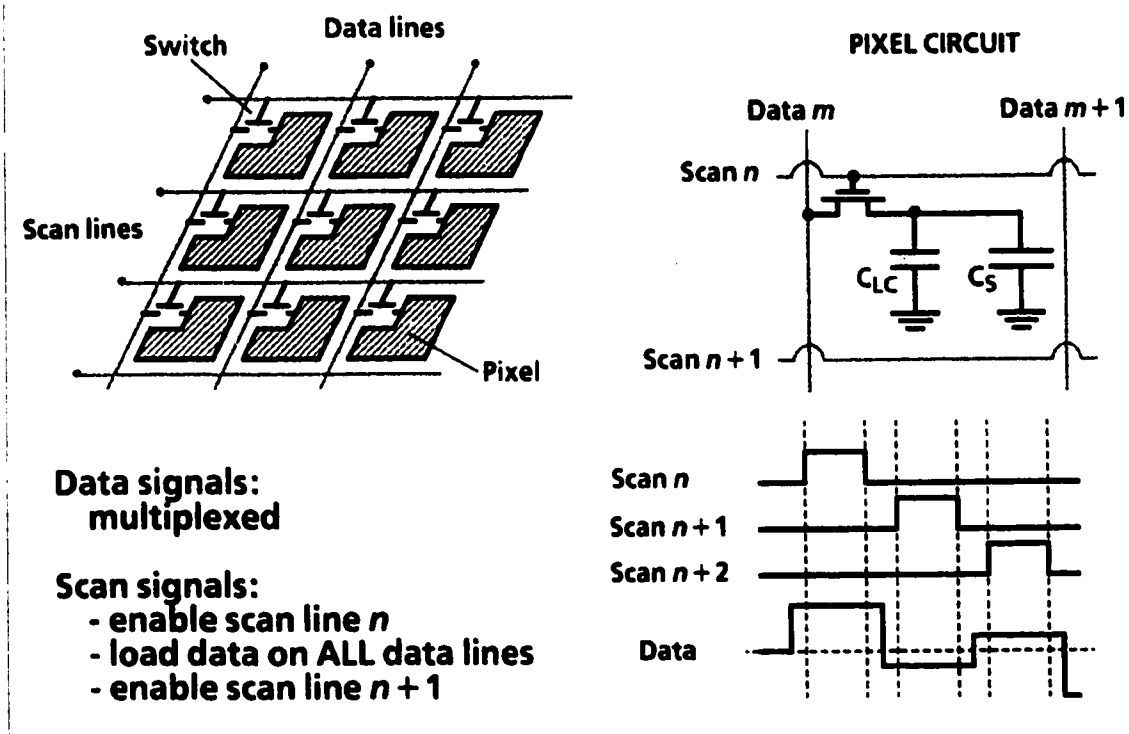

Figure 1.6. A schematic of active-matrix LCD structure and operation. A TFT is used at each pixel as a switch to control the voltage of the LC cell. Image data is loaded as follows: the TFT gates are turned on by applying a voltage to single row, then data is transferred to the pixels from the column (data) lines. Then, the row is turned off and the next row is selected. This process is repeated for each row line until the entire display image is loaded. A storage capacitor (C_S) is placed in parallel with the LC cell to maintain the voltage across the LC cell for a frame time (~16msec for a 60Hz refresh rate).

Pixel TFTs in active-matrix displays have relatively modest performance requirements. The devices must be able to fully charge the pixel capacitance ($C_{LC} + C_S$) during one line time (the duration that the scan line is pulsed high). Typically, the drive current required is ~1μA. Such drive currents should be achievable at a gate-to-source voltage (V_{GS}) < 30V in order to avoid the use of expensive, high-voltage IC driver chips. The leakage currents should be low enough so grayscale levels can be maintained over the frame refresh time. Typically, the voltage across the pixel should not change by more than 20mV over the frame time, and the corresponding requirement is for leakage currents to be less than 1pA.

Unfortunately, fabrication of active-matrix displays is a difficult task because the TFTs are distributed over such a large area. The costliest and most complex component in the AMLCD manufacturing process is the active-matrix backplane. An XGA monitor (1024x768 pixels) has approximately 785,000 transistors for a monochrome display. For color displays, 2.35 million transistors are required! The active-matrix must be fabricated on a large glass panel (roughly one meter on a side) with near perfect yield. But the most challenging constraint is that the process must entirely compatible with the substrate material. In most cases, displays are fabricated on glass sheets that have a strain point far below the melting point of silicon. For example, the commonly used Corning 1737 has a strain point of 666°C, so all process steps must be performed below this temperature.

Thin-film transistor performance and process technology is closely correlated to the maximum fabrication temperature, which has implications for the electrical properties of the active layer. For example, amorphous silicon (a-Si:H) TFTs can be fabricated at temperatures below 350°C, while poly-Si TFTs generally require much higher

temperatures due to the need to crystallize Si. The resulting electrical performance of these two TFT technologies can differ dramatically. In the next section, an overview of TFT technologies is presented.

1.2 Thin-Film Transistor Technologies

Figure 1.7 shows a typical structure for a top-gated TFT. TFTs are similar to silicon-on-insulator (SOI) transistors; the active layer is a thin film isolated from the substrate by a buffer dielectric. However, unlike SOI CMOS devices, TFTs are usually fabricated on glass substrates using either amorphous or polycrystalline Si films, which have an abundance of defects with associated carrier trap states within the Si bandgap. The presence of these traps results in significantly poorer transistor performance when compared to crystalline Si (c-Si) MOSFETs.

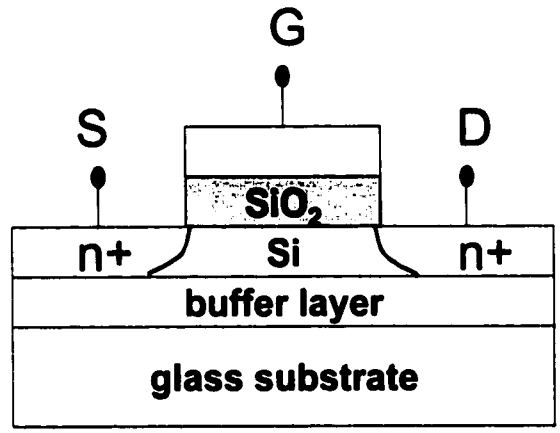

Figure 1.7. A cross-sectional schematic of a typical top-gate TFT structure (in this case, n-channel).

The spatial and energy distribution of trap states within the bandgap are largely a function of how the Si film is formed. For instance, in the case of a-Si, the spatial distribution of defect states is fairly uniformly throughout the material. In the case of poly-Si, trap states are mostly localized at the grain boundaries (intergranular defects) but can also exist within the grains themselves (intragranular defects) in the form of strained or dangling bonds.[6] The energy distribution of trap state densities also differs between a-Si and poly-Si. Figure 1.8 shows a sample trap state density distribution as a function of energy within the bandgap. The Fermi level is located near the midgap (for undoped material), and the trap state density is usually higher near the conduction and valence bands. The exact shape of this curve varies depending on the physical structure of the film, which is usually dictated by the temperature and method of deposition.

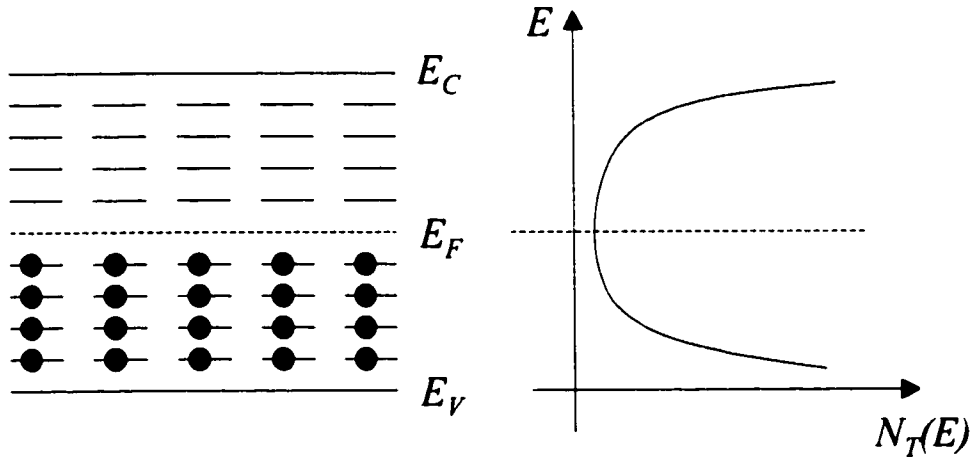

Figure 1.8. An illustration of trap state density distribution within the Si bandgap. Typically the trap state density increases near the band edges, but the exact shape of the distribution is dependent on the physical structure of the material itself. The temperature and method of film deposition is the largest determinant of film structure.

When transistors are fabricated using such high trap state density material (such as a-Si or poly-Si), electrical performance suffers in a number of ways. First, the threshold voltage is high. As the gate voltage is increased, it is initially balanced by the trapped charge in the midgap, and the trap states must be filled before sufficient mobile carrier concentration is generated for current conduction between source and drain. Secondly, the mobility is very low. The presence of defects leads to additional scattering of carriers, and the maximum achievable mobility of a-Si devices is about two orders of magnitude lower than for VLSI CMOS devices. Nonetheless, a-Si TFT technology remains the dominant transistor technology used in AMLCDs today. Why? Amorphous silicon TFTs are easily and inexpensively fabricated at temperatures compatible with low-cost glass substrates, and they provide adequate performance for the vast majority of AMLCDs.

1.2.1. Amorphous silicon TFT Technology

Amorphous silicon has no long-range order. The film is essentially a random network of Si atoms with a distribution of bond angles near the 109.5° bond angle of crystalline, tetrahedrally bonded silicon. A-Si can be distinguished from perfectly ordered c-Si and poly-Si, which consists of randomly oriented grains of single-crystalline material, as shown in Figure 1.9. While crystalline silicon exists only as a perfect matrix, both a-Si and poly-Si are not unique materials, taking on many forms depending on deposition method and temperature.

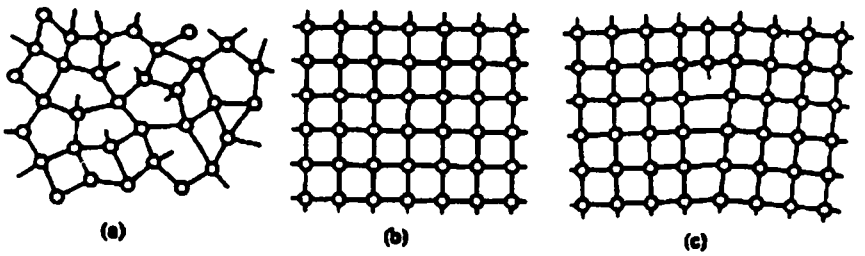

Figure 1.9. Two-dimensional schematic illustrations of the atomic structure of (a) amorphous, (b) crystalline and (c) polycrystalline silicon. Amorphous Si has no long-range order and contains many dangling bonds. Crystalline Si exhibits perfect order with no defects, and poly-Si is composed of randomly-oriented grains, where defects tend to be localized at the grain boundaries.

Deposition of a-Si and SiN_x (dielectric) is usually accomplished with plasma-enhanced chemical vapor deposition (PECVD) at low substrate temperatures (250-350°C) using a gas flow of reactants (SiH_4, NH_3), dopants (PH_3, for n-type Si), and dilution gases (N_2, Ar or He). At these temperatures, hydrogen from the reactant gas is not completely desorbed, and consequently the a-Si contains considerable quantities of hydrogen (10-30%). The presence of hydrogen is actually beneficial, serving to terminate the many dangling bonds that exist in the random network of Si atoms (thus reducing the number of electrical defects in the film).

The best a-Si films, however, yield TFTs with effective electron mobility $\leq$ $2cm^2/Vs$. While a-Si TFTs provide enough drive current to charge an LC cell, they do not have sufficient performance to be used efficiently in the peripheral circuitry that is used to address the display. As a result, conventional AMLCDs must use off-chip IC driver chips for addressing the "dumb" a-Si active-matrix. In such a scheme, there must be as many connections to the display as there are scan lines and data lines. For commonly used chip-bonding methods (such as tape-automated bonding), the pitch between the lines

is extremely tight (~60μm for 4000 lines in high-resolution displays), and the bonded wires must be able to withstand mechanical shock and thermal mismatch between the glass, silicon and polymers used in the package. Thus, strict requirements are placed on these connections, and the cost of packaging reliable external driver circuitry is high.

The higher mobility of poly-Si TFTs (vs. a-Si TFTs) makes it possible to directly integrate driver circuitry onto the display substrate periphery. In Figure 1.10, an illustration of a "dumb" a-Si active matrix display is shown in comparison with poly-Si TFT active matrix technology, where drivers for both scan and data lines are sketched. With high performance poly-Si TFT technology, the number of external connections can be significantly reduced, thus improving reliability and reducing overall system cost.

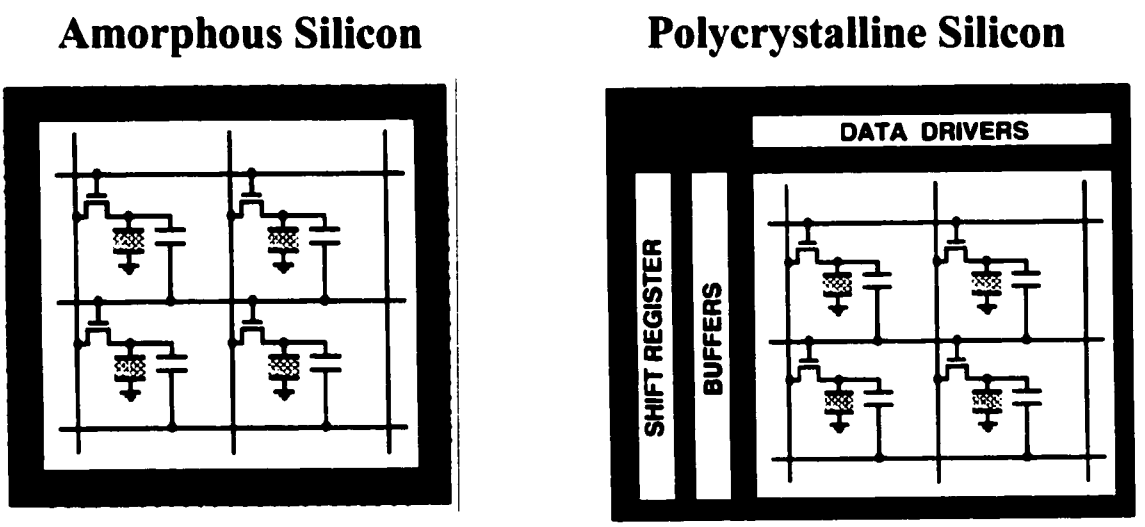

Figure 1.10. A-Si vs poly-Si technology. A-Si TFTs have carrier mobility < $2cm^2/Vs$, while poly-Si carrier mobility typically exceeds $30cm^2/Vs$. The higher performance of poly-Si TFT technology offers the possibility of: (1) higher-aperture-ratio for lower power or brighter displays (2) integration of peripheral driver circuitry, leading to reduced system cost and improved reliability.

1.2.2. Poly-Si TFT Technology

Poly-Si TFTs not only offer higher mobilities than a-Si TFTs but also lower threshold voltages and the capability to implement CMOS circuitry for reduced power consumption. (Hole mobility in p-channel a-Si TFTs is too low for practical devices, but p-channel poly-Si devices are feasible.) The higher performance of poly-Si TFTs is beneficial in a number of ways. First, the aperture ratio of the pixel can be increased, since the poly-Si TFT does not require as much area as its a-Si counterpart, resulting in a brighter display. Second, higher resolution displays are realizable, since the pixel sizes can be reduced with the smaller TFT dimensions. Third, high-speed CMOS poly-Si TFT driver circuitry can be integrated directly on the display periphery to reduce the number of external connections, which serves to reduce the packaging cost and to make the display more compact. Ultimately, it may be possible to achieve a system-on-glass, where even complex CPU logic is implemented using TFTs. Figure 1.11 illustrates how such a system might look.

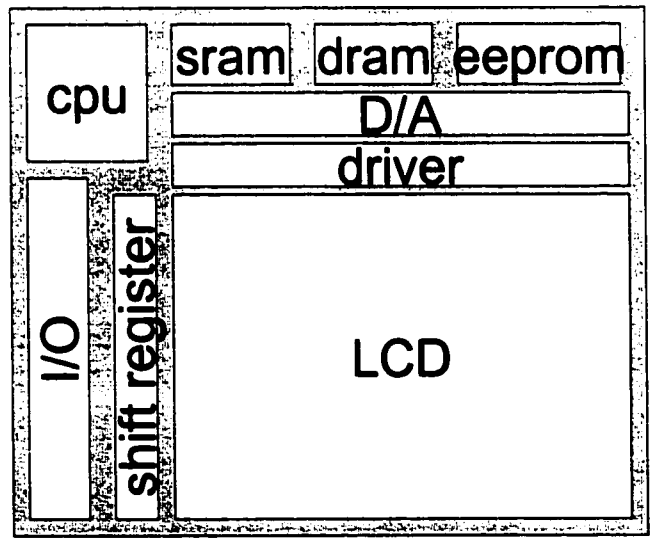

Figure 1.11. A vision of future "system-on-glass" technology, where all components are fabricated directly on the display (glass) substrate.

As mentioned previously, poly-Si has many forms. Grain size can vary from the smallest extreme, i.e. a-Si in the zero limit, to being infinitely large, i.e. crystalline silicon. Not only can grain size vary, but the quality of the Si grain can vary as well. The intragranular defect density can be different even for films having the same average grain size. However, the greatest factor in poly-Si TFT performance is grain size, because defects tend to be concentrated at the grain boundaries. Poly-Si TFTs with larger grain sizes have higher drive currents, lower leakage currents and lower threshold voltages because there are fewer grain boundaries within the active channel region. In crystallizing Si films, the eventual goal is to form a single-crystalline structure, but the immediate research focus is to achieve the largest grains possible at temperatures compatible with glass panels used in flat-panel display manufacture.

The use of poly-Si introduces additional process complexity because substrates used in flat-panel display manufacture only tolerate very low maximum process temperatures. Generally, the average grain size of the poly-Si film improves with increasing process temperature.[7] Poly-Si is optimally formed by crystallizing an a-Si precursor film, which is deposited using LPCVD or PECVD at 350-550°C. Crystallization can be accomplished by annealing at 550-600°C (known as solid-phase crystallization or SPC) or the presently preferred method of pulsed excimer laser crystallization (ELC).

Using SPC, large poly-Si grains can be obtained by annealing at high temperatures (>950°C) and/or for many hours, but such techniques are unfortunately incompatible with glass substrates. The best glass panels such as Corning 1737 has a strain point near 660°C. Thus, for SPC, the poly-Si quality is effectively constrained by

the glass substrate. For crystallization temperatures near 600°C, the average grain size can range from 500-5000Å. With minimum TFT dimensions being on the order of one micron, a number of grain boundaries will exist in the active channel.

In contrast, ELC of a-Si precursor films tends to form larger, much less faulted grains,[8] and resulting films can have mobilities approaching that of single-crystalline silicon.[9] The short-pulsed, transient nature of ELC also significantly reduces the impact of the annealing process on the underlying substrate. (The laser dwell time is short enough so that even plastic substrates with glass transition temperature as low as 150°C can be used with ELC of poly-Si.)[10] Hence, ELC is the preferred procedure for the formation of large-grained high-quality poly-Si films. There are, however, problems associated with ELC. Poly-Si grain size is highly sensitive to laser energy fluence and therefore difficult to control.[11] As a result, poly-Si TFT performance and uniformity are important issues for ELC.

Gate dielectric formation is another critical process step in low-temperature poly-Si TFT fabrication. Unfortunately, it is impossible to form a thermal oxide, which requires growth temperatures greater than 700°C. The poly-Si TFT gate oxide is typically deposited by a chemical vapor deposition technique: low-pressure CVD (LPCVD, 400°C), atmospheric-pressure CVD (APCVD, 300–500°C), or plasma-enhanced CVD (PECVD, R.T.–500°C). CVD oxides are substantially inferior to thermal oxides, having a more porous physical structure and a lower quality SiO_2/Si interface (higher density of interfacial trap states, D_{it}). The D_{it} for PECVD oxides can be as much as two orders of magnitude higher than for thermal oxide. The quality of the SiO_2/Si interface has direct impact on the threshold voltage and mobility of the TFT. Therefore, the development of a

low-temperature CVD oxide with a D_{it} close to that of thermal oxide would be a significant research contribution.

Poly-Si TFTs have generated a great deal of attention in the past decade, on account of their high performance and potential for unprecedented system integration. The business of information displays is growing rapidly, and the next section describes some of the leading trends in the display industry.

1.3 Display Industry Trends

The need for displayed information is growing with the increasing number of electronic devices. This demand has led to a few major trends in the flat panel display industry.

The first trend is toward lower power displays. Reflective display technologies such as reflective LCs will become increasingly important. However, passive-matrix reflective LC displays with simple multiplexed addressing schemes cannot be used because of their broad-transition electro-optic characteristic. Unless significant improvements are made in the LC material itself, active-matrix addressing will be required for high-resolution, reflective LC displays.

Secondly, there is a trend toward lower cost, larger area displays. OLED displays are a promising technology to address this need. Active-matrix addressing is also required for OLEDs because lifetime and efficiency degrade at high operating brightness. Passive-matrix OLEDs use a short, high current pulse scheme to drive OLEDs at low efficiency levels, which results in short lifetimes for the organic materials.[12] The active-

matrix addressing scheme provides a constant current to the pixel, reducing the power requirement and prolonging the OLED lifetime.

The third trend is toward lighter, more robust and compact displays for mobile electronics, where monolithic integration of driver circuitry is necessary to have highly portable rollup or foldable displays. To meet these demands, a high-performance transistor technology that is compatible with flexible substrates is needed. The ability to fabricate poly-Si TFTs on plastic substrates is critical to the achievement of these goals.

1.4 Organization

This dissertation addresses issues for direct fabrication of poly-Si TFTs on flexible plastic substrates. The formation of high-quality gate dielectrics at ultra-low temperatures (≤150°) is a critical step in the achievement of a high-performance TFT-on-plastic technology. Chapter 2 presents two methods for depositing low interfacial defect density SiO_2 using high-density plasma (HDP) CVD tools, namely electron cyclotron resonance (ECR) and helicon sources. We fabricated simple NMOS capacitors using an aluminum gate material and performed capacitance measurements for various deposition conditions. The highest-quality gate dielectrics were then selected for use in ultra-low temperature poly-Si TFT fabrication described in Chapter 3. This chapter presents the specific process methods used: sputtered a-Si, excimer laser annealing for poly-Si formation, ECR and helicon source PECVD oxide deposition, and laser-assisted source/drain formation. In Chapter 4, we present a method for improving poly-Si TFT uniformity by controlling grain growth using excimer laser crystallization. A patterned, anti-reflective oxide capping layer was used to align large-grained poly-Si to the active

channel region. N- and p-channel TFTs were fabricated using various laser fluences and compared. Chapter 5 describes an active-matrix organic light-emitting diode (AMOLED) prototype display designed in collaboration with Universal Display Corporation. The 128-by-64 pixel prototype utilizes a 2-TFT pixel design, and the fabrication process was designed to integrate seamlessly with backend OLED deposition. Lastly, in Chapter 6, a method for simplifying conventional lithography methods for large-area electronics manufacture is presented. We describe preliminary work on a direct patterning method using an excimer laser and Si_xGe_{1-x} as a sacrificial material for transferring patterns without the use of resist and traditional optical lithography methods.

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Chapter 2

Ultra-Low Temperature Gate Dielectric Formation

2.1 Introduction

Much of the success of modern microelectronics can be attributed to the inherent ability of Si to form a stable, high-quality dielectric of silicon dioxide (SiO_2) on its surface. Silicon dioxide (referred to as simply "oxide") grows readily on a bare Si surface, even at room temperature in air. In very-large-system-integration (VLSI) integrated circuits (ICs), oxide is commonly formed by thermal oxidation, a high-temperature ($\geq$700°C) process that uses either O_2 (dry) or H_2O (wet) ambients. The elevated temperature supplies the energy needed for reactions to occur between the Si

surface atoms and the gaseous oxygen atoms, and the resulting oxide typically has an exact stoichiometric ratio (SiO_2) and is strongly bonded to the Si surface. Thermally grown oxides have stable and controllable electrical properties, so they are the preferred gate dielectric for metal-oxide-semiconductor field-effect transistors (MOSFETs).

However, no oxide is electrically perfect or defect free. There are various types of traps and charges that exist in the bulk SiO_2 and at the Si-SiO_2 interface. These defects have a profound effect on the characteristics and performance of the devices fabricated in the underlying silicon. There are four basic types of charges that exist in the oxide itself or near the Si/SiO_2: (1) interface trap charge, Q_{it} (2) fixed oxide charge, Q_f (3) bulk oxide trapped charge, Q_{ot} and (4) mobile ionic charge, Q_m. The precise origin of the interface trap states is not well understood, but it is known that these trap states exist within the Si bandgap, and thus their charge state changes with gate bias if the interface trap is moved past the Fermi level, changing its occupancy. The fixed oxide charge is also associated with the Si/SiO_2 interface but is located in the oxide about 30-40Å away from the Si surface. Unlike Q_{it}, the fixed oxide charge occupies energy levels outside the bandgap and does not change charge state with applied bias. Bulk oxide trapped charge can be located anywhere in the oxide and is associated with defects, such as impurities and broken bonds. All the charge types discussed so far can be effectively reduced by annealing the oxides at elevated temperatures. Only the mobile ionic charge is essentially independent of process temperature; Q_m is commonly caused by the presence of ionized alkali metal atoms, such as Na^+ and K^+, and can be reduced with a cleaner deposition system.

Oxide quality depends strongly on both the method of formation and post-formation annealing. Other than thermal oxidation, oxide can be formed by low-pressure chemical vapor deposition (LPCVD), plasma-enhanced CVD (PECVD) and physical vapor deposition (sputtering). In VLSI applications, CVD oxides have found extensive use for insulation between layers of interconnect, as getters, as diffusion sources, as diffusion and implantation masks, as capping layers to prevent outdiffusion, and as final passivation layers.[1] But deposited oxides are generally of much lower quality than those that are thermally grown.[2] Thus, CVD oxides are rarely used as gate dielectrics in VLSI devices.

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) fabricated on plastic substrates *must* use gate dielectrics formed by low temperature deposition. SiO_2 is also the preferred dielectric because it can form a better interface with Si than other options such as silicon nitride. Plastic has a very low strain point; the most advanced polymer substrates can only tolerate a maximum process temperature of ~200°C (see Chapter 3 for details), so the preferred method of thermal oxidation is impossible. LPCVD SiO_2 requires temperatures in excess of 350°C, which is also incompatible with plastic. Sputtering of SiO_2 can be done as low as room temperature, but interface quality is typically poor and impurities from the chamber walls can easily be incorporated into the oxide film. Conventional radio frequency (13.56 MHz) (RF) PECVD can be used to deposit oxides at temperatures down to 100°C, but the quality of the Si/SiO_2 interface generally decreases with decreasing deposition temperature, resulting in poor TFT performance and reliability. It has been shown that RF PECVD oxide formed below 250°C results in dramatically degraded poly-Si TFT performance.[3] High-density plasma

(HDP) processing is the best method of attaining high-quality Si/SiO_2 interfaces at ultra-low, plastic-compatible temperatures (<150°C).

In this chapter, we describe two types of HDP systems (electron cyclotron resonance (ECR) PECVD and helicon source PECVD). We present electrical data for oxides deposited at temperatures compatible with plastic substrates using these tools. The work presented in this chapter provides an optimum gate dielectric for the ultra-low temperature fabrication of poly-Si TFTs described in Chapter 3.

2.2 Electron Cyclotron Resonance PECVD

2.2.1 Background and System Configuration

ECR PECVD allows for low temperature deposition of high quality thin oxide films. Using a microwave power source and electromagnets, high-reactivity plasmas can be generated under ECR conditions.[4] High densities of low-energy ions enhance surface reactions without the need for substrate heating. ECR systems can generate plasma densities as high as $5x10^{12}$ cm^{-3}, which are 2-3 orders of magnitude higher than those achievable in RF PECVD tools.[5] Figure 2.1 shows a schematic of the ECR PECVD system used in this work.

The ECR reactor uses an electromagnet that produces a magnetic field for the resonance zone near the top of the chamber, where the 2.45GHz microwaves are injected. Oxygen and dilution gas mixtures are delivered into the ECR source and a high-density plasma is formed. The wafer sits on a graphite chuck in the lower portion of the chamber, and silane (SiH_4) is injected directly above the wafer. Oxygen ions diffuse from the ECR

zone toward the substrate and dissociate the SiH_4, which react with the oxygen to form SiO_2 on the wafer. The spool piece distances the ECR zone from the wafer surface, improving uniformity and reducing substrate temperature heating. The lower magnet was not used in the experiments, since its use worsened uniformity without providing any noticeable benefit in the deposited film quality. Although the substrate was not deliberately heated, the temperature increased due to the ion bombardment during deposition. Typically, the base pressure of the system was ~$8x10^{-8}$ torr. Gases available in the ECR chamber were SiH_4, Ar, O_2, and N_2.

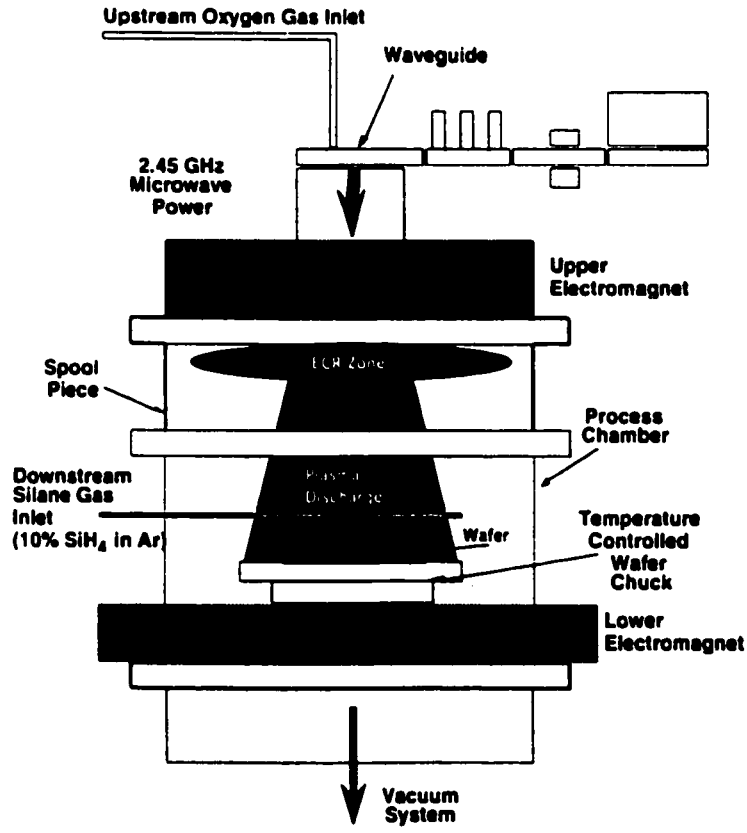


Figure 2.1. Schematic diagram of the ECR PECVD system.

2.2.2 Experiments

A number of experiments were carried out in the ECR PECVD system to determine the best conditions for gate oxide deposition without substrate heating. Optimum conditions were determined by systematically varying the following parameters: microwave power, reactant gases, gas flow rates, and deposition time. The wafer surface temperature was measured for various deposition conditions to ensure compatibility with plastic substrates. The studies are described below and their results are presented. Since we use the deposited oxides as the gate dielectric in poly-Si TFTs, we are interested chiefly in their electrical characteristics. Thus, we fabricated simple test capacitors on lightly doped Si wafers by depositing blanket oxides to a thickness of 1000Å and then patterning aluminum gates on top of the oxide films to form capacitors of various sizes. We measured the high-frequency (100kHz) capacitance-voltage (CV) and current-voltage (IV) characteristics of the capacitors to determine the oxides' suitability for use in poly-Si TFTs.

ECR vs. LPCVD LTO and RF PECVD oxides

In the first experiment, we used an existing oxide deposition recipe (which we will refer to as the "standard" recipe), which had been optimized for superconductor IC fabrication. Dielectrics used in superconducting ICs have similar deposition temperature requirements as those used with polymer substrates. The parameters for the "standard" ECR oxide recipe are shown in Table 2.1.

PARAMETER	VALUE
Power	350W
SiH_4 flow rate	100 sccm
O_2 flow rate	20 sccm
Ar flow rate	120 sccm
Pressure	5 mTorr

Table 2.1. "Standard" ECR oxide deposition parameters. These were the parameters for the first ultra-low temperature gate oxide experiment. They do not reflect the optimum deposition conditions.

In this initial experiment, the quality of the standard ECR oxide was compared with oxides deposited using LPCVD at 450°C and RF PECVD at 100°C. Capacitors were fabricated on lightly doped n-type Si wafers in the following manner. First, the Si wafer was cleaned and placed in an HF bath to remove all native oxide. Immediately following the HF dip, the wafer was placed in the deposition chamber, and oxide was deposited to a thickness of 1000Å. The blanket film was then capped with 3000Å of sputtered Al. These thicknesses were chosen to be representative of the gate dielectric and metal thicknesses used in the TFTs. Lithography and etching defined squares in the Al film that determined the capacitor size. The backside of the wafer served as the bottom electrode of the capacitor.

High-frequency CV measurements were performed on the completed capacitors. Figure 2.2 compares the CV curves for the 450°C LPCVD oxide (LTO), the unheated pure ECR oxide, and the 100°C pure PECVD oxide. The ECR oxide exhibits steep characteristics similar to that of the 450°C LTO, demonstrating that a similar quality Si/SiO_2 interface is achieved with ECR. The shallow slope of the PECVD oxide CV

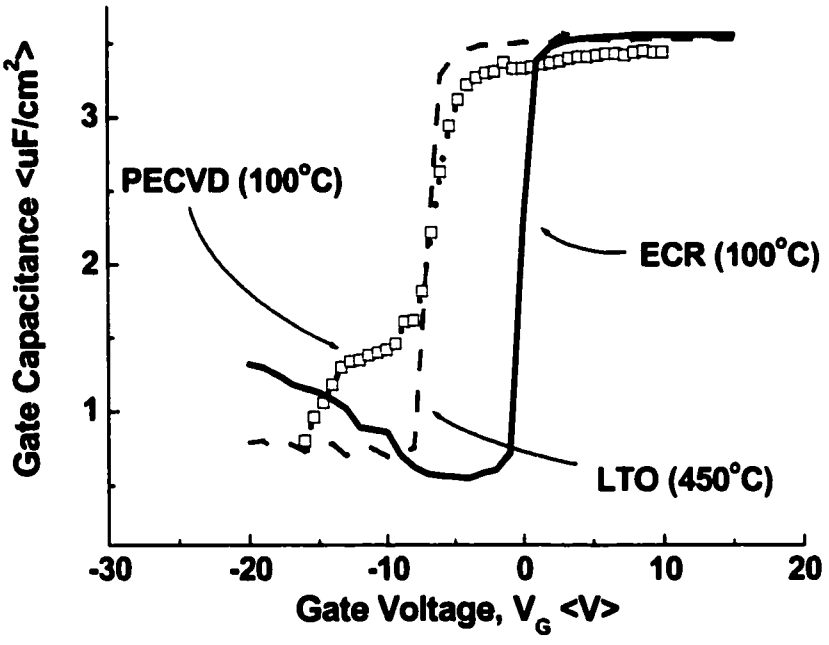


Figure 2.2. High-frequency CV characteristics for 450°C LPCVD, 100°C PECVD and 100°C ECR oxides (0.1μm thick). The ECR oxide exhibits a silicon-oxide interface quality superior to that of PECVD oxide and close to that of the LTO.

characteristic indicates a higher density of interface trap states. Variations in capacitance values are due to slight differences in oxide thickness arising from process variation.

Unfortunately, the IV characteristics of the ECR oxide indicate that it has poor bulk properties. Figure 2.3 shows leakage characteristics and breakdown voltages of the devices. The pure ECR oxide exhibits excessive leakage current even at moderate values of gate voltage, and it also has an unsatisfactorily low V_{bd}. The largest breakdown voltage is achieved with a pure PECVD oxide. Through the use of a composite ECR/RF-PECVD oxide (200Å/800Å), both good interface quality and acceptable leakage current can be achieved. The composite ECR-PECVD oxide CV characteristic is shown in Figure 2.3. It has a lower breakdown voltage than that of pure PECVD oxide, but the breakdown field is still >4 MV/cm.

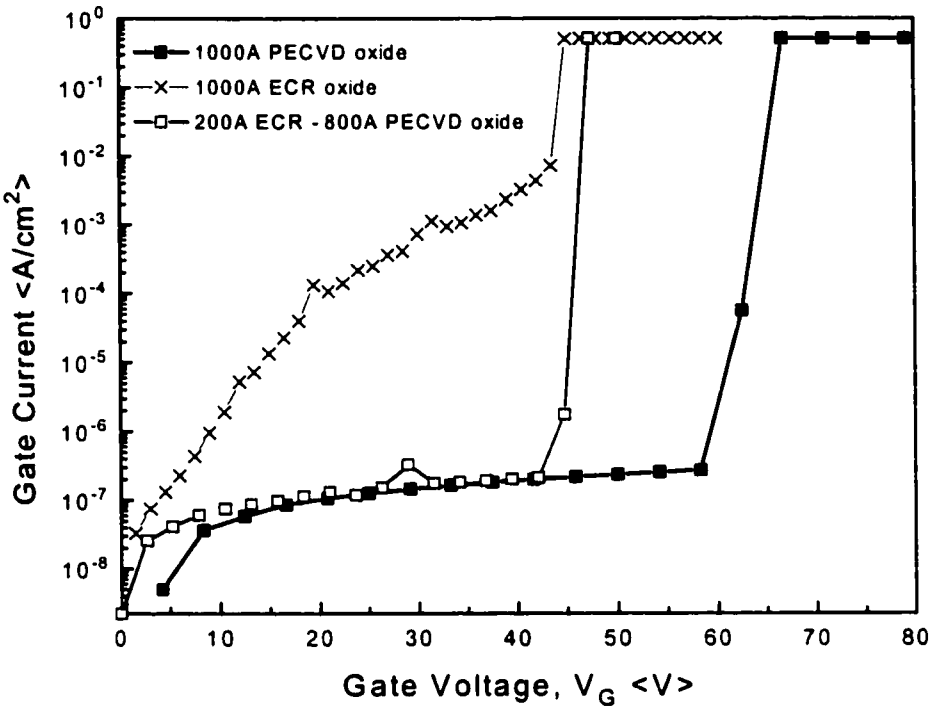


Figure 2.3. Comparison of oxide breakdown voltages. The ECR-PECVD stack shows superior leakage current characteristics to a pure ECR oxide, but smaller breakdown voltage than pure PECVD oxide.

Improvement of ECR oxide leakage current

The standard oxide deposition recipe in the ECR system yielded a porous, electrically leaky film. It was unlikely that the ECR system inherently produces such high leakage oxides, so we aimed to improve the bulk properties of the oxide without adversely affecting the good interface properties. The starting point for the experiment was to lower the silane flow rate, because a lower deposition rate leads to a denser, less porous oxide. The lowest SiH_4 flow rate possible was found to be 40sccm. Below this point, the plasma was unstable and the reflected power fluctuated wildly. (For silane flow rates between 60-100 sccm, there was no appreciable change in the oxides.) Next, we

replaced Ar with N_2 as the carrier gas. It was reported that ECR N_2O plasma oxides grown on poly-Si had the effect of smoothing the interface with poly-Si.[6] Because our system did not have N_2O available, N_2 was flowed at twice the rate of O_2, so that the relative densities of reactant ions would be similar. Lastly, the power was increased. We found that it was necessary to run the plasma at powers ≥500W to see improvements in the oxide. The pressure was kept as low as possible (~5mTorr) to maintain a high plasma density.[5] Table 2.2 shows the parameters for the low leakage, low SiH_4 flow rate oxide.

PARAMETER	VALUE
Power	>500W
SiH_4 flow rate	40 sccm
O_2 flow rate	75 sccm
N_2 flow rate	150 sccm
Pressure	5 mTorr

Table 2.2. Low SiH_4 flow rate ECR oxide recipe. The above conditions yield an oxide that has leakage characteristics similar to that of 450°C LPCVD LTO.

Simple Al-gate capacitors were fabricated using this new recipe (1000Å oxide thickness) and compared with the standard ECR oxide and 450°C LTO. Figure 2.4 shows the oxide leakage characteristics. The new low SiH_4 flow rate recipe yields an oxide with leakage characteristics comparable to LTO, while the leakage current of the standard recipe exceeds both.

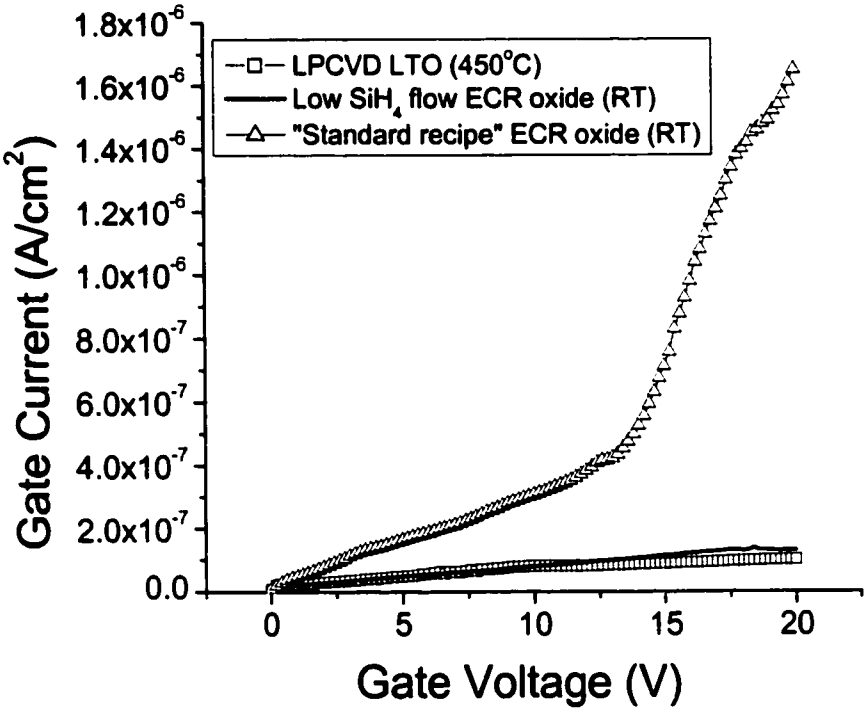


Figure 2.4. Improvement in leakage current with new, low-SiH_4, N_2, O_2 gas flow recipe in the ECR system. The low leakage oxide was deposited at 500W microwave power using the gases listed in Table 2.2.

Interface characteristics achieved with the low leakage oxide were similar to those seen using the standard recipe. Figure 2.5 compares the CV curves for capacitors fabricated using the standard ECR oxide and the low leakage ECR oxide recipe. The substrate was a lightly doped p-type Si wafer. Comparable interface quality is achieved for the two ECR oxides.

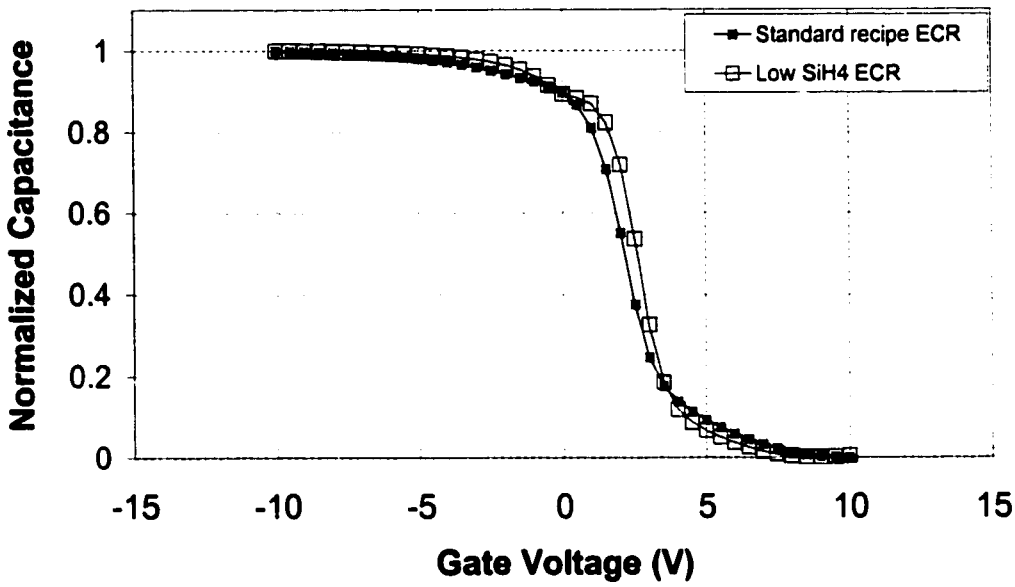


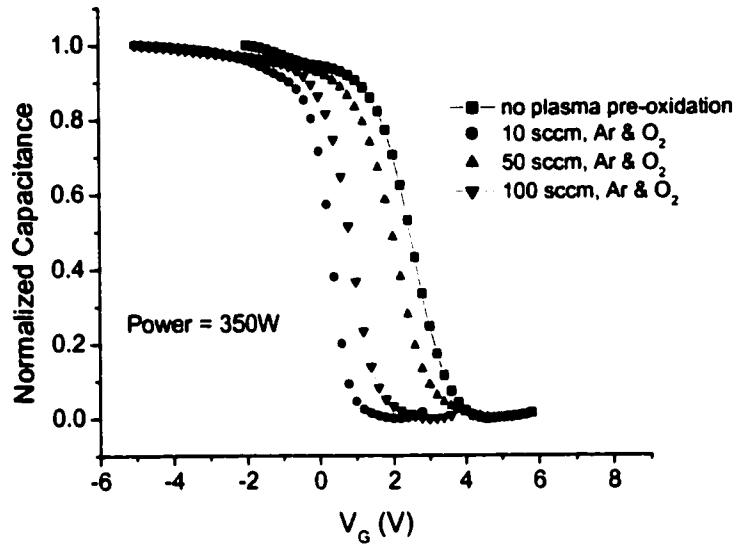
Figure 2.5. No loss in interface quality is seen with the new low SiH_4 flow rate ECR oxide. LTO contains some fixed charge that causes the shift towards positive gate voltages.

One disadvantage of using a low silane flow rate is that the deposition time increases. The new low leakage oxide recipe lengthened the required deposition time by nearly five times. At 800W, the ECR plasma can cause the substrate temperature to rise substantially, especially if the run time is long. It was important to know whether the temperature rise led to the observed improvement in oxide quality. The temperature study is explained in a later section.

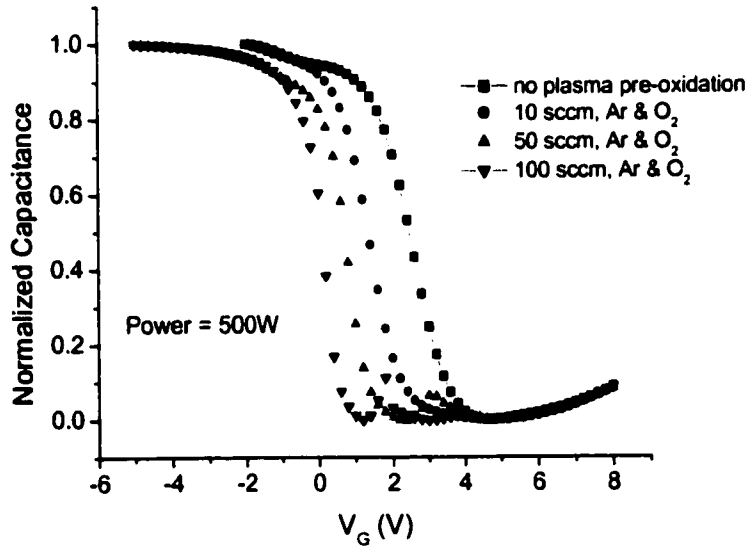
Oxygen Plasma Pre-Treatment

The effect of pre-treating the Si surface with oxygen plasma prior to oxide deposition was investigated. O_2 and Ar were flowed at equal rates (O_2=Ar=10, 50, and 100 sccm), and power was varied (350, 500, 600, 700W) to determine the impact on the interface quality. The oxygen plasma pre-treatment was run for 120 seconds, and then it

was followed by deposition of standard recipe ECR oxide to a thickness of 1000Å. Figure 2.6a-d shows the CV characteristics for capacitors fabricated using the described splits.

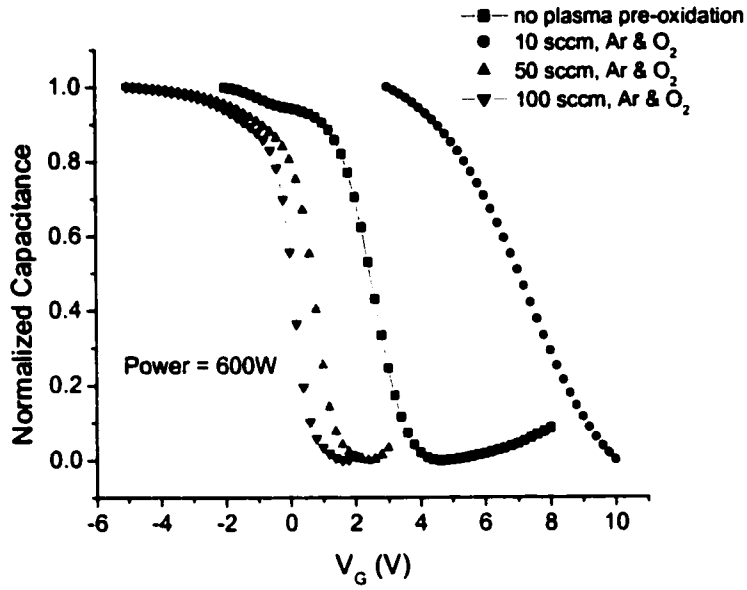


(a)

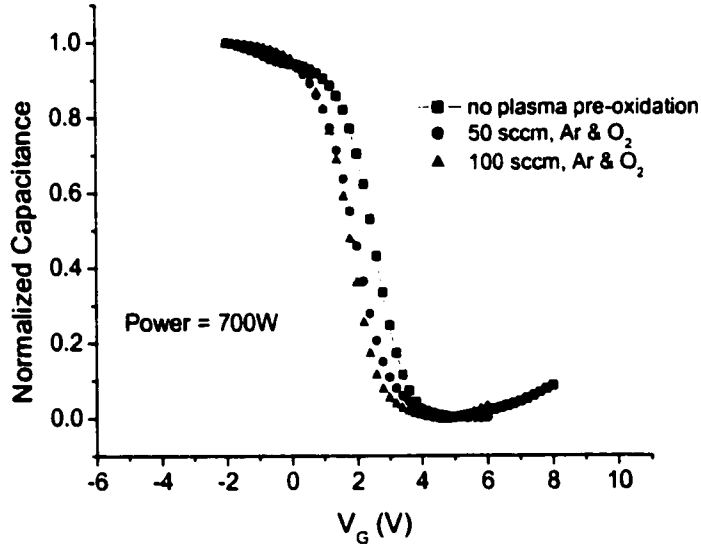


(b)

Figure 2.6 (a) & (b). *continued on next page*



(c)



(d)

Figure 2.6 (c) & (d). CV characteristics for ECR oxygen plasma pre-treated oxide capacitors. Microwave power was varied from (a) 350W, (b) 500W, (c) 600W to (d) 700W, and the oxygen plasma was run for 120 seconds in all cases. The optimum condition for O_2 plasma pre-treatment was found to be with O_2=Ar=100sccm at 500-600W.

The benefit of an oxygen plasma pre-treatment step is seen for nearly all ECR conditions. The anomalous result for 10sccm gas flows at 600W is due to plasma instability. At such low gas flows, the plasma had difficulty sustaining itself and the reflected power was highly unstable. The problem was only exacerbated at 700W, where the gas flows of O_2=Ar=10sccm was too low to even strike a plasma. The best characteristics are seen for 100sccm gas flows around 500-600W of microwave power. At these conditions, the CV characteristics are steep and the flatband voltage is low (desirable for low TFT threshold voltage).

Wafer Surface Temperature in ECR Chamber

Under ion bombardment, the surface temperature of the wafer rises. An experiment was carried out to quantify the substrate heating in the ECR chamber. Temperature-sensitive adhesives were mounted on Si wafers, and various plasma conditions were run in the ECR chamber. The stickers changed color when their designated temperature was reached, and through the use of assorted dots (i.e. sensitive at 99°C, 110°C, 116°C, 127°C, 138°C, 149°C, 163°C, and 177°C), the temperature was measured as a function of time for given plasma conditions. For microwave power levels up to 350W, the wafer surface did not exceed 150°C (the T_g of a common plastic, polyethylene terephthalate or PET) even for depositions that lasted several minutes. Since the optimum oxide formation process sequence required power $\geq$500W, extra care was taken to ensure that the use of higher power levels does not cause the substrate temperature to exceed 150°C.

The processes that require high power are the oxygen plasma pre-treatment and the reduced SiH_4 flow rate, low leakage recipe. Figure 2.7 shows the evolution of temperature in the system as a function of run time and recipe. A thick bar indicates the 100°C mark, which is the preferred maximum process temperature for poly-Si TFTs on plastic. (The gate dielectric deposition usually demands the highest sustained temperature in the poly-Si TFT fabrication process.) It is important to note, however, that these results are only an approximate indication of the actual substrate temperature: the temperature dots themselves have error; the surface temperature differs considerably from the temperatures at substrate depths; lastly, the thermal conductivity of the Si wafer is significantly higher than glass or plastic. For TFT fabrication on silicon substrates, these data represent the worst case temperature rise.

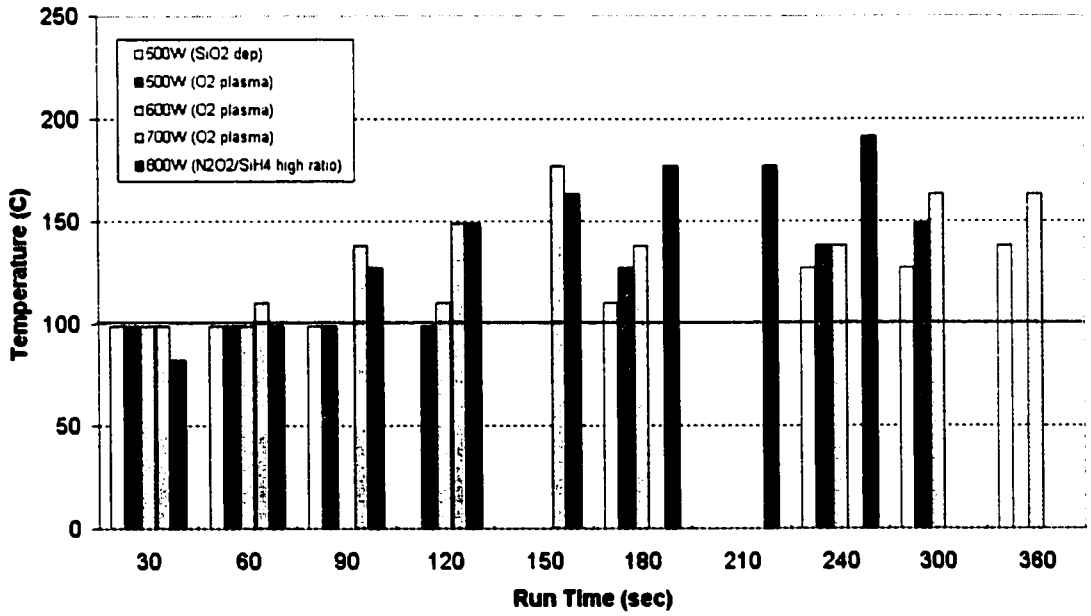


Figure 2.7. Wafer temperature in the ECR PECVD system as a function of time. Surface temperature is also a function of the particular recipe, since gas flows and pressures vary.

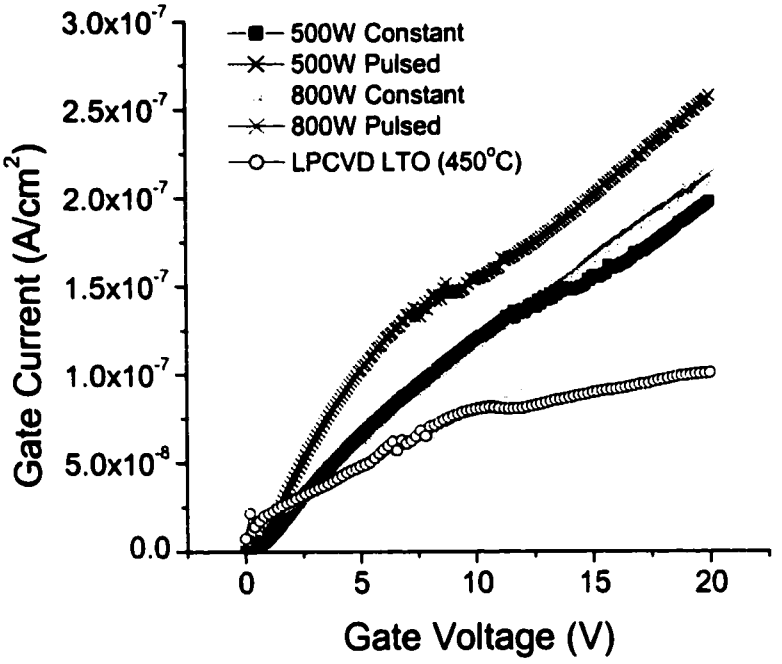


Figure 2.8. Leakage current as a function of pulsed vs. constant mode deposition in the ECR PECVD system. Oxide thickness is 100nm.

It can be seen from the figure that, for most plasma conditions, the surface temperature exceeds 100°C after 120 seconds. Thus, it is necessary to use a pulsed mode operation for depositions or treatments requiring longer times. Pulsed mode depositions break up the plasma run time into smaller durations with lag times, so that substrate cooling can occur.

Pulsed mode deposition was performed for the low leakage oxide recipe. The cycle executed as follows: gas stabilization (60 sec), deposition (150 sec), and cooling (60 sec of 50 sccm N_2). Results are shown in Figure 2.8 for 100nm-thick oxides. The pulsed mode deposited oxides have slightly higher leakages for both 500W and 800W depositions, but the leakage currents are tolerable. The CV characteristics were indistinguishable for pulsed mode vs. constant mode depositions. Thus, pulsed mode

deposition is a viable method to achieve high-quality, low temperature oxides. The obvious disadvantage is the longer process times required.

2.3 Helicon Source PECVD

2.3.1 Background and System Configuration

Typical plasma density values for helicon source plasmas are roughly $1x10^{13}$ – $5x10^{13}$ cm^{-3}, which is about an order of magnitude higher than typical ECR plasma densities.[7] The helicon source PECVD reactor uses an RF frequency (13.56 MHz) antenna to couple power into the plasma. As shown in Figure 2.9, the antenna consists of two loops placed diametrically on the outside of the source chamber. This antenna produces a transverse RF magnetic field perpendicular to both the main chamber axis and the constant axial magnetic field generated by the solenoids shown in the figure. The RF field excites one mode of the helicon wave in the source tube, which in turn transfers energy to the plasma electrons. Various frequencies ranging from 2 to 70 MHz can be used with excellent results, but the use of 13.56 MHz is historically practical and has the added benefit of giving a plasma wavelength of 22cm, a convenient size for reactor geometry.[8]

Gases were introduced into the chamber in a configuration nearly identical to that of the ECR system, but with only O_2 and SiH_4 available. Oxygen gas entered the chamber at the top of the source tube where the helicon plasma was generated. Silane was flowed evenly over the wafer using a gas distribution ring that was located approximately 3 cm

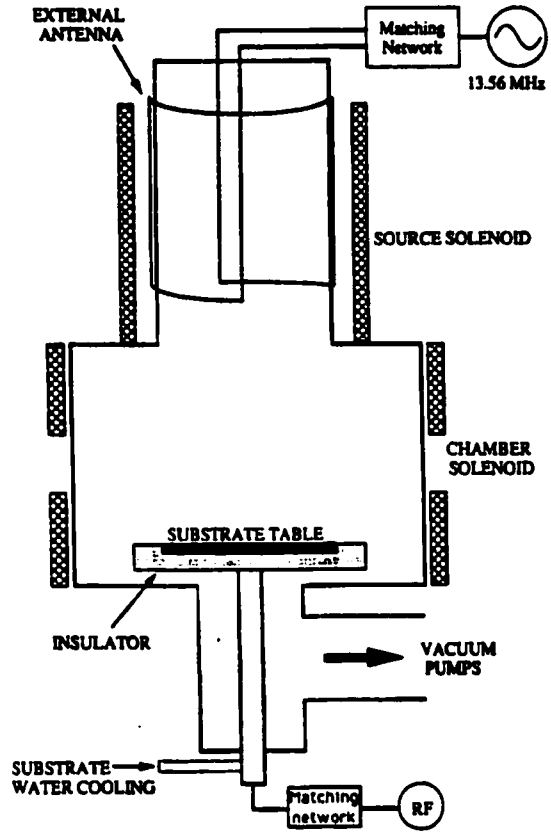


Figure 2.9. Schematic diagram of the helicon source PECVD process chamber (from A.J. Perry et al., *J. Vac. Sci. Technol.*, B 9 (2), 1991). Missing from the diagram is the SiH_4 ring that evenly distributes the gas from a distance of ~3cm from the surface of the substrate.

above the wafer. Typical process pressures were in the 1 to 12 mTorr range, with exact values depending on the gas flow rates and turbo valve aperture.

2.3.2 Experiments

A variety of helicon chamber process conditions were run to determine the best achievable oxide interface and bulk characteristics. Initially, experiments were run to determine the maximum possible power that could be used with plastic substrates. Wafers cut from 175μm-thick PET were placed in the chamber and the plasma was run for 10 minutes at 400W, 500W, 600W, and 700W. SiH_4 and O_2 were introduced into the

chamber at the equal rate of 10sccm. The plastic suffered no damage, even when run at 700W for 10 minutes. The separation between the helicon resonance zone and the wafer itself is approximately 40cm, so the physical ion bombardment is relatively low. All subsequent experiments were performed at 700W to achieve the highest possible plasma density.

Since ECR and helicon sources generate plasmas with similar characteristics, the main objective was first to develop a dense, low leakage oxide. Blanket oxides were deposited on Si wafers, and oxide characteristics were measured using a mercury probe. Figure 2.10 shows the leakage currents for oxides deposited using various gas flows and SiH_4/O_2 ratios. Increasing oxygen flow has the effect of increasing the deposition rate, leading to porous, leaky oxides. However, the pressure was a variable in the experiment because the pumping speed remained the same for all gas flows.

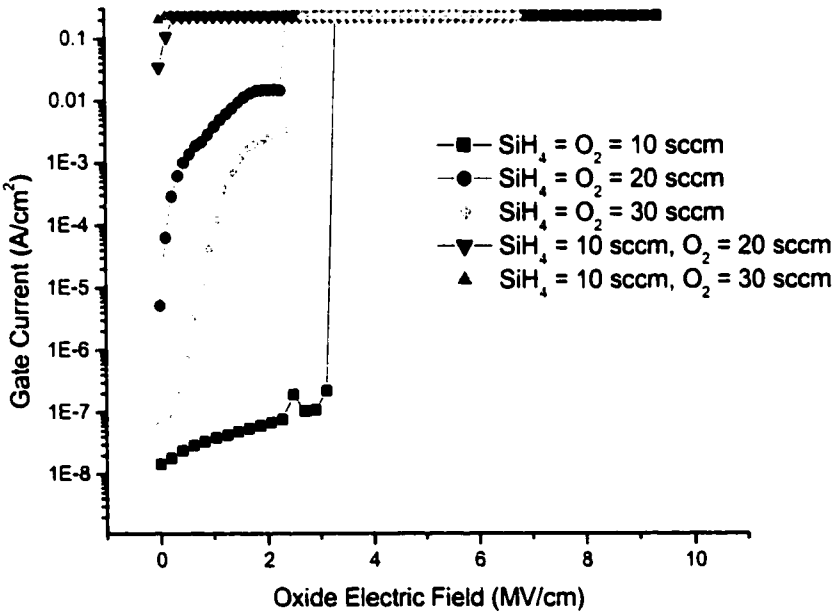


Figure 2.10. Leakage characteristics for helicon oxides deposited on Si wafers using the indicated gas flows. 100nm-thick oxides were deposited at 700W without substrate heating.

An experiment was then performed to determine the effect of pressure on leakage current. Using the best result from Figure 2.10 (SiH_4=O_2=10 sccm), the turbo pump valve aperture was systematically adjusted to control the pressure in the chamber during deposition. Figure 2.11 shows the leakage currents for oxides deposited at five different pressures. Leakage increases monotonically with pressure, so it is best to use the lowest possible chamber pressure. In the helicon system, this condition is achieved by flowing silane and oxygen at 10sccm and fully opening the turbo pump valve.

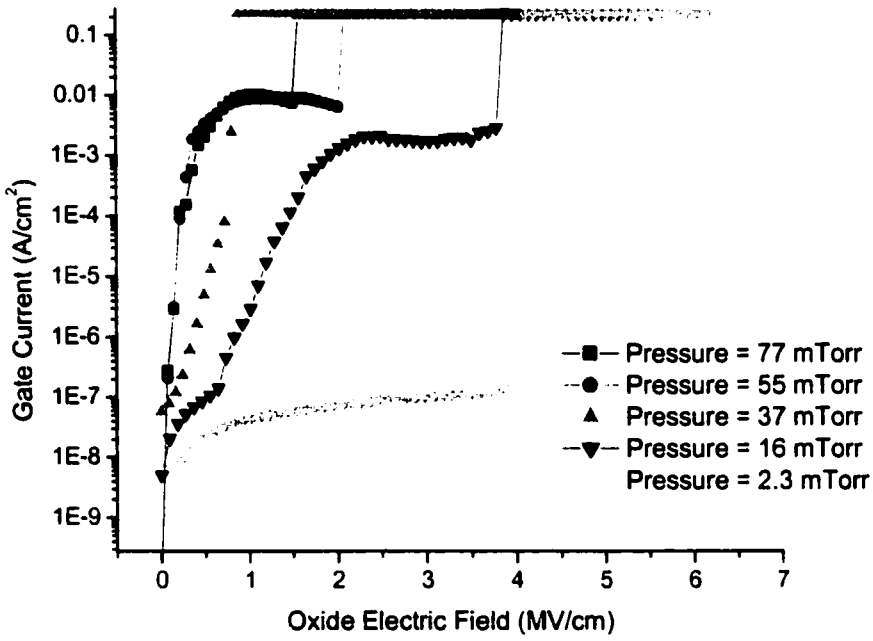


Figure 2.11. Leakage characteristics for helicon oxides deposited at various pressures. (SiH_4=O_2=10sccm; power=700W; T_{ox}=100nm)

Similar to the ECR system, oxygen plasma pre-treatment in the helicon system improves interface quality. Plasma oxidation of Si wafers was performed at low pressure (2.5mTorr, 20sccm O_2 flow) and high power (700W) for various durations. Then, the thin oxides were capped with 100nm-thick 100°C RF PECVD oxides for testing. CV

characteristics for this experiment are shown in Figure 2.12 (w/o RF substrate bias) and 2.13 (w/ RF substrate bias). After approximately 6.5 minutes of plasma oxidation, there is no further improvement. Measurement of the thin oxide shows a logarithmic growth curve (Figure 2.14), where little change in oxide thickness occurs after 400 seconds (~6.5 minutes). There is no added benefit to longer plasma oxidation durations, only possible downsides such as temperature elevation, plasma damage, etc. The use of RF bias on the substrate does not change the oxide quality significantly, but it changes the shape of the plasma so that thickness uniformity is degraded slightly. These results indicate that the use of RF bias is not necessary.

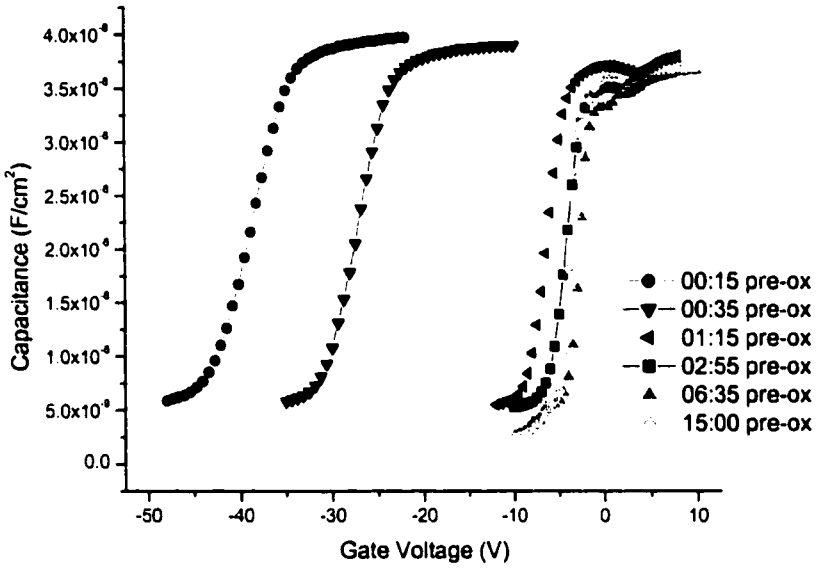


Figure 2.12. Effect of helicon plasma pre-oxidation on interface quality. No improvement is seen after 6:35 of oxygen plasma treatment. Plasma conditions: Pressure=2.5mTorr, O_2=20sccm, Power=700W, no RF bias.

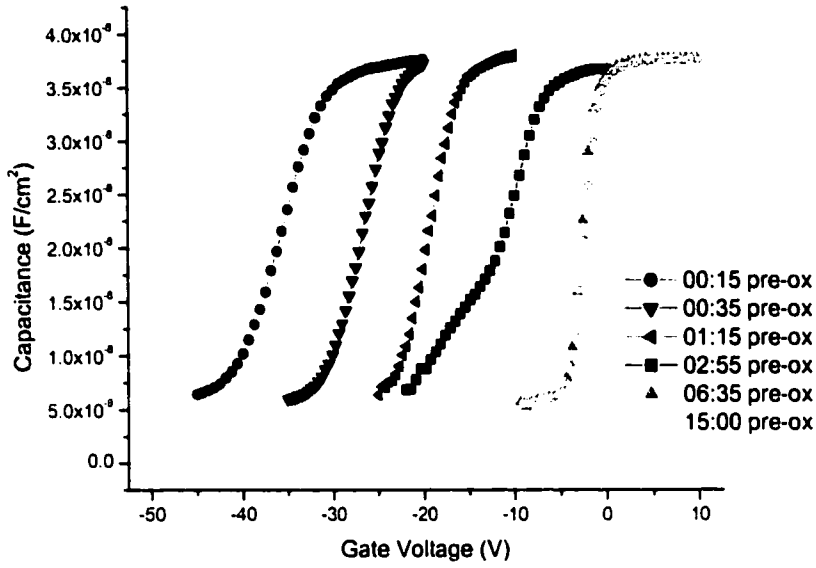


Figure 2.13. Same as Figure 2.12, but with RF substrate bias (–55V DC). Plasma conditions: Pressure=2.5mTorr, O_2=20sccm, Power=700W, with RF bias.

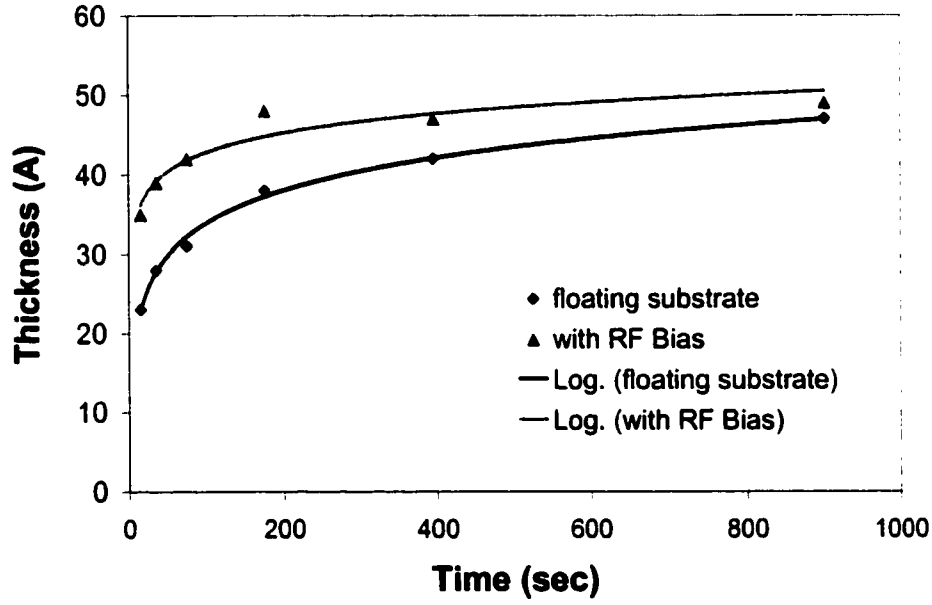


Figure 2.14. Helicon plasma oxidation growth curve. (Same oxygen plasma conditions as in Figure 2.12.) Little growth occurs after 400 seconds, corresponding to the limit on interface improvement as seen in Figure 2.12. The solid lines are a logarithmic fit to the measured data points.

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Chapter 3

Ultra-Low Temperature Fabrication of Poly-Si TFTs

3.1 Introduction

Flat-panel displays that are high-resolution, low power, lightweight, rugged, and portable will be well suited for wide ranging applications in both military and commercial sectors. If the feature of flexibility in displays were added, a vast array of entirely new markets could be created. The development of a high-performance active-matrix technology that is adaptable to plastic substrates is critical to achieving this vision for the future. In this chapter, a method for fabricating high-performance poly-Si TFTs at a maximum process temperature of 100°C is described. This process was demonstrated to

yield the highest performance TFTs for any technology compatible with polyester substrates, at the time of the work.

3.1.1 Polymer substrates: Advantages and Disadvantages

The primary advantages of plastic substrates with respect to glass are a reduction in the weight of the display and an alleviation of the problem of display breakage[1], both during fabrication and use. Plastic substrates are also significantly cheaper than the types of glass currently used in displays. The vast majority of plastics typically cost only cents per square foot while the cost of Corning Code 1737 glass, used in AMLCDs, is orders of magnitude higher. Another advantage for displays fabricated on plastic substrates is the potential to be more compact, since plastic thicknesses are usually <200μm, compared to 0.5mm for glass. Polymer substrates are also an ideal platform for the development of ultra-large displays, such as those used in advertising and other large-scale information systems, due to their compatibility with roll-to-roll processing.

Clear plastic substrates would therefore appear to be a superb alternative to glass. However, the introduction of plastic into a poly-Si TFT fabrication process has its attendant disadvantages. Standard processing techniques for both amorphous and polycrystalline TFTs require temperatures far in excess of those compatible with commonly available plastics. The maximum standard processing temperatures (T_{max}) of 350°C for conventional a-Si:H TFTs and 600°C for poly-Si TFTs are well above the glass transition temperature (T_G) for most varieties of polymer substrates. Plastic also has poor thermal stability compared to glass; the coefficient of thermal expansion (CTE) for plastics generally range from 20-100x10^{-6} °C^{-1} while Corning Code 1737 glass has a CTE of 3.8x10^{-6} °C^{-1}, which is much closer to that of silicon (CTE of Si is 2.5x10^{-6} °C^{-1}). The

large thermal expansion mismatch can produce significant stress in the deposited Si (or SiO_2) films when the samples are heated during processing. This has led some researchers to attempt to reduce the T_{max} needed to fabricate a-Si:H TFTs with promising results[2,3,4]. It remains to be seen whether or not these modified processing techniques are readily transferable to commercial application. But for *poly-Si* TFTs, simple modifications of standard processing techniques to reduce the T_{max} to one suitable for plastic substrates are clearly not feasible. Previously, the process barrier for poly-Si on plastic was dictated by the lowest temperature needed to crystallize a-Si using some form of solid-phase crystallization, e.g. conventional furnace annealing or rapid thermal processing (RTP).

There is a wide variety of polymer substrates available, but not all are suitable for poly-Si TFT processes, so careful selection is necessary. There are several material requirements for the plastic. First, it must be compatible with the standard wet chemicals used in semiconductor processing, e.g. hydrofluoric acid, photoresists, acetone, various metal etchants, etc. Second, the plastic must be able to withstand laser processing, but the use of a protective barrier film often can ease this constraint. Third, it should have high optical quality so that it can be used for transmissive displays (such as AMLCDs). Fourth, the plastic should be both flexible and cheap (i.e. cost-effective to use plastic over conventional glass substrates). Lastly, the CTE ideally matches that of silicon; this is the most difficult requirement to meet, and currently the optimum CTE for flexible plastics is still at least an order of magnitude larger than that of Si. It turns out that many polymers fulfill most of these requirements, but they vary in their T_{max}. Figure 3.1 lists a number of candidates and their respective maximum tolerable processing temperatures.

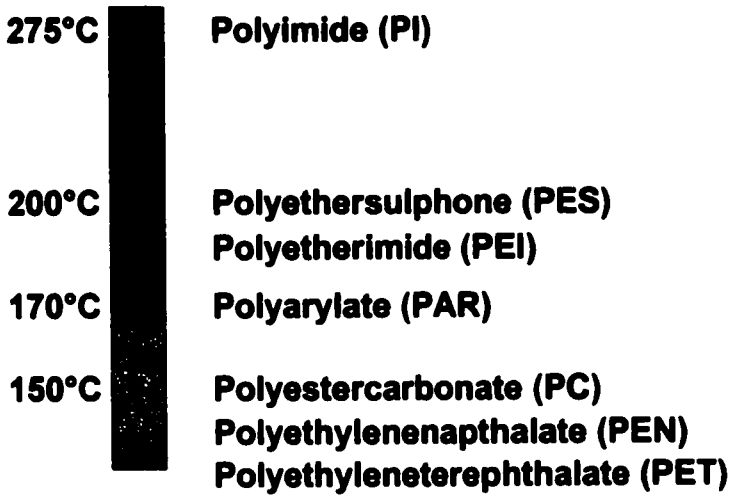

Figure 3.1. Candidate polymers for use as substrates for TFT fabrication and their respective maximum processing temperatures.

3.1.2 TFTs on Polymer Substrates: Prior Work

The development of pulsed laser processing using excimer lasers allowed the temperature limitations for crystallization to be bypassed, thus enabling the formation of poly-Si on a wide variety of substrate materials. Excimer laser crystallization (ELC) of a-Si films is a highly transient (hundreds of nanoseconds), far-from-equilibrium process that involves melting and solidification of the Si films.[5] The absorption coefficient of a-Si is $10^6 cm^{-1}$ for a XeCl laser (λ=308nm), so that a large amount of the incident XeCl excimer laser radiation is coupled into the near-surface region (~20nm) of the Si film,[6] thereby inducing high temperatures. The laser annealing process is not technically a "low-temperature" one, since melting of the Si film is an integral part of the phenomenon. But the time scale is so short that significant heating of the substrate does not occur.[7] Figure 3.2 shows a thermal simulation of temperatures achieved during laser anneal.[8] In the example, the underlying substrate is polyester. Although the temperature of the plastic is elevated to greater than 500°C, the transient nature of the pulsed laser

confines the heating to the surface, thus preventing physical damage to the substrate. The first reported use of excimer laser annealing to fabricate poly-Si TFTs demonstrated a $T_{max} = 260°C$.[9]

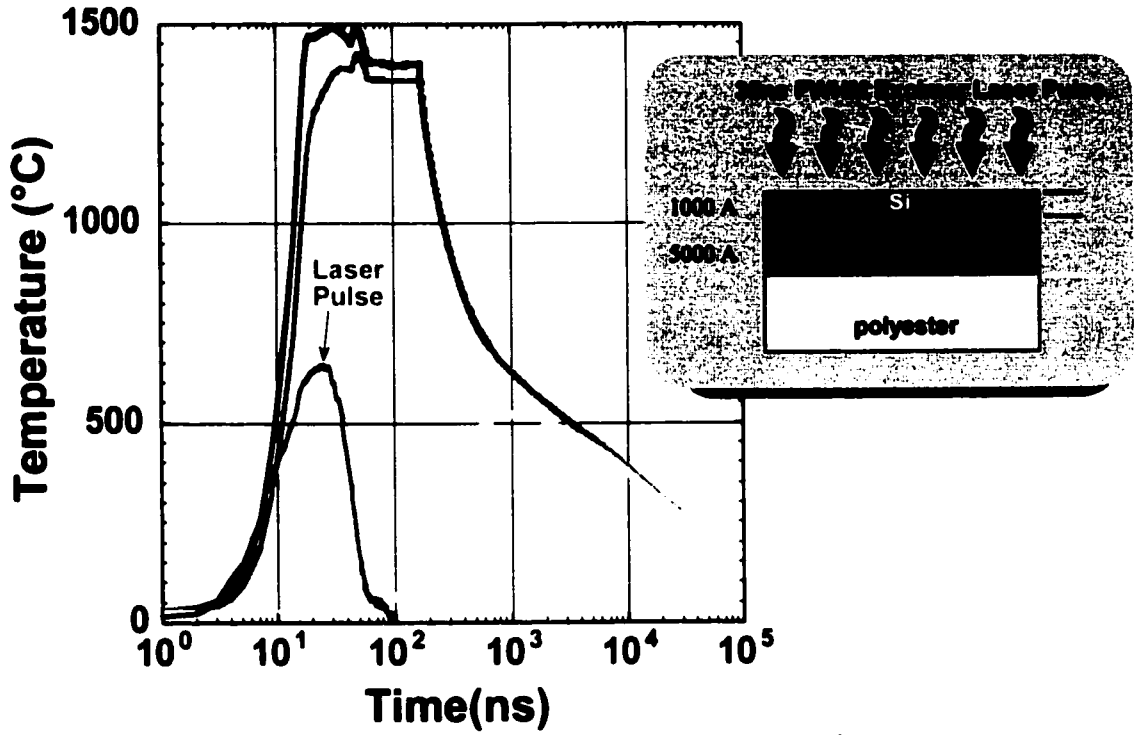

Figure 3.2. Thermal simulation of heating during laser annealing.[8] The Si film reaches its melting point and then recrystallizes, while the underlying substrate is protected by the SiO_2 buffer layer. For plastic substrates, temperatures above the T_G are reached, but the transient nature of the pulse (tens of microseconds) prevents any detrimental physical damage to the substrate.

In the past decade, the research effort to develop a viable poly-Si TFT technology on plastic substrates has increased considerably. A group at Philips Research Laboratories, Young et al., used ELC to demonstrate high-quality poly-Si TFTs on high-temperature plastics such as polyimide (PI) (T_{max}=250°C) and polyethersulphone (PES) (T_{max}=200°C).[10] For the TFTs fabricated at 250°C on PI (or glass), the group reported device results that were comparable for devices fabricated at 400°C on glass, with

effective mobilities up to 160cm^2/Vs and leakage currents down to 6x10^{-14} A/μm. (See Figure 3.3.) At 200°C on PES (or PI), the device characteristics were substantially poorer, having lower mobility (μ_{eff}=60cm^2/Vs) and higher leakage currents. The loss in performance was attributed to the 200°C gate oxide, which yielded a poorer quality interface with silicon compared with the 250°C gate oxide. The results of this work established two important points: (1) Reducing T_{max} to the point of enabling the fabrication of high-quality polycrystalline TFTs on low temperature, inexpensive plastic substrates is indeed possible, and (2) the quality of the critical gate-dielectric interface is very sensitive to process temperature, especially at temperatures below 250°C, and further research is needed to develop a high-quality gate insulator formed at ultra-low temperatures.

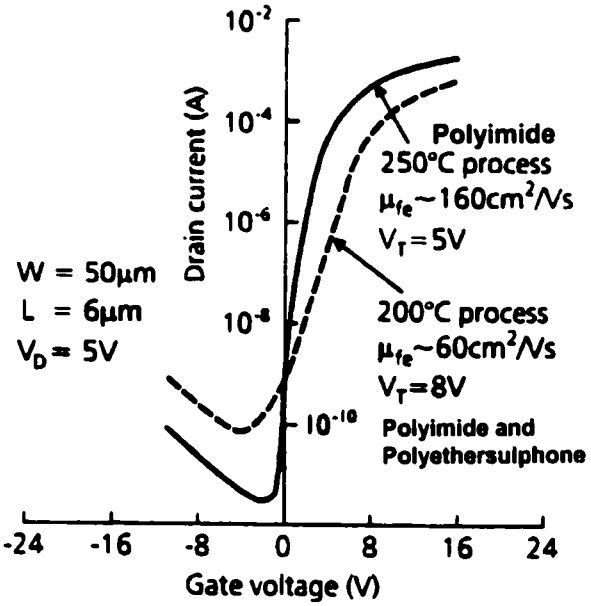

Figure 3.3. Transfer characteristics for poly-Si TFTs fabricated on polyimide (PI) and polyethersulphone (PES) from Philips Research Laboratories.[10] The results demonstrate that, at such low process temperatures, the performance difference between T_{max}=200°C and T_{max}=250°C is significant, most likely due to the quality of the SiO_2 gate dielectric.

Researchers at the Lawrence Livermore National Laboratory (LLNL) reported on poly-Si TFTs fabricated at T_{max}=100°C on polyethylene terephthalate (PET) substrates.[11] The process utilized conventional plasma-enhanced chemical vapor deposition (PECVD) for deposition of a-Si and SiO_2 films and exploited pulsed laser annealing for crystallization and doping (gas immersion laser doping, or GILD[12]). In this process, as in Young et al., careful laser crystallization was required to avoid Si film ablation because the a-Si films were high in hydrogen content (~15 atomic%), a result of deposition by PECVD, which involves the decomposition of SiH_4. (A method for low-temperature deposition of a-Si containing no hydrogen is preferred and will be introduced in the next section.) While the TFT performance was modest (μ_{eff}=7.5cm^2/Vs, V_T=8V), this work at LLNL was the first to demonstrate functional poly-Si TFTs fabricated at 100°C on plastic.

In Figure 3.1, PET sits at the bottom of the temperature scale, having a maximum use temperature of 150°C. At first glance, it may seem more sensible to select a plastic that has the highest maximum use temperature, so that higher temperatures may be used in the process to achieve better films. However, substantial problems occur when plastic is heated even slightly above room temperature. As mentioned previously, the CTE of most plastics is at best an order of magnitude larger than that of Si-based films. This difference causes large thermal expansion mismatch and leads to great thermal stresses in the deposited films. Cracking and delamination of the TFT layers can then occur. At sustained high temperatures, many plastics undergo substantial shrinkage, as well as a decrease in optical transparency and flexibility.[13] Shrinkage between lithography levels leads to misalignment of various TFT features. It is therefore best to perform TFT

fabrication at the lowest temperature possible, selecting a material that fulfills all the requirements outlined above.[1] In general, superior poly-Si TFT performance is achieved with higher temperature fabrication processes. By working at 100°C, there is the potential for achieving significantly higher performance devices by simply increasing the maximum process temperature, if necessary. Unfortunately, the cost of the plastic also increases with its T_{max}, generally speaking.

3.1.3. TFT Performance Requirements

Future information display needs will call for low-power screens, so reflective LCDs will become an important technology. Reflective liquid-crystal materials require higher drive voltages. This affects the pixel TFT in two ways: (1) the gate dielectric thickness needs to be increased, and (2) the breakdown voltage (V_{bd}) (maximum voltage that can be sustained across the source and drain terminals) must be greater than 20V, so the channel length must either increase or the source/drain doping profile must be re-engineered. As with all LC materials, the TFT leakage current must be low (<1pA/μm) for fine grayscale.

Another important emerging display technology is organic light-emitting-diodes (OLED). OLED displays have the potential to be much lower cost than LCDs and are likely easier to scale to large area displays. In addition, OLEDs are of special interest because they have been demonstrated on flexible plastic substrates.[14] In contrast to LCDs, which are voltage-driven devices, OLEDs are current-driven devices. OLED displays

[1] For example, PET is a good selection because it fulfills the desired properties for displays: it has a very high optical quality (~80% transmission); it is very low cost and widely available, and it has a relatively low CTE ($18x10^{-6}$ $°C^{-1}$); also, it holds up to standard wet chemical etches and maintains its integrity under laser processing.

usually require a two-transistor pixel: one acts as a current source (to drive the OLED) and the other acts as a switch transistor (to transfer the voltage from the data line to the gate-electrode of the drive TFT when the pixel is addressed). The performance requirements of the switch transistor are similar to those for AMLCD pixel TFTs, but the drive TFT must provide a higher drive current. For a typical peak OLED current density of $10mA/cm^2$ and a pixel size of 10^{-3} cm^2, the drive TFT must supply up to $10\mu A$ for ~5V source-to-drain bias and ~10V source-to-gate bias. This translates to an effective mobility close to $20cm^2/Vs$.

In the following section, two processes for the ultra-low-temperature fabrication of high-performance poly-Si TFTs are described in detail (in the experimental order they were carried out). They are fundamentally the same but differ in important ways. The first process was performed at a maximum temperature of 150°C, with gate oxide formed in an ECR-source PECVD tool. Devices in this process were fabricated on single-crystal Si wafers. The second process was performed at 100°C on glass substrates, using a helicon source PECVD tool for gate oxide formation.

3.2 Fabrication Approach

Numerous challenges exist in the fabrication of high-performance poly-Si TFTs on plastic substrates. First, the gate dielectric cannot be formed by thermal oxidation (requiring T>700°C) or even LPCVD low-temperature oxide (LTO) (T>350°C). Without such techniques for oxide formation, the quality of the gate-dielectric/channel interface is crucial issue. Second, poly-Si cannot be formed by solid-phase crystallization (SPC), and therefore laser annealing is a necessity. (RTA is not fast enough to prevent damage to the

plastic). Third, conventional dopant activation by high-temperature (>600°C) furnace anneal is impossible, so a method for ensuring low sheet resistance source/drain regions is required. Again, excimer laser annealing is needed. Fourth, there is no possibility for sintering of contacts, and extra care must be taken to achieve low contact resistance. Lastly, the completed poly-Si TFTs cannot be effectively passivated[2] by typical plasma hydrogenation or any other method. For passivation to occur in poly-Si, hydrogen must diffuse into the poly-Si film and have sufficient energy to form bonds at the defect sites. The minimum required temperature is approximately 250°C, and the time required is on the order of hours. Such a process is unfortunately not compatible with plastic substrates, so TFTs fabricated on plastic may suffer from poor uniformity of performance. (On the other hand, the passivating hydrogen that leads to improved TFT performance and uniformity also is the culprit in device degradation.[15] Without hydrogenation, poly-Si TFTs on plastic may exhibit improved reliability, provided the gate dielectric is stable.)

Given these constraints and challenges, what kind of a fabrication approach can achieve the best results? In the following section, the key process steps in the ultra-low temperature TFT fabrication process are described, namely: (1) the sputtered a-Si precursor film, (2) the excimer laser annealing process, and (3) the gate oxide formation by high-density plasma PECVD.

3.2.1 Sputtered a-Si

PECVD a-Si precursor films containing large amounts of hydrogen are not well-suited for excimer laser annealing. The rapid heating of the Si during the short laser pulse

[2] For poly-Si TFTs, inter- and intra-granular defects severely affect device characteristics and degrade carrier transport. Hydrogen passivation is a well-accepted technique for trap-state density reduction, serving to not only improve overall TFT performance but also device-to-device uniformity.

can lead to catastrophic explosive evolution of the hydrogen, resulting in rough or even ablated films.[16] For such films, the laser intensity must be increased slowly in a number of pulses to the fluence required for optimum crystallization. It is preferable to use physical vapor deposition (PVD) of Si because no hydrogen is incorporated into the film, and the method does not require elevated substrate temperatures. The result is not only improved poly-Si film quality, but also a reduction in the number of requisite laser pulses by at least 30%.[16]

A-Si films were deposited for this experiment by Intevac using dc magnetron sputtering in an Ar ambient at both room temperature (RT) and at a substrate temperature of 100°C. Process conditions were not provided and are proprietary to Intevac.

3.2.2 Excimer Laser Annealing

The system used was a Lambda-Physik XeCl excimer laser (λ=308nm). To produce the laser spot used for crystallization and doping, the beam was passed through homogenizing optics that results in a "top hat" beam profile. This spot was then focused down to a 4x4mm^2 area at the surface of the sample. The beam was rastered across the sample at a repetition rate of 50Hz at a fixed energy fluence. Figure 3.4 shows a schematic of the laser annealing process.

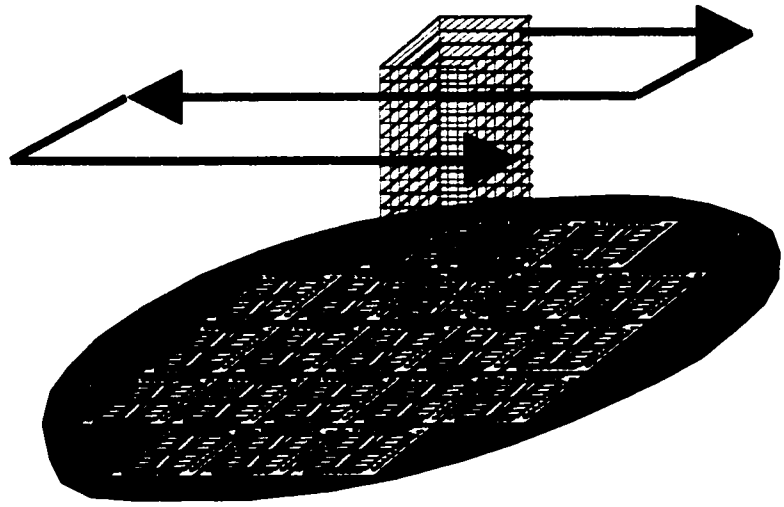

Figure 3.4. The 4x4mm^2 area excimer laser beam is rastered across the sample as shown by the arrows.

The ability to perform *in-situ* process monitoring was a feature of the system. IR and HeNe lasers were focused on the sample and detectors measured their transmission and reflectance as the laser pulse was applied. Molten Si reduces the transmission of the IR laser diode by > 80% compared to a solidified Si film. By measuring the IR diode response, the melt duration could be found and a corresponding melt depth determined. In this way, laser energy fluences could be selected to either fully melt the film (full melt threshold or FMT) for crystallization or partially melt the film for dopant activation. Typical fluences needed to fully melt films were ~270mJ/cm^2 for 50nm-thick films and ~450mJ/cm^2 for 100nm-thick films.

3.2.3 Gate Oxide Formation

The high-density plasma (HDP) PECVD systems are described in detail in Chapter 2. Specifically, electron cyclotron resonance (ECR) and helicon source plasma

systems were used for the first and second processes, respectively. These two fabrication runs are presented below.

3.3 ECR-PECVD Gate Oxide Process

The purpose of our experiment was to determine an optimum ultra-low temperature TFT fabrication process. To accomplish this, our first process (using the ECR-PECVD oxide) was designed to examine (a) channel-film deposition method and thickness and (b) gate-oxide deposition method. The second run investigated TFT performance using a helicon source PECVD gate oxide.

The substrates used are silicon and glass, respectively. Plastic substrates were not used because we wanted to determine the best possible TFT performance before addressing the difficulties inherent to flexible substrates. These difficulties include lithographic alignment problems due to plastic's larger thermal coefficient and tendency to shrink after thermal cycling, the modifying of equipment to handle flexible substrates, non-uniformity due to substrate curvature, etc. These known problems, once addressed, should not adversely affect TFT performance when plastic substrates are actually used. This same basic process was proven to be compatible with polyester as reported in previous publications [17,18].

3.3.1. Process Flow

A diagram of the TFT process flow is shown in Figure 3.5. The starting substrate is a silicon wafer with 1μm of thermal oxide. Channel films were then sputtered by dc magnetron sputtering at Intevac at two different thicknesses (500Å and 1000Å) and at

two temperatures (100°C and room temperature (RT)). LPCVD (550°C) a-Si films were also deposited for comparison. The films were laser crystallized as follows: each area was pulsed three times at energy fluences ranging from 260-275 mJ/cm^2 for 500Å films and 440-450 mJ/cm^2 for 1000Å thick films. Laser energies were targeted at slightly below FMT to obtain the largest average grain size in the film. Samples were also irradiated at fluences above FMT by 50mJ/cm^2 to achieve uniformly small grain size, again for comparison purposes. After crystallization, the device islands were patterned using standard lithography and plasma etch processes.

Next, the gate oxides were deposited using an ECR tool (at RT) and a conventional parallel-plate RF PECVD reactor (100°C). Two oxides were formed: a 1000Å pure PECVD oxide and a 200Å-ECR / 800Å-PECVD oxide composite stack. A composite stack was chosen for oxides deposited by ECR because pure ECR oxide exhibits excessive leakage at moderate gate voltage and also a lower breakdown voltage (see Chapter 2). Prior to the pure PECVD oxide deposition, an oxygen plasma treatment was used to improve the Si-SiO_2 interface.

A 3000Å-thick, sputtered Al-2%Si metal was used as the gate material. This thickness ensures its integrity during subsequent laser activation of the source/drain. Thinner Al may possibly be damaged during laser exposure. Pure Al gate metal reflects the laser energy, so the channel poly-Si is not affected. With the addition of just 2% Si, however, the energy absorption increases significantly, and we discovered that some gates melted and re-flowed, which we describe below. Following gate definition lithography, the metal was wet-etched. Self-aligned source/drain regions were formed by

ion-implantation of phosphorus dopants. Activation was subsequently accomplished with three pulses of the excimer laser at fluences of 250-280 mJ/cm^2.

Then, a 4000Å-thick PECVD isolation oxide was deposited at 100°C, and contact holes were patterned and etched into the oxide. The device was completed with subsequent deposition, patterning and etching of Al/2%Si metal to obtain contact pads for device testing. Lastly, the devices were annealed at 150°C for one hour to improve the contact resistance. This was the highest temperature step involved in the process.

3.3.2. TFT Performance

TFTs having W/L=100μm/100μm were measured,[3] and representative performance parameters are tabulated in Table 3.1. Optimum performance was achieved for TFTs with 500Å PVD sputtered channel film and 1000Å composite ECR-PECVD gate oxide. These devices exhibited an effective electron mobility of 92 cm^2/Vs and threshold voltage of 9.3V. Sheet resistance of channel films is well below 1kΩ/□. Comparison with previous results[11] indicates that PVD sputtered Si films yield superior TFT performance than films deposited by PECVD. In addition, ECR oxide exhibits a higher quality Si/SiO_2 interface than that of PECVD oxide. TFTs with the same channel film but with a pure PECVD gate oxide has mobility < 1 cm^2/Vs and threshold voltage > 20V. Since all other process steps were identical, this indicates that a higher quality, lower defect density Si-SiO_2 interface was achieved with the ECR-PECVD oxide stack.

[3] Many of the small dimension TFTs had damaged gate metals. Recall that the gate material used was Al/2%Si. The presence of Si increases laser absorption such that the small gates melted completely, re-flowed and prevented the TFTs from working properly. The use of pure Al should circumvent this problem we encountered, so that small TFTs should be indeed be realizable using a laser process.

The TFTs with the ECR gate oxide also exhibit steeper subthreshold slope, larger I_{on}/I_{off} ratio, and higher on-current than TFTs with a pure PECVD gate dielectric (Figure 3.7).

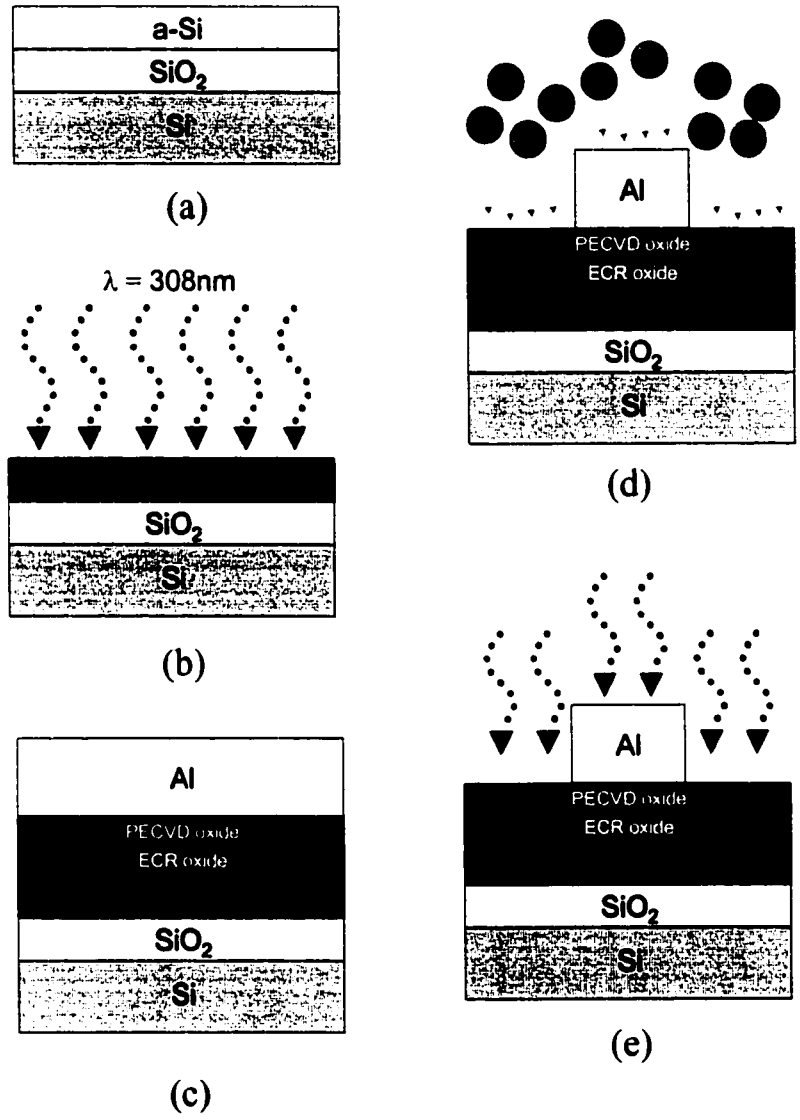

Figure 3.5. Schematic diagram of the ultra-low temperature poly-Si TFT process flow using an ECR-PECVD gate oxide. (a) The starting substrate is a thermally oxidized Si wafer with sputtered a-Si film, which is then (b) laser annealed to form poly-Si. The active area is then patterned (not shown). (c) The gate oxide consists of 200Å of ECR oxide, followed by 800Å of conventional PECVD oxide. An Al gate is sputter deposited. (d) The gate is then patterned and phosphorus ions are implanted to form self-aligned source/drain regions. (e) Dopant activation is accomplished using the laser. Not shown are the final steps of passivation oxide, contact hole formation, and contact metal deposition and patterning. Lastly, a 150°C anneal was performed for 60 minutes to lower contact resistance.

TFT process details	Mobility ($cm^2/V \cdot s$)	Subthreshold Swing (V/dec)	Threshold Voltage (V) @ I_{ds}=0.1μA	Leakage Current (pA/μm)
1000Å PVD Sputtered 100°C Si, ECR-PECVD Oxide Stack	42	2.4	7.5	6.9
1000Å PVD Sputtered 100°C Si, pure PECVD Oxide	<1	1.5	22.8	0.9
1000Å PVD Sputtered Room Temp Si, ECR-PECVD Oxide Stack	48	2.3	8.3	4.4
500Å PVD Sputtered 100°C Si, ECR-PECVD Oxide Stack	92	2.5	9.9	2.5
500Å PVD Sputtered Room Temp Si, ECR-PECVD Oxide Stack	92	2.2	9.3	5.1
500Å LPCVD 550°C Si, ECR-PECVD Oxide Stack	87	2.2	9.2	6.2
500Å LPCVD 550°C Si, pure PECVD Oxide	<1	2.5	20.1	0.1

Table 3.1. Representative TFT parameters for W/L = 100μm/100μm

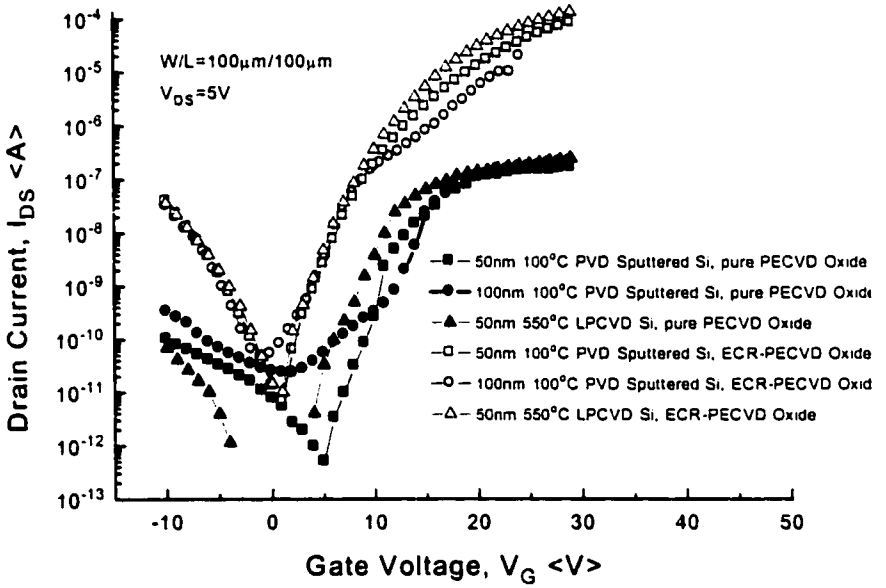

Figure 3.7. Comparison of transfer characteristics for TFTs with pure PECVD oxide and ECR-PECVD oxide stack. A superior Si/SiO_2 interface is achieved with the ECR oxide. Devices with the ECR-PECVD gate stack exhibit higher mobility, lower threshold voltage, steeper subthreshold slope, larger I_{on}/I_{off} ratio, and higher on-current than TFTs with a pure PECVD gate dielectric, irrespective of the Si deposition method.

Devices with sputtered channel films show comparable performance to those fabricated using LPCVD films (Figure 3.8). The difference in sputtering temperature between RT and 100°C has little effect on device performance. As expected, TFTs fabricated in thinner (50nm thick) films are superior to those fabricated in thicker (100nm thick) films (Figure 3.9). Mobilities for the 50nm thick channel TFTs are consistently greater by a factor of two.

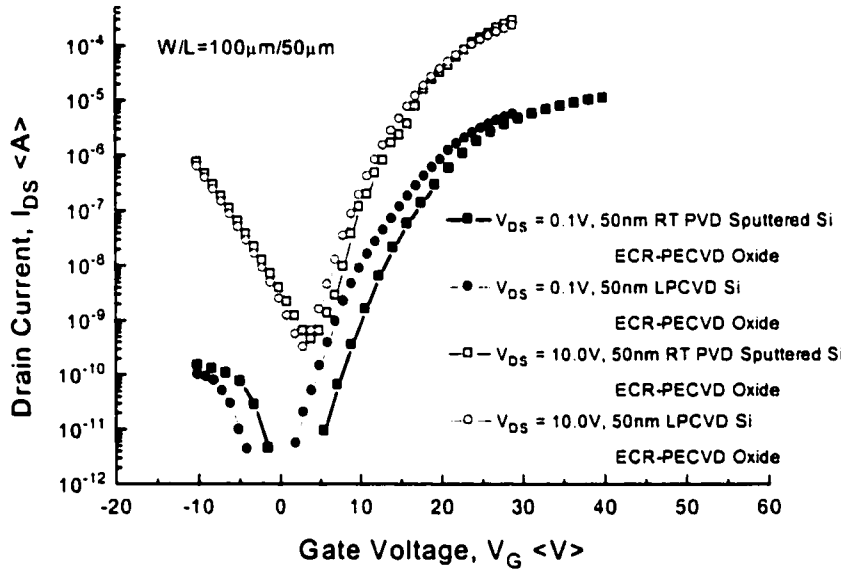

Figure 3.8. Comparison of transfer characteristics for TFTs deposited by sputtering at RT and LPCVD at 550°C. Performance is comparable. Sputtered films are lightly doped, while LPCVD films are undoped, causing the shift in curves.

Lastly, Figure 3.10 compares device performance at the two laser energies mentioned above. Crystallization of the film at full melt threshold (FMT) generally yields the largest grain sizes. However, because the number of grain boundaries within the channel varies from device to device across the wafer, a large variation in mobility is observed for same-sized devices. At laser energies above full melt threshold, grains are

uniformly small. Thus, generally lower mobilities are observed, but variation across the wafer is significantly less.

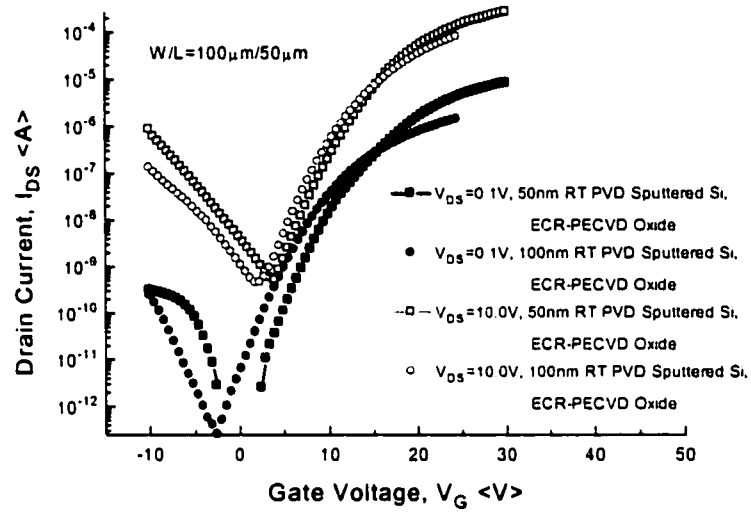

Figure 3.9. Comparison of transfer characteristics for TFTs with channel thicknesses of 50nm and 100nm. TFTs with 50nm channel film have mobility twice that of 100nm channel films.

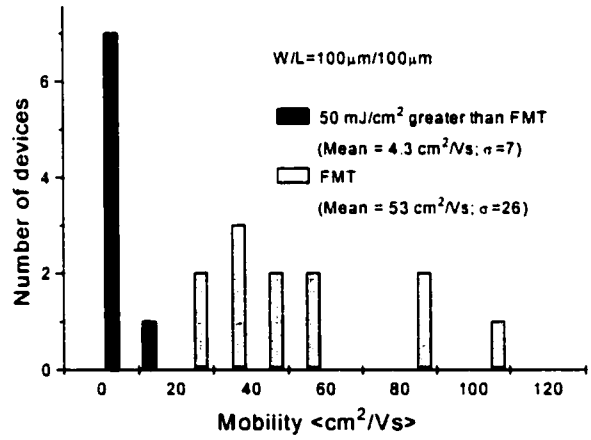

Figure 3.10. Histogram of mobilities for TFTs with 50nm-thick RT PVD sputtered Si, ECR-PECVD gate oxide. For laser energies > FMT, mobilities are low and the distribution is tight. At FMT, mobilities are higher but standard deviation is large.

3.4 Helicon Source PECVD Gate Oxide Process

3.4.1. Process Flow

Glass wafers were used as the substrate material in this run. First, a 1μm buffer layer of PECVD SiO_2 was deposited at 100°C. A 400Å-thick a-Si channel film was then deposited using physical vapor deposition (dc sputtering) at room temperature (RT). Similar to the previous process, each area was irradiated three times at laser energy fluences where near-complete melting of the film occurs (~180mJ/cm^2).

Following channel film formation, the gate oxides are formed. (The sequence of lithography steps differs from the above process: Island definition was performed after the source/drain dopant activation step to mimic the process sequence necessary for plastic substrates. We found that the laser energies required for dopant activation will damage plastic exposed to the laser pulse, so island definition cannot be performed prior to the laser activation of dopants.) A helicon source PECVD tool was used for gate oxide formation. ECR and helicon sources both generate high-density plasmas but film quality can be equipment dependent and the new helicon source was used for comparison. The gate oxide was formed in two steps: First, in the helicon chamber, a high power (700W), low-pressure (2.5mTorr), oxygen (20sccm) plasma treatment was used for several minutes to form a thin high-quality oxide layer (~40Å). Then, a conventional RF parallel-plate PECVD reactor was used to complete the gate oxide so that the total thickness was 1000Å.

Then, a 100% pure Al gate metal was sputtered to a thickness of 3000Å. (Al purity ensured high laser reflectivity during source/drain doping, in contrast to the first

run.) Following the gate lithography, the metal was etched, and the source/drain areas were cleared of oxide for doping. Source/drain formation was accomplished as follows: (1) a PH_3 plasma deposited a 5-8nm thick phosphorus-rich film (for n-channel TFTs) directly on the surface of the devices and (2) the laser was used to drive-in and activate the dopants, resulting in self-aligned, low-resistivity doped source/drain regions. (See Figure 3.6 for a diagram of this and the entire process flow.) With the last laser step finished, the device islands were patterned and etched. Next, a 4000Å PECVD passivation oxide was deposited, followed by contact hole lithography and etching. Device fabrication was completed with subsequent deposition, patterning and etching of sputtered Al contact metal. The maximum process temperature never exceeded 100°C, and no annealing or passivation (hydrogenation or otherwise) was performed after device fabrication was completed.

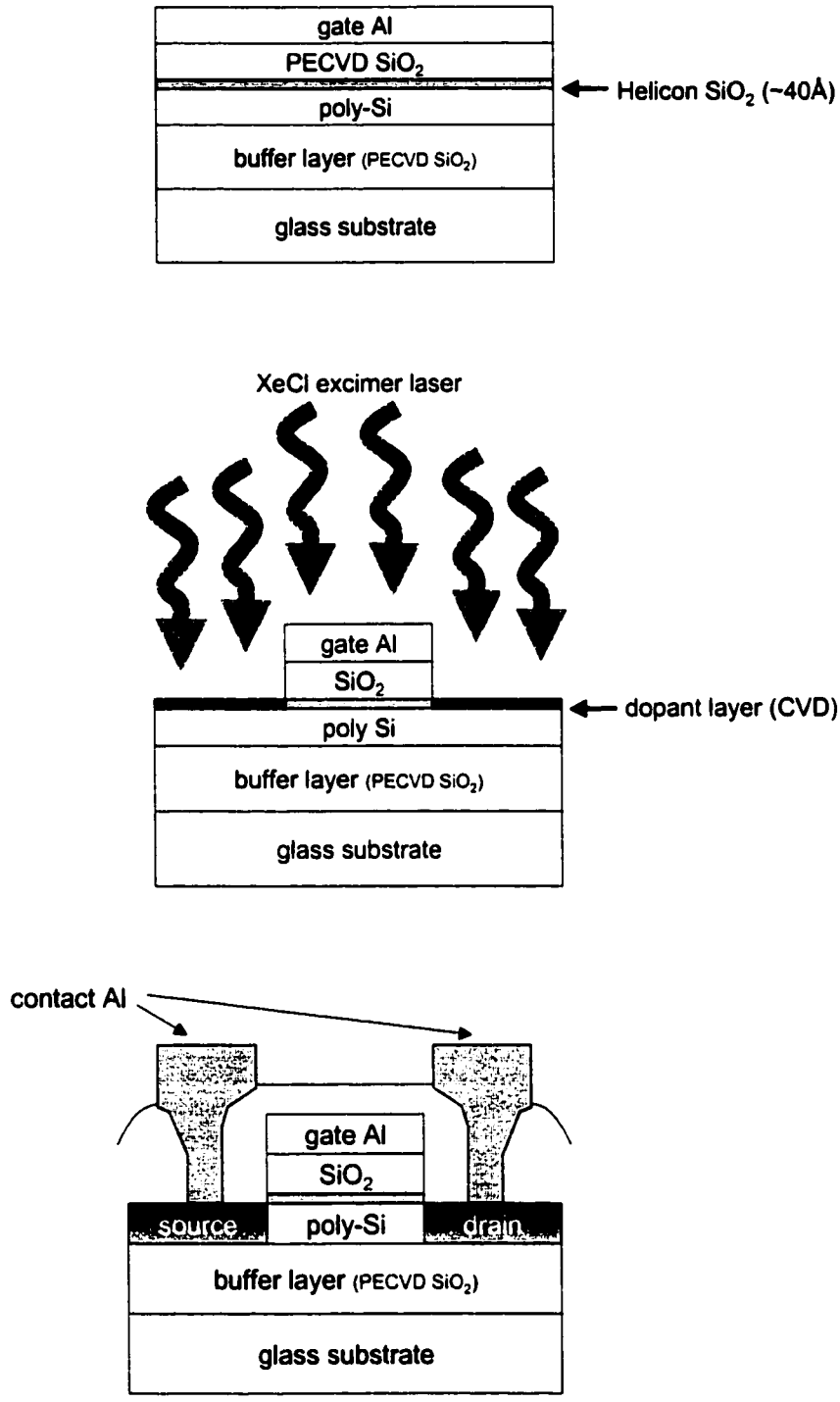

Figure 3.6. Schematic diagram of the helicon oxide process flow. The gate dielectric is deposited in two steps: (1) helicon oxygen plasma and (2) conventional PECVD. Self-aligned source and drain regions are obtained through the CVD dopant drive-in technique. Device islands are patterned after source and drain formation (not seen in diagram, but occurring between diagrams two and three). TFT fabrication is completed with a thick passivation oxide (~4000Å) and contact metal deposition.

3.4.2. TFT Performance

Fabricated TFTs have mobilities greater than 70 cm^2/Vs, drive currents of 1 mA (at V_{ds}=10Vand V_{gs}=30V), and threshold voltages around 3V. (V_T is determined by the constant current method, i.e. V_T is the gate voltage where I_d=0.1μA/(W/L) at low V_{ds}). Table 3.2 summarizes the best TFT performance parameters and Figure 3.11 shows the transfer characteristics for the completed devices. The enhanced drive current and low threshold voltage can be attributed to the improved Si-SiO_2 interface obtained as a result of the helicon plasma pre-treatment oxidation step.

Typical plasma density values for helicon source plasmas are roughly $1x10^{13}$ – $5x10^{13}$ cm^{-3}, which is about an order of magnitude higher than typical ECR plasma densities.[19,20] Helicon sources generate close to fully ionized plasmas, providing a large reactive-ion flux to the substrate to facilitate the reactions necessary to form a low-defect interface. It is interesting to compare the TFT performance results between the two runs. Figure 3.12 plots the cumulative distribution of drive currents for TFTs (W/L=100 μm/50μm) fabricated with ECR and helicon gate oxides. All TFTs having a helicon oxide interface exhibit higher drive current (measured at V_{gs}=10V). Approximately 90% of the helicon oxide devices demonstrate I_d > 1μA, while all ECR oxide devices have I_d < 1μA. We attribute the improved drive current and threshold voltage to the higher-quality Si-SiO_2 interface obtained as a result of the helicon plasma pre-treatment oxidation step. It is worthwhile to repeat that the maximum processing temperature for the helicon oxide TFTs did not exceed 100°C.

TFT Parameters	(W/L=100μm/50μm)
μ_{eff} ($cm^2/V\cdot s$)	71
S_t (V/dec)	2.5
V_T (V)	2.5
I_{min} (pA/μm)	9.3
I_{on}/I_{off}	$1.4x10^6$

Table 3.2. TFT performance parameters from the helicon source gate oxide process. V_T is calculated at a fixed normalized I_d=0.1μA/(W/L) as in [6]. (μ_{eff}, S_t, V_T are measured at V_{ds}=1.0V; I_{min} and I_{on}/I_{off} are measured at V_{ds}=10.0V)

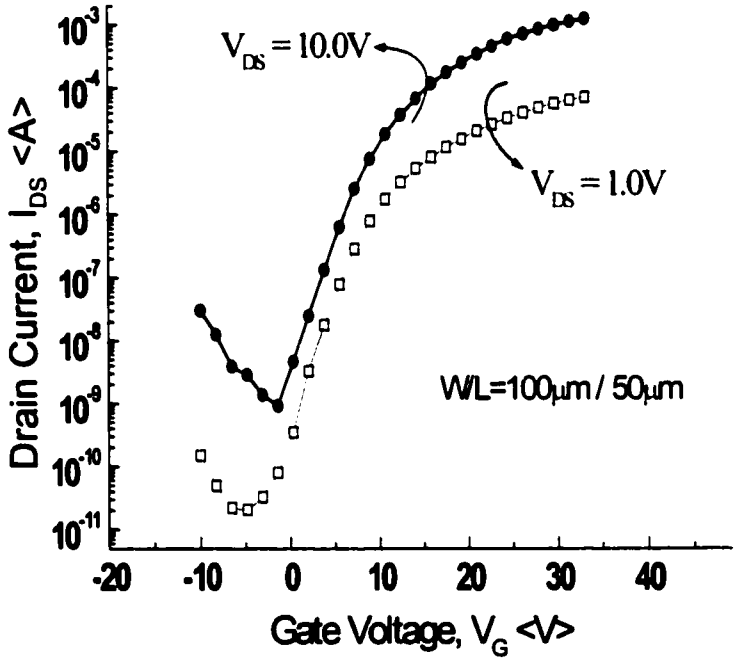

Figure 3.11. Transfer characteristics for an n-channel poly-Si TFT fabricated at a maximum process temperature of 100°C (W/L=100μm/50μm)

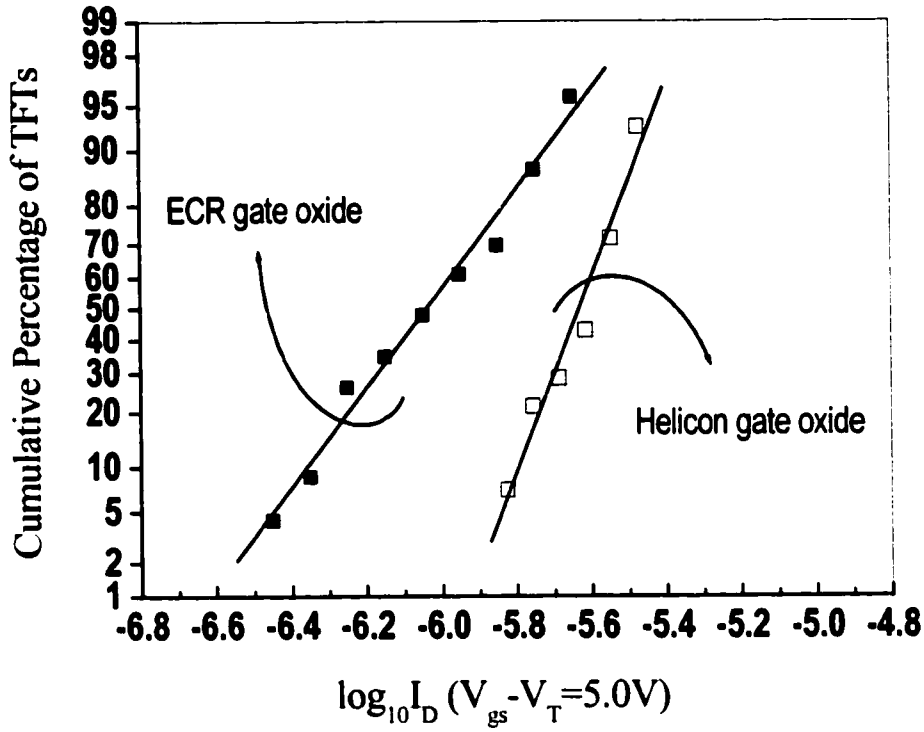

Figure 3.12. Cumulative distribution of drain current (at Vgs=10V) for TFTs fabricated with ECR- and Helicon-PECVD gate oxides. Devices fabricated with the helicon plasma oxide show consistently higher drive current. (W/L=100μm/50μm)

3.5 Conclusion

Our 100°C poly-Si TFT fabrication process introduces the use of high-density plasma for gate oxide formation to achieve a Si/SiO_2 interface superior to that of conventional PECVD oxide. High quality channel films are obtained with dc magnetron sputtering of Si and excimer laser annealing. The results of this work suggest that ultra-low temperature fabricated polysilicon TFTs can meet OLED drive requirements, particularly as luminous efficiencies improve. Hence, poly-Si TFTs on plastic substrates can be employed to achieve lightweight, high-performance, flexible and rugged flat panel displays in the future.

At the time of this work, these were the highest performance poly-Si TFTs reported for use with polyester substrates. Since our work was performed, other groups have further refined the process and demonstrated impressive results. LLNL reported results on PET (T_{MAX}=100°C) that showed high TFT drive current (0.5mA at V_{DS}=10V, W/L=100/50μm, μ_{eff}>60cm^2/Vs), but also a high V_T=18V.

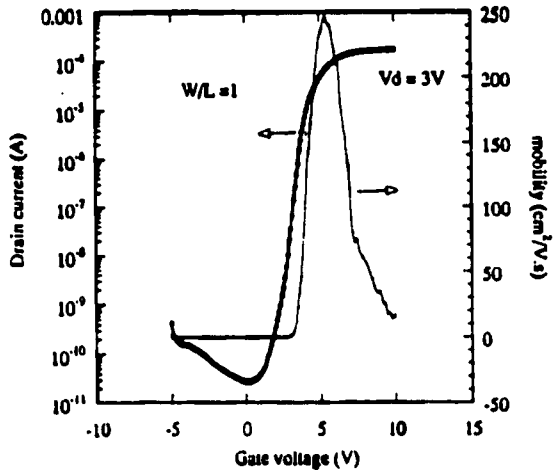

Figure 3.13. Transfer characteristics of an n-channel poly-Si TFT fabricated at a process temperature of 110°C on a PES substrate (W/L=20/20μm). (Gosain et al., *Jpn. J. Appl. Phys.*, vol. 39 (2000))

The best results reported to date come from D.P. Gosain et al. at the Yokohama Research Center of Sony Corporation.[21] Figure 3.13 shows the transfer characteristics of n-channel poly-Si TFTs fabricated at a process temperature of 110°C on a PES substrate (W/L=20/20μm). The reported mobility of the device is ~250cm^2/Vs, which approaches single-crystalline MOSFET mobilities. The work focused on large-grained poly-Si formation using a high number of laser pulses (50 per unit area). The quality of the poly-Si was attributed to the thermally insulating property of the PES substrate, which permitted a longer melt duration and presumably larger grains (compared to glass substrates, which have higher thermal conductivity). Indeed, the results here point toward

a growing interest in poly-Si TFT on plastic technology and the promise for future, high-performance flexible displays.

3.6 References

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Chapter 4

A New Method for Improving Uniformity of Poly-Si TFT Performance

4.1 Introduction

The formation of high-quality, large-grained poly-Si films is a research area of considerable interest. High-quality poly-Si has electron mobility up to 200 times greater than the currently predominant hydrogenated amorphous Si (a-Si:H) films used for TFTs in AMLCDs. TFTs fabricated using such Si films offer the promise of high-performance driver circuitry that can be monolithically integrated on the display substrate. In addition, a poly-Si TFT active-matrix will provide for lower power consumption and higher aperture ratios (for brighter displays).

In the IC industry, LPCVD poly-Si used for the MOSFET gate material is routinely deposited by LPCVD. This technique has been investigated for poly-Si TFT applications, but was found to yield fine-grained films with poor electrical properties[1] (giving an electron mobility of $5cm^2/Vs$). At present, the favored method is to form poly-Si by depositing a precursor film of a-Si and subsequently crystallizing it. With this approach, smooth, larger grained films can be obtained. The methods of crystallization can be categorized into two groups: solid-phase crystallization (SPC) and excimer-laser crystallization (ELC). The former transforms the metastable a-Si into crystalline Si through simple substrate heating, usually involving a conventional furnace anneal at 500-600°C (low-temperature SPC). Rapid thermal annealing (RTA) also falls into the SPC category, but accomplishes the same task at higher temperature in a shorter amount of time. Average grain size depends on film thickness and deposition temperature, as well as annealing time and temperature. In general, the average grain size decreases with increasing crystallization temperature, because the nucleation rate increases more rapidly with increasing temperature than the grain growth rate.[2]

The drawback of SPC is the large thermal process budget. Because SPC relies on random nucleation of grains in the a-Si films, crystallization times of several hours at temperatures of ~600°C are typically required to achieve sizable grains. The large thermal budget requirement of SPC can have a significant detrimental impact on the dimensional stability of glass substrates, so that costly high-strain-point glass substrates must be used. Moreover, the grains formed by SPC tend to be highly faulted and require lengthy plasma hydrogenation to passivate the numerous intra- and inter-granular defects in the film.

In contrast, ELC of the a-Si precursor films tends to form larger, much less faulted grains, often obviating the need for hydrogen passivation. In addition, the short-pulsed, transient nature of ELC significantly reduces the impact of the annealing process on the underlying substrate. Hence, ELC is the preferred procedure for the formation of large-grained high-quality poly-Si films. There are, however, problems associated with ELC. Poly-Si grain size is highly sensitive to laser energy fluence and therefore difficult to control. As a result, poly-Si TFT performance and uniformity are important issues for ELC.

In conventional ELC, poly-Si grain growth occurs in three distinct laser-energy-density regimes: (1) a low-energy-density regime, (2) a high-energy-density regime, and (3) the "super-lateral-growth" (SLG) regime[3]. First, in the low-energy-density regime, grain size increases only slightly with increasing energy density. Grain growth in this regime occurs via explosive crystallization followed by partial melting of the fine-grained film. Crystallization then proceeds via vertical regrowth. In the high-energy-density regime, laser energies are high enough to completely melt the Si film. Fine grain growth also occurs in this regime because the fully melted, molten film undergoes significant supercooling, followed by homogeneous nucleation. The resultant grain size is uniformly small for a wide range of fluences. The most notable regime is the SLG regime. Grain size increases sharply with laser fluence in this regime, but the range of energies for which this occurs is small. (See Figure 4.1.) The SLG regime comprises the narrow window between the low- and high-energy-density regimes. The SLG phenomenon is associated with a near-complete melting of the film, where the laser liquefies almost all of the film. However, small isolated solid-Si clusters remain at the bottom of the film,

acting as nucleation seeds for vertical and lateral grain growth. Significant grain growth can occur if the nucleation Si clusters are widely scattered, but ultimately the grain size is limited by homogeneous nucleation due to continuous cooling of the film via thermal conduction to the ambient and underlying substrate.

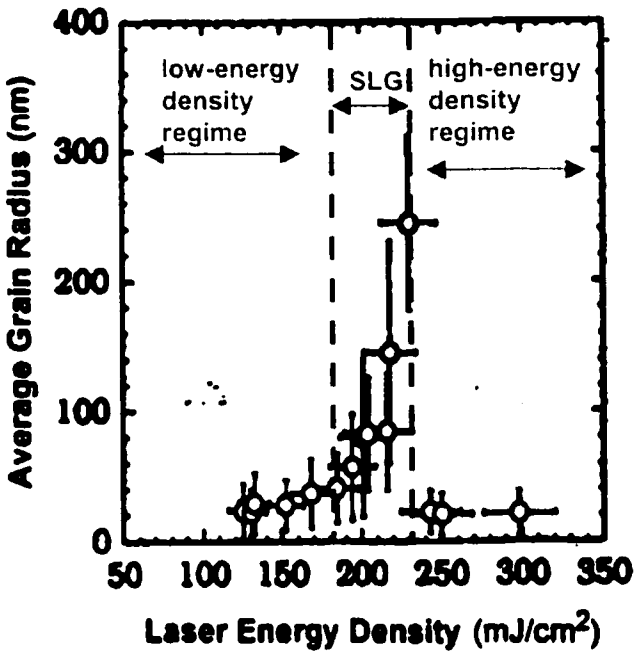

Figure 4.1. Poly-Si grain size dependence on laser energy density. The steep slope corresponds to the super lateral growth (SLG) regime, the narrow laser processing window where large grains can be achieved.[4]

It is advantageous to reduce the rate of cooling of the molten Si film, thus lessening the degree of quenching of the Si film. One method for achieving this is increasing the substrate temperature during the ELC process. Results have shown that average grain size can be roughly doubled by raising the substrate temperature (in this case, 550°C)[3]. However, substrate heating is a slow process, requiring temperature ramping and stabilization before ELC can be performed. Also, although the average grain size can be increased with this method, the window in which SLG occurs is not widened;

only the peak grain size increases. Substrate heating is not suitable for plastic substrates, since polymers can only tolerate a maximum processing temperature of 150-200°C and there is little improvement in grain size with these low temperatures. ELC on plastic substrates may have its advantages however. It has been shown that laser crystallized poly-Si on plastic substrates yields grain sizes 2 to 3 times larger compared to poly-Si on SiO_2.[5] The reason for this improvement was attributed to the lower thermal conductivity of the plastic (one tenth that of SiO_2) that leads to a longer heating time during ELC. Other options to reduce heat conduction into the substrate have been investigated, such as using a thicker SiO_2 layer that tends to isolate the thermal mass of the thin film.[6] Tradeoffs exist between adding process complexity and gaining improvement in poly-Si film quality.

The narrow processing window associated with ELC hampers the feasibility of wide-scale production of poly-Si TFTs. Although ELC techniques have produced relatively large grains of crystallized silicon by exploiting the SLG phenomenon, variation in the location of these grains results in large statistical variations in the electrical performance of TFTs fabricated using such material. For a poly-Si TFT manufacturing process to be viable, it must simultaneously minimize the number of grain boundaries in the active area (to improve performance), minimize the statistical fluctuation in grain number (to improve uniformity), and widen the ELC processing window.

The work here seeks to exploit the SLG phenomenon in a more reproducible manner and demonstrate improved device performance. A number of investigations have reported on methods to control poly-Si grain structure using ELC.[7,8,9] High-quality,

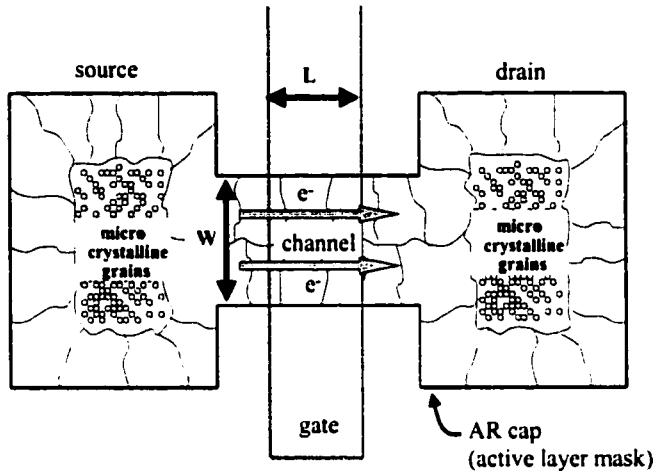

Figure 4.2. Top view sketch of a TFT illustrating typical grain structure achieved using the AR cap approach. (The channel length L and width W are indicated.) In the channel region, SLG occurs until the grains meet in the center and form one continuous grain boundary parallel to the direction of current flow. In the larger source/drain regions, a microcrystalline area is present due to homogeneous nucleation. The upper limit for grain growth under the AR cap was found to be ~1μm.

single-crystal Si can be achieved using sequential lateral solidification[7], but the method requires complex laser stepper systems and impractically long process times. TFTs fabricated using a patterned Al cap method to control channel grain structure were shown to have good performance,[8] but the process requires an additional lithography step and the source/drain regions are not self-aligned to the gate electrode. However, one technique appears to be most promising for incorporation into a typical poly-Si TFT fabrication process. A patterned 50nm-thick SiO_2 capping layer on top of Si films can be used as an anti-reflective (AR) coating to induce more laser energy coupling into the Si beneath the cap than in the surrounding, uncapped Si film.[9] With this AR cap approach, it was found that the laser-processing window for achieving large-grained poly-Si is widened significantly beyond the narrow SLG regime.[10] Our process technique is simple and reproducible: It requires only one laser pulse, no additional lithography steps, and it

simultaneously self-aligns the large grains to the TFT channel region by using the active island mask to define the AR cap. Figure 4.2 shows a top view sketch of the typical grain structure obtained for a TFT using this approach.

4.2 Process Flow

To demonstrate the viability of the AR cap approach, poly-Si TFTs were fabricated. Figure 4.3 shows a schematic diagram of the process flow. The starting substrates for these devices were quartz substrates coated with a 1μm-thick LPCVD buffer oxide. The process was performed as follows: 50nm and 100nm thick LPCVD a-Si films were deposited at 550°C using Si_2H_6 gas at 300mTorr. Next, an anti-reflective (AR) layer consisting of 50nm of low-temperature-oxide (LTO) was deposited by LPCVD at 450°C. Patterning of the AR layer was done using the active Si island mask. Next, the films were crystallized using a large-area (27mm × 68mm), pulsed (50ns), 308nm XeCl excimer laser at SOPRA of France. For the 50nm-thick Si films, laser energy fluences of 375, 400, 425, 450 and 475mJ/cm^2 were used. For 100nm films, the fluences used were 350, 375, 400, 450 and 475mJ/cm^2. In all cases, only one pulse was used to crystallize the film. Table 4.1 summarizes the experimental splits. Conventional TFTs without the AR cap having identical splits were also fabricated for comparison.

Following laser exposure, the poly-Si was patterned using the AR oxide cap as a hard mask for dry etching. The oxide cap layer was then stripped, and a blanket 50nm LTO gate dielectric was deposited. Next, a 200nm-thick poly-Si film was deposited by LPCVD and patterned to form gate electrodes. Gate doping and source/drain formation was achieved by implantation of phosphorus ($5x10^{15}cm^{-2}$, 60keV) or boron ($5x10^{15}cm^{-2}$,

20keV) ions and subsequent 15-hr. 600°C activation anneal. An isolation oxide was then deposited by ECR-PECVD to a thickness of 500nm. Contact holes were patterned and etched. After that, a metal layer consisting of a Ti/TiN/Al stack was deposited and patterned. Finally, a 400°C sinter was performed to ensure low contact resistance, but no hydrogenation or other method of defect passivation was performed. For comparison purposes, conventional TFTs were also fabricated without the AR cap technique, but otherwise using the identical process.

Sample number	Poly-Si thickness	Laser fluence (mJ/cm^2)	Comments
1	50 nm	375	
2	50 nm	400	
3	50 nm	425	
4	50 nm	450	AR cap was **ablated**
5	50 nm	475	AR cap was **ablated**
6	100 nm	350	
7	100 nm	375	
8	100 nm	400	
9	100 nm	450	AR cap was **damaged**
10	100 nm	475	AR cap was **ablated**

Table 4.1. Summary of experimental splits for laser annealing energies.

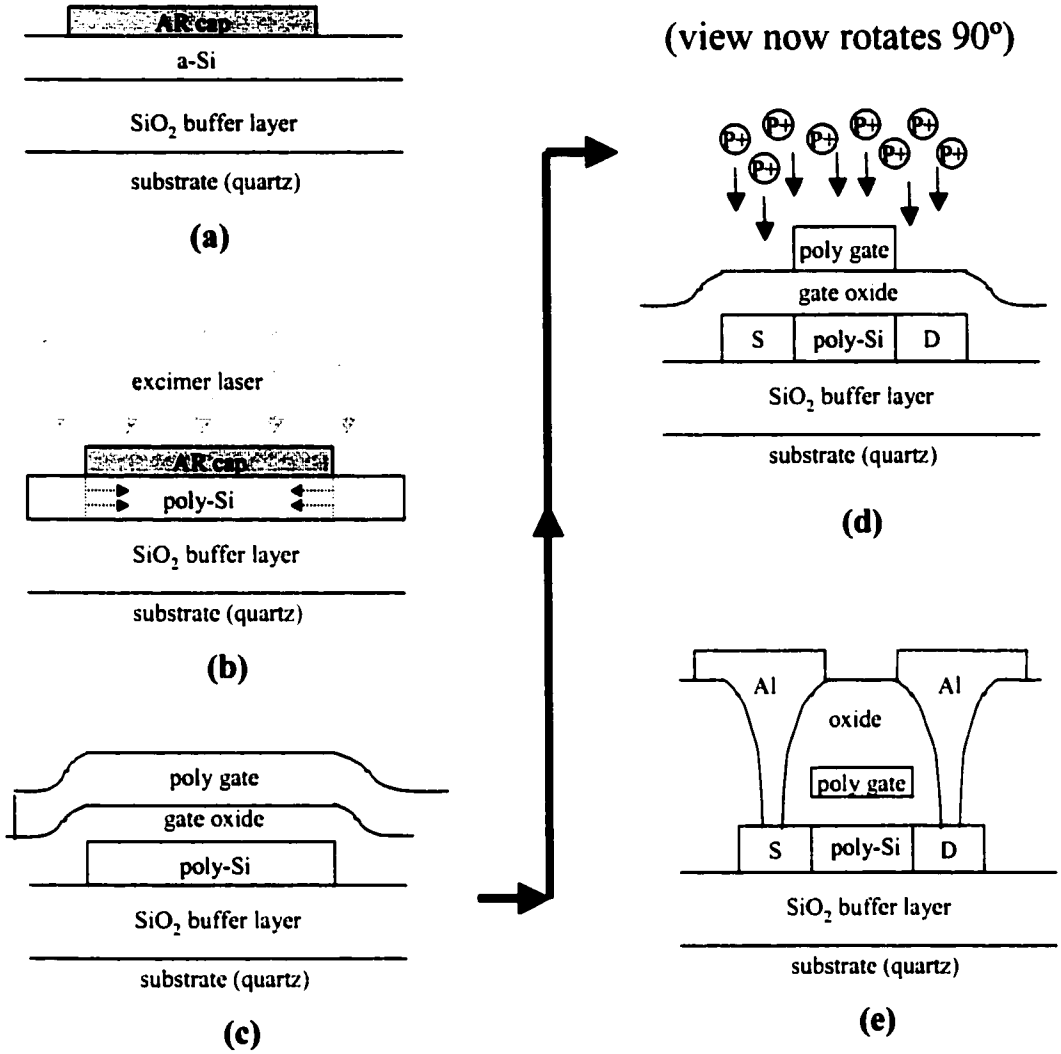

Figure 4.3. TFT process flow diagram. (a) (*view is looking down the channel in the direction of current flow*) A 50nm AR oxide layer is deposited and patterned on top of LPCVD a-Si. (b) A XeCl 308nm excimer laser crystallizes the Si film to form poly-Si. Large grains are formed beneath the AR cap; horizontal arrows indicate the direction of grain growth. (c) After laser annealing, the AR cap is used as a hardmask to define the Si active area. The AR layer is then stripped and a blanket gate oxide is deposited. A poly-Si gate is deposited and patterned. (d) (*view is rotated 90° now, a conventional view looking perpendicular to the channel*) Ion implantation and a subsequent 600°C anneal is used for gate doping and source/drain formation. (e) An isolation oxide is deposited, contact holes etched, and contact metal deposited and patterned. A final 400°C sinter is performed to lower contact resistance. No hydrogenation or other passivation was performed.

4.3 TFT Performance

As illustrated in Figure 4.2, poly-Si grains in the channel grow from the edge of the oxide cap to meet in the middle of the channel. However, if the cap has a large width such that enough time elapses for spontaneous nucleation to occur in the middle of the capped region, fine grains will dominate the microstructure there. Indeed, the upper limit for inward SLG-regime grain growth was found to be ~1μm.[10] It is therefore expected that TFTs with W ≤2μm will have no microcrystalline region whatsoever and thus exhibit better performance. To illustrate the impact of this phenomenon on device performance, TFTs with five separate, parallel channels were fabricated. Each channel in the five-channel device has a width of 2μm giving an effective total W=10μm. Figure 4.4 compares the output characteristics for the five-channel TFT vs. a conventional single-channel TFT, both having W/L=10/5μm. The drive current of the five-channel TFT is larger because there is no small-grained, high-defect region in the channel. This increase in drive current is observed at all three laser energy densities. Five-channel TFTs showed drive current enhancements over single-channel TFTs by factors of 3.0, 2.4 and 2.3 (at V_{gs}=20V, V_{ds}=15V) for laser fluences of 375, 400, and 425mJ/cm^2 respectively.

Similar improvement is seen for five-channel p-channel TFTs. Figure 4.5 shows the output characteristics for p-channel TFTs, comparing five- vs. single-channel devices. Again, the drive current improvement occurs at all three laser energy densities. P-channel five-channel devices showed drive current enhancement by factors of 3.0, 4.3 and 2.9 (at V_{gs}=-20V, V_{ds}=-15V) for laser fluences of 375, 400, and 425mJ/cm^2 respectively.

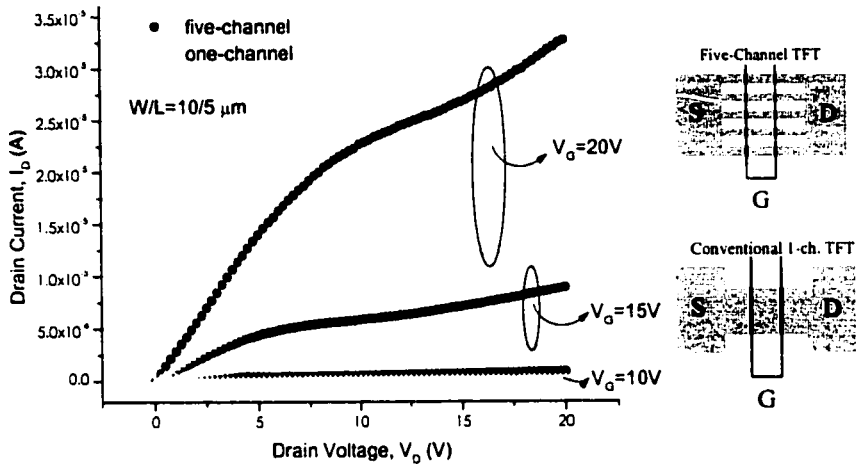

Figure 4.4. Output characteristics for 5- and 1-channel AR-capped n-channel TFTs with $W_{eff}/L=10/5\mu m$ and $T_{Si}=50nm$, annealed at a laser fluence of 425mJ/cm^2. (Schematics of the two TFT structures are shown at right.) Five-channel TFTs ($W=5\times2\mu m$, $L=2\mu m$) have higher drive currents than conventional TFTs of $W/L=10/5\mu m$. The narrower channel region has SLG-regime grains that meet in the center of the capped region. When the cap width exceeds 2μm, homogeneous nucleation occurs in the center of the capped region during laser annealing, leading to a microcrystalline grain structure and consequently poorer TFT performance.

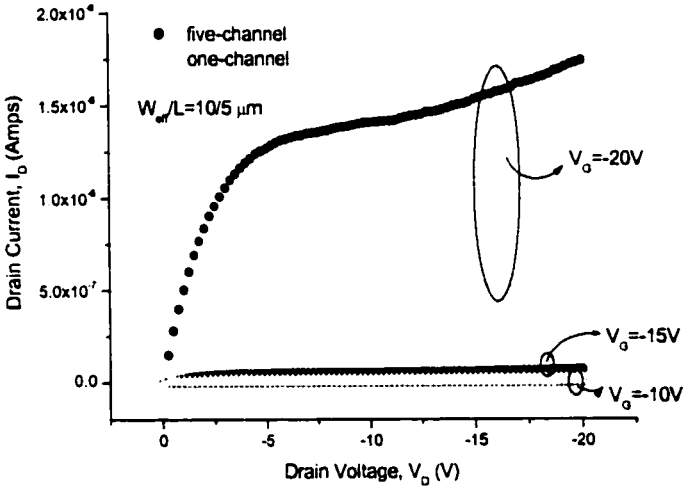

Figure 4.5. Output characteristics for 5- and 1-channel AR-capped p-channel TFTs with $W_{eff}/L=10/5\mu m$ and $T_{Si}=50nm$, annealed at a laser fluence of 425mJ/cm^2. These devices have the same structure as the devices sketched in Figure 4.4. Like the n-channel TFTs, the p-channel five-channel devices show improved drive current over the conventional single-channel TFT.

Figure 4.6(a) compares average on-currents (I_{ON}, measured at V_{ds}=-10V, V_{gs}=-25V) for capped and uncapped p-channel TFTs (W=2μm and L=1,2,3,4μm) crystallized at various laser fluences. The laser energies used for the capped TFTs were 375, 400, and 425mJ/cm^2. (Beyond 425mJ/cm^2, the oxide cap layer was ablated, and the surface of the underlying poly-Si film was too rough to yield working devices.) For uncapped devices, the range was 375-475mJ/cm^2. At its upper end, this range of fluences includes the SLG regime where large-grained poly-Si forms. As a result, the average on-currents shown in Figure 4.6(a) are higher for the uncapped TFTs. Some uncapped devices may not contain any grain boundaries in the channel region. However, the uniformity of performance is poor. I_{ON} should be directly proportional to W/L, and this is seen for capped TFTs but not for uncapped TFTs. Because grain growth can be easily controlled using the capping method, performance is uniform even for small-dimensioned TFTs. In Figure 4.6(b), the standard deviation (σ) of I_{ON} is plotted for the same devices. For all channel lengths, σ is greater for uncapped TFTs, indicating poor uniformity of channel film grain structure. Figure 4.7 shows the average leakage currents (I_{OFF}, measured at V_{ds}=-10V and V_{gs}<5V) for the same p-channel TFTs. Average leakage current is larger for uncapped TFTs, and Figure 4.7(b) shows that the I_{OFF} standard deviation varies significantly for uncapped devices while remaining constant for capped TFTs.

The laser fluence ranges in which the three poly-Si grain growth regimes exist are highly dependent on the method of a-Si film deposition and thickness. In this experiment, it was necessary to pre-specify a range of energies to SOPRA, which required us to predict in advance the proper window of laser fluences. Our goal was to select a window of energies that would be bounded at the upper limit by the full melt threshold, and at the

lower limit, the laser energy at which the AR cap provides no advantage. For our samples, full melting of the film (SLG regime) occurred near 450 – 475 mJ/cm^2 for the uncapped film.[4] Thus, the range of selected laser energies included the upper limit of the AR capping layer's working window. However, improvement in AR capped TFT performance is still seen at the lowest laser energy (375mJ/cm^2), as seen above. But the lower limit of the patterned capping method's effectiveness is uncertain. At the least, there is a 50mJ/cm^2-wide (375-425mJ/cm^2) processing window using the patterned AR cap. Our results indicate that the window of acceptable laser energies for large-grained, high-performance poly-Si TFTs will extend below this experiment's lower bound of 375mJ/cm^2.

Uncapped n-channel TFTs exhibited higher source/drain series resistance than the uncapped p-channel devices. All steps in the process were identical except for the dopant type (phosphorus for n-channel, and boron for p-channel), so the difference is likely due to a change in grain structure as a result of the ion implantation. Prior to ion implantation, the average grain size of the uncapped films in the source/drain regions is smaller than for the capped devices. As a result, the implant step results in more completely amorphized source/drain regions for the uncapped films. Boron has less mass than phosphorus, so the p-channel implant likely did not amorphize the p-channel source/drain regions to the same extent. The activation anneal step was identical for both n- and p-channel TFTs, so it is possible that the anneal was adequate to re-crystallize the boron-implanted regions but not the phosphorus-implanted regions, leading to increased series/contact resistance for n-channel TFTs.

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[4] Use of *in-situ* HeNe laser reflectance allowed the melt duration to be measured, and the corresponding melt depth was calculated. In this way, the full melt threshold laser energy was found.

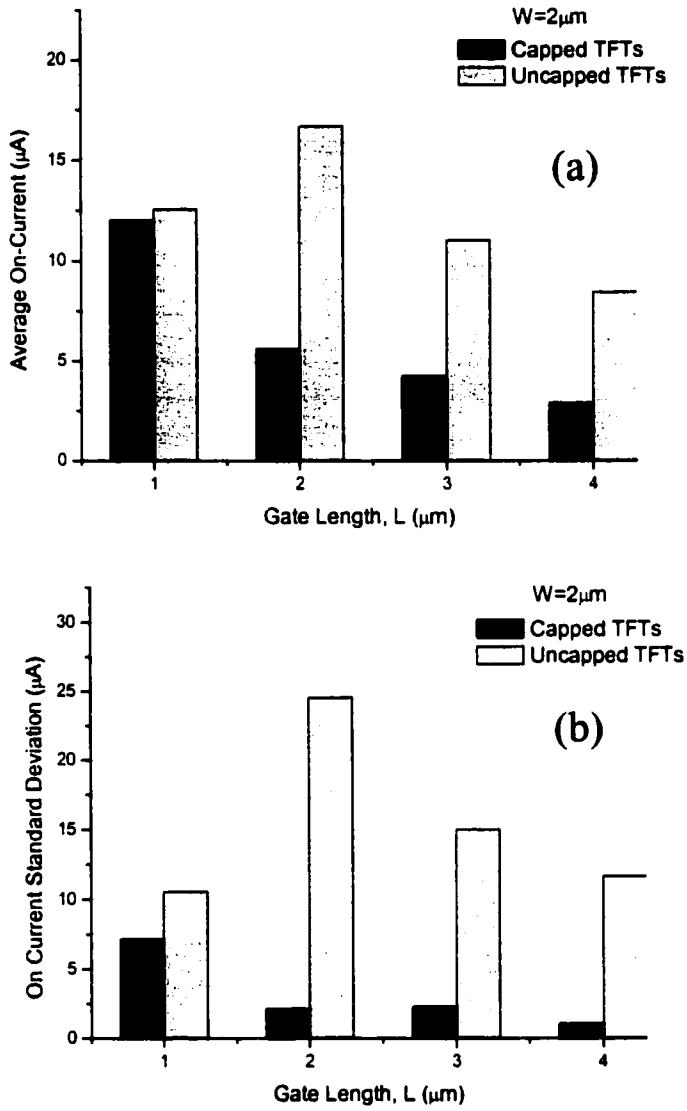

Figure 4.6. (a) Average I_{ON} for capped and uncapped p-channel TFTs (W=2μm). Eight devices for each channel length were measured. Capped devices were crystallized at laser fluences of 375-425mJ/cm^2. Beyond 425mJ/cm^2, the oxide cap was ablated, and the poly-Si surface was too rough to obtain working TFTs. Uncapped devices were annealed at laser fluences of 375-475mJ/cm^2. This range spans the SLG regime, so channel films formed in this regime yielded uncapped TFTs with large average grain sizes and thus higher average I_{ON}. However, uniformity of TFT performance is poor. The average I_{ON} for capped TFTs decreases with increasing channel length as expected, while the uncapped TFT average I_{ON} is not a strong function of channel length, indicating non-uniformity in channel film grain structure. (b) Standard deviation of I_{ON}. Capped TFTs have smaller σ for all channel lengths.

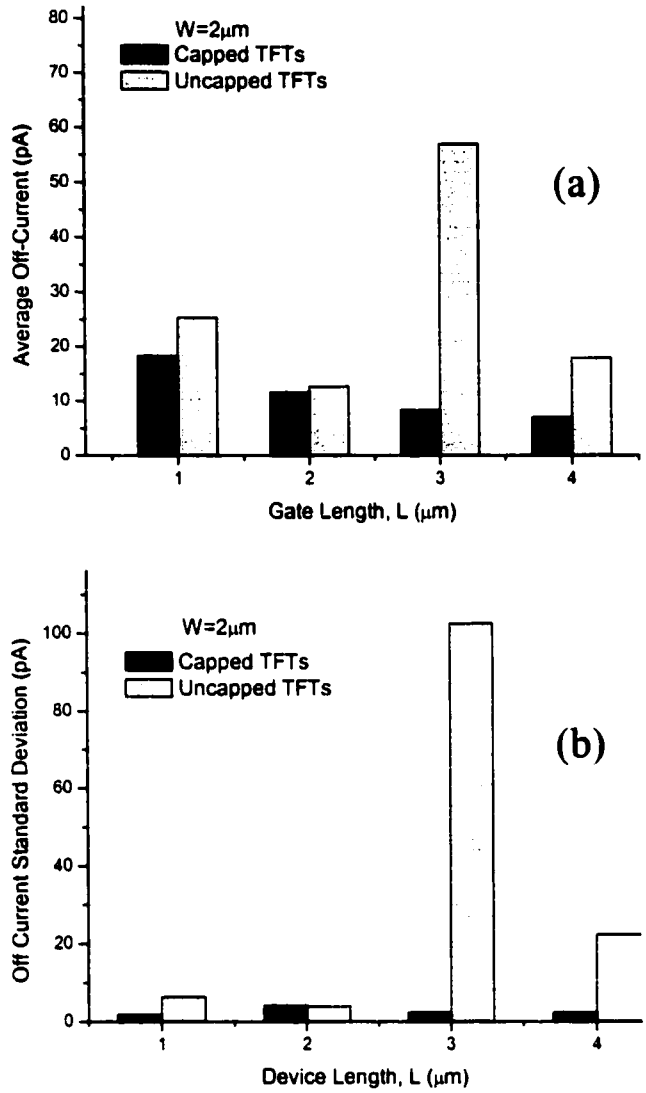

Figure 4.7. (a) Average I_{OFF} for capped and uncapped p-channel TFTs (W=2μm). (b) Standard deviation (σ) of I_{ON}. Capped TFTs have smaller I_{OFF} and σ for all channel lengths.

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Chapter 5

Design of a Poly-Si TFT Active-Matrix Organic Light-Emitting Diode Display Prototype

5.1 Introduction

Electroluminescence in organic materials was first observed in 1963 by Pope et al.[1], but interest in organic light-emitting diodes (OLEDs) did not grow significantly until a high efficiency device was demonstrated by Tang in 1987.[2] Since then, flat panel display technology development based on organic light-emitting diodes (OLED) has been accelerating rapidly. Figure 5.1 shows the growth and market forecast for OLEDs for different applications.

OLEDs have many attributes that are very attractive for use in information displays: (a) wide viewing angles (Lambertian emission), (b) fast response (typically

microseconds) for video applications, (c) thin, compact *solid-state* films for mobile applications, (d) low drive voltage (<10V) for low power consumption, (e) high brightness (up to 10^5 cd/m^2) and contrast ratio (>100:1), (f) full color tuning capability, (g) easy grayscale since luminance is linear with current density, and (h) low temperature processing compatible with plastic substrates, presenting the opportunity for flexible displays. However, substantial research is still needed before these potential qualities can be fully realized in displays.

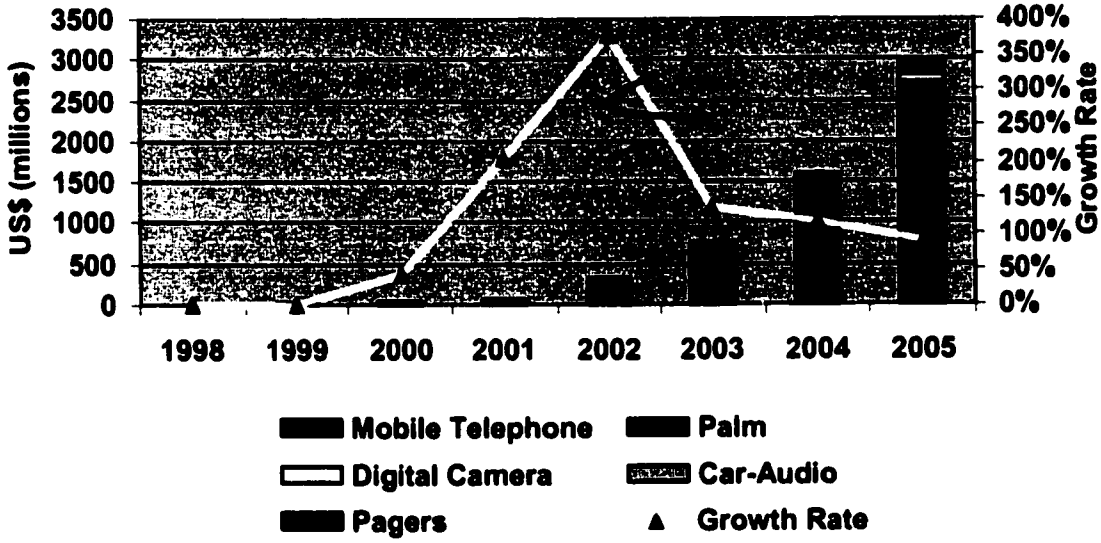

Figure 5.1. OLED forecast for various electronic devices. Also, the growth rate of OLEDs is projected. *(source: Display Search, 2000)*

A typical multi-layer OLED structure is shown in Figure 5.2.[5] The cathode is typically opaque, so light is emitted through the bottom of the structure (through the transparent substrate), which employs indium tin oxide (ITO), a transparent conductor for

[5] In this chapter, we consider only small molecule OLEDs. Another type of organic LED exists: polymer based organic LEDs, which are often referred to as PLEDs.

the anode. The hole transport layer (HTL), emissive layer, and electron transport layer (ETL) are the organic materials, whose composition and thickness are optimized for color and luminance. The top electrode is usually a thin, reflective low workfunction metal. The total thickness of the completed device is usually no more than 0.5μm.

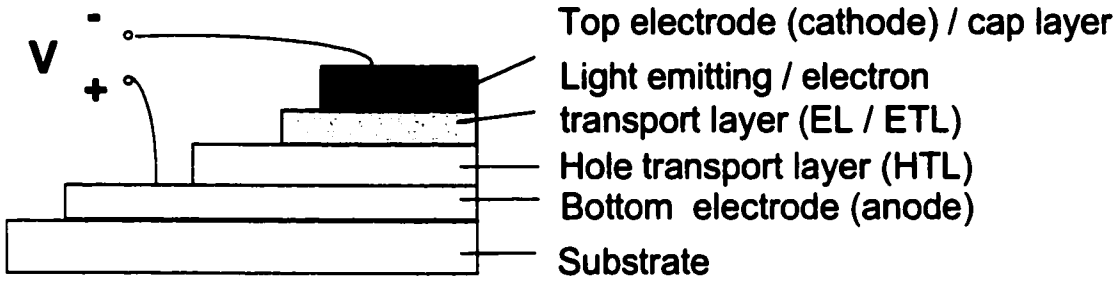

Figure 5.2. Schematic diagram of the layered OLED structure.

Although the OLED structure is relatively simple, several hurdles exist on the road to achieving a high-resolution, full-color organic display. To start, there are processing challenges. Precise control during deposition is required to ensure accurate composition of the organic material, which directly affects the OLED color and efficiency. Another difficulty that occurs in OLED fabrication is patterning. Conventional photolithography is not feasible, because photoresist attacks the organic materials. Patterning is accomplished by using a shadow mask during deposition, so challenges will arise for fine pixel definition in high-resolution displays. After the OLED is made, the device must be hermetically sealed to prevent detrimental reactions with air and moisture. Independent of encapsulation, OLED lifetime for all colors (red, green and blue) must be greater than 10,000 hours to be useful for a variety of display applications. Currently, red OLEDs have the longest lifetime, followed by green, then blue.[3] This differential aging can lead to non-trivial problems in image appearance over time. Also, OLEDs are

current-driven devices, not voltage-driven like LC cells, so new driver electronics and pixel circuitry must be designed.

Passive-matrix OLEDs suffer several problems. As display size increases, the long column and row lines will require very low resistance interconnects to avoid voltage drops across the display. A more serious problem is that OLED lifetime in passive-matrix displays is very short. The simple, multiplexed addressing scheme sequentially delivers a short, high-current pulse to momentarily operate the OLEDs at high brightness (as much as 100 times the perceived luminance) one row at a time, and the eye integrates the light over the entire frame time. But unfortunately, OLED efficiency and lifetime are much worse when operating at high currents. The solution is to use active-matrix addressing, so that the OLED can operate in constant-current mode with lower peak brightness.

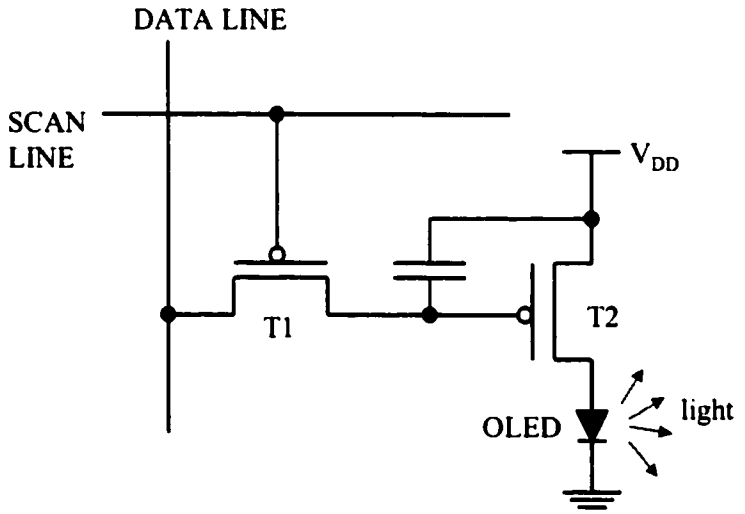

Figure 5.3. Simple 2T OLED pixel circuit. T1 acts as a voltage switch, and T2 is a current source to drive the OLED.

The simplest pixel structure for AMOLEDs requires two transistors: one acts as a voltage switch, similar to TFT operation in AMLCDs, while the second acts as a current source to drive the OLED. Figure 5.3 depicts a schematic of the pixel circuitry.

Addressing is accomplished by switching the scan line, such that T1 passes the data line signal to the gate of T2. The storage capacitor holds the T2 gate at a constant voltage for the entire frame time, so the OLED operates in constant current mode. This active-matrix scheme has a number of advantages. First, as mentioned above, full duty cycle operation is possible, so OLED lifetime and efficiency will be improved, leading to lower power consumption. Second, a common cathode can be used, eliminating the need for fine patterning of top cathode lines. The blanket cathode has the added benefit of enhancing the protection of the active organic layers. Third, current control is easier so that grayscale can be controlled more accurately.

In implementing the AMOLED display, poly-Si TFTs are preferred. The OLED structure generally has the transparent ITO anode deposited first, because reliability problems result when ITO is deposited onto the organic material. Thus, the drive TFT is connected to the anode. For the drive current to be well controlled, the TFT source voltage should be fixed. Thus, a high-current-drive p-channel TFT is required, which is practical only with poly-Si. Also, the higher current drive of poly-Si TFTs allows for smaller devices and consequently a higher pixel aperture ratio for higher display brightness. Finally, high-performance poly-Si TFTs offer the capability to monolithically integrate the driver circuitry on the display substrate. Schemes do exist for the use of n-channel a-Si TFTs, but lower transistor performance translates into higher power consumption, lower aperture ratio, and a dependence on off-chip drivers.

Thus, the development of a poly-Si TFT active-matrix backplane for an OLED display would be an important step toward the replacement of a-Si TFT AMLCDs.

5.2 Display Prototype Specifications

A prototype poly-Si TFT AMOLED was designed in collaboration with Universal Display Corporation. The display contains 128x64 pixels at 80 dots per inch (dpi). Each pixel contains two transistors in a circuit identical to the one drawn in Figure 5.3. Device sizes are as follows: T1 has W/L=4/4μm, T2 has W/L=40/4μm. The maximum leakage current specification is 10pA. To meet this requirement, T1 was given a double-gate structure (see Figure 5.4). By employing two gates, the peak electric field in the channel is lowered, so that the dominant mechanisms of leakage current (i.e. trap-assisted tunneling and thermionic emission) are significantly reduced. The drive TFT was oversized to ensure that an adequate drive current is provided to the OLED. The W/L ratio of ten is more than sufficient, assuming a mobility $\geq 30 cm^2/Vs$ for a supply voltage of 8V and an OLED current density of $10 mA/cm^2$. The capacitance of the storage capacitor was set at 1.5pF, so that the gate voltage of the drive TFT will not fall by more than 0.1V over the refresh time, assuming a leakage current through the switch TFT of 10pA and a frame rate of 60Hz.

Figures 5.5 and 5.6 shows the pixel layout and the stitching of the pixels to form the array. Included on the substrate are TFT test devices, contact and sheet resistance measurement structures, large OLED pixels, electro-static discharge (ESD) protection rings, and large contact pads to the scan and data lines for off-chip TAB driver circuits.

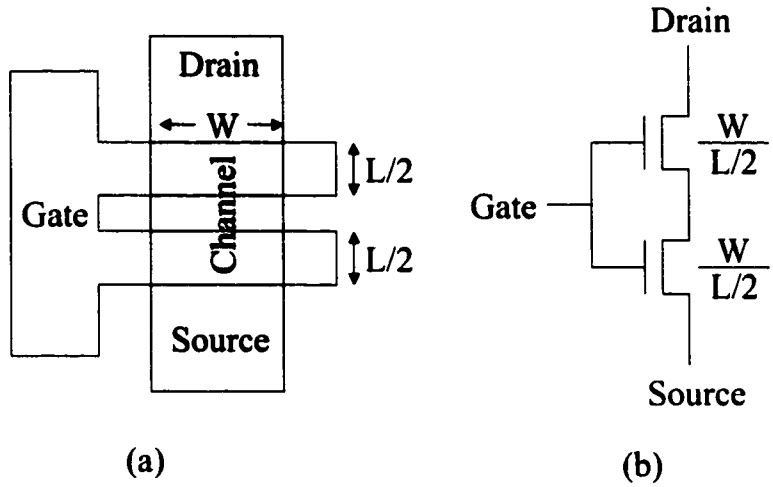

Figure 5.4. (a) Layout of the leakage-reducing double-gate TFT structure. The use of multiple gates lowers the peak electric field in the channel, so the dominant leakage mechanisms (trap-assisted tunneling and thermionic emission) are inhibited. (b) Circuit schematic of the double-gate TFT. Transistor width, W, is defined in the same way, whereas the length, L, is the sum of the two gate lengths.

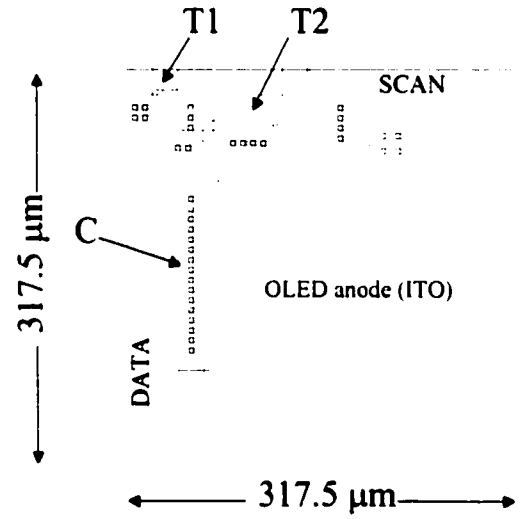

Figure 5.5. 2T AMOLED pixel layout. The data line runs vertically on the left side of the pixel, and the scan line runs horizontally at the top of the pixel. The switch TFT is a double-gated device to minimize leakage. The storage capacitor runs underneath the V_{DD} line on the left side of the pixel. Aperture ratio of the pixel defined by the ITO pad area is roughly 60%.

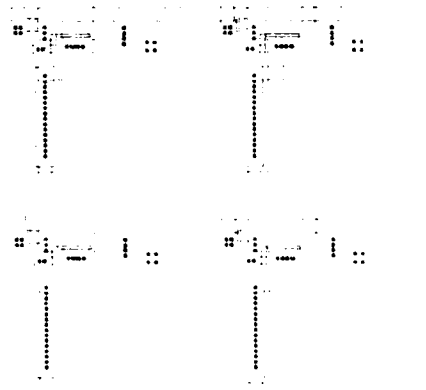

Figure 5.6. Stitching of four pixels. The total active-matrix array consists of 128x64 pixels.

5.3 Active-Matrix Process Flow

An integrated process flow for active-matrix fabrication was developed, and 4"x4" square glass substrates were processed to accommodate the equipment at Universal Display Corporation. (See Appendix for a detailed process runsheet.) First, a thick (>3μm) buffer oxide was deposited by LPCVD SiO_2. A "zero-level" lithography step was then performed, and alignment marks were etched into the buffer oxide. Next, the active Si film was depsoted by LPCVD at 550°C to a thickness of 500Å. Active layer lithography and patterning was then performed. An SF_6 plasma was used to etch the Si film.

Ion implantation (BF_2, dose $5x10^{15}cm^{-2}$, 20keV) was used form the bottom electrode of the pixel storage capacitor. A resist mask was used to prevent undesired implantation into the active regions of the pixel TFTs. LPCVD LTO (450°C) formed the

700Å- thick gate dielectric. The gate/scan-line metal was molybdenum, e-beam evaporated to a thickness of 1500Å. Mo patterning was then accomplished using standard lithography processes and SF_6 plasma etching. The Mo served as a mask for source/drain B^+ ion implantation (B^+, dose $5x10^{15}cm^{-2}$, 23keV). After implantation, a 5000Å thick ECR-PECVD passivation oxide was deposited. To activate the dopants and densify the passivation oxide, the substrates were annealed at 600°C in N_2 ambient for 15 hours.

Contact holes were etched through the passivation oxide, and data line metal consisting of a Ti/TiN/Al/Ni (450Å/200Å/1000Å/400Å) stack was deposited and patterned. The bottom Ti was used for better contact to poly-Si (lower contact resistance than Al), and the thin TiN layer capped the Ti to minimize the oxidation of titanium. The thick Al layer facilitates conductivity in the metal, and the top Ni layer provides a low resistance contact to the ITO.

The final 5000Å passivation layer formed the barrier between the active matrix devices and the OLED structures. Because organic materials are deposited by thermal evaporation, step coverage is poor. Thus it is important that the vias in the passivation layer have a tapered profile such that the organic films are continuous over the contact holes. Such a profile was achieved through the use of ECR-PECVD oxide, as follows: (1) a "dense" oxide (low deposition rate and low wet etch rate) was formed to a thickness of 4500Å, then (2) 500Å of a "porous" (high wet etch rate) oxide completed the layer. Using a dilute (5:1) BHF wet etch, the top porous layer was etched quickly and a large undercut developed, leading to a highly tapered via angle. Experiments demonstrated that good contact to the ITO and continuous step coverage in the organic layers were obtained using this process.

The design permitted the use of an additional nitride layer between the ITO and organic layers. Openings etched in the nitride define the emissive area of the pixel (where the organic films contact the ITO). The nitride also serves to separate the ITO-to-TFT contact from the OLED emissive area. The purpose behind this separation is to ensure uniform current density within the pixel. If the contact was located within the pixel itself, current crowding may occur there. The localized higher current density could reduce the OLED lifetime, which degrades quickly with increasing current density.

5.4 References

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Chapter 6

A Direct Patterning Method using Silicon-Germanium Films

6.1 Introduction

In order to be commercially viable, LCD manufacturers must produce displays that continue to be both lower in cost and higher in performance. The costliest and most complex component in the AMLCD manufacturing process is the active-matrix backplane; it requires the fabrication of large-area integrated circuits on glass panels with feature sizes on the order of a few microns. To date, the LCD industry has been able to leverage process technology from the IC industry, and display production has been rapidly built up on this knowledge base. The active-matrix cell in an LCD backplane is

similar in structure to a dynamic random-access memory (DRAM) cell, containing a (thin-film) transistor and (liquid-crystal) capacitor. Unfortunately, transistor size in display pixels cannot be scaled as in DRAMs because pixel size cannot be reduced beyond the discrimination of the human eye. As a result, the cost reduction per pixel for LCDs decreases much less rapidly compared to the cost per bit of DRAMs. In addition, in terms of price per unit area, LCDs garner significantly less revenue than DRAMs. This difference in revenue and the resulting need for larger (~$1m^2$) and more unwieldy (thickness < 0.5mm) glass panels indicate that the LCD manufacturing paradigm must depart from that of the IC industry in the near future. The development of novel manufacturing processes that dramatically decrease cost and improve display performance is critical to the large-area electronics industry's future growth.

One principal method of lowering manufacturing cost is the enlargement of glass substrate sizes with each generation, thus yielding more display panels per substrate. Unfortunately, display substrate scaling has a practical limit for a few reasons. First, as glass substrates increase in size, their thickness must be reduced accordingly to maintain a manageable handling weight. The latest Gen IV panels are 800mm×950mm with a thickness of less than 0.5mm. Future generation glass sheets will be increasingly fragile and difficult to handle. Secondly, substrate scaling will not be cost effective unless additional productivity improvements occur in TFT materials and process technology. There have been numerous efforts aimed at lowering manufacturing cost through decreased material consumption, increasing process throughput, and/or improving process uniformity (thereby improving yield). Deposition and etch processes used in standard VLSI manufacturing become particularly wasteful and problematic as substrate

size increases. Also, the standard plasma-processing tools used extensively in FPD manufacturing are best avoided if suitable alternative technologies were available. To enable a conveyor-belt type approach to handling large-area substrates, it is advantageous to use atmospheric-pressure process tools. Currently, tools with these process technologies are being developed: meniscus coating systems for substrate cleaning[1], and atmospheric-pressure chemical vapor deposition (APCVD) for thin-film deposition and annealing.[2] Meniscus coating techniques can also be used for wet etching and deposition of films.[3] Thus, process technologies compatible with the lower-cost conveyor-belt manufacturing model already exist for the each of the modules in a FPD front-end fabrication process – with the notable exception of a lithography module.

Inexpensive, large-area lithography methods are a central goal in the FPD industry.[4] Common tools are contact or proximity printers and large steppers akin to wafer steppers used in the VLSI industry. There are also the recently developed large-area scanning projection exposure tools, which provide lower defects and higher resolution than contact and proximity printers at a lower cost than steppers.[5] All of these tools create patterns by exposing a thin-film (~1μm) of photoresist that is subsequently developed and hardened to act as a mask for etching. The photoresist is typically spin-coated, which uses less than ~5% of the liquid film precursor. Due to the material and environmental cost (toxic waste disposal) of this conventional method, alternative means of coating resist are aggressively being developed, e.g. meniscus and capillary coating, and patch coating.

In this chapter, an innovative, efficient method for simplifying large-area patterning for FPD manufacture is presented. Specifically, a resist-free direct patterning

method using selective high-fluence laser (UV-light) exposure is demonstrated. To form a pattern, the laser light is directed through a patterned mask to alter a thin film on the substrate. The exposed film is then selectively etched (or not etched) away. In the preliminary results presented here, a sacrificial film (deposited *in-situ*) is used. The sacrificial layer mixes with the film in the areas selectively exposed by the laser, forming a compound that is highly selective to the patterned film in suitable chemical wet etches. This direct patterning method exploits laser processing, a tool already commonly used in FPD manufacturing. Table 6.1 compares the steps involved with conventional photolithography patterning and the proposed direct patterning method.

CONVENTIONAL METHOD	PROPOSED METHOD
1. substrate preparation a. dehydration b. prime 2. photoresist coat 3. pre- or softbake 4. UV-light exposure 5. post-exposure bake 6. photoresist develop 7. hardbake 8. etch 9. photoresist removal	1. sacrificial film deposition 2. UV-light exposure 3. etch

Table 6.1. Comparison of patterning methods. The proposed direct patterning method saves a considerable number of process steps.

The principal advantage of this direct-patterning process is the elimination of photoresist from the lithography process, resulting in a less expensive, safer and more environmentally friendly technique for patterning. In addition, dry etching for large-area FPD manufacturing and its associated problems (vacuum processing, etch uniformity, plasma damage, etc.) can be avoided since wet etch chemistries are highly selective. In the example process demonstrated here, little complexity and cost are added because the sacrificial film is deposited *in-situ*.

The direct patterning method can be used in other variations. For example, rather than fully melting the film, the laser can be used at a lower fluence to treat only the surface of the sample, e.g. forming a thin oxide layer to subsequently be used as hard mask for etching.

Anvik Corporation has developed high-resolution, large-area lithography tools for production of large-format electronics such as displays.[6] For example, the Anvik HexScan™ 3030 SXE employs a 308nm XeCl excimer laser to deliver 3μm resolution across substrate sizes up to 610mm x 915mm. Figure 6.1 shows an illustration of the system. The mask and substrate are mounted rigidly on a single planar stage, so issues concerning relative mask-substrate movements are eliminated. Because the Anvik system uses an excimer laser, it can perform both imaging and laser crystallization. Thus, it is ideally suited for the direct patterning method proposed in this chapter.

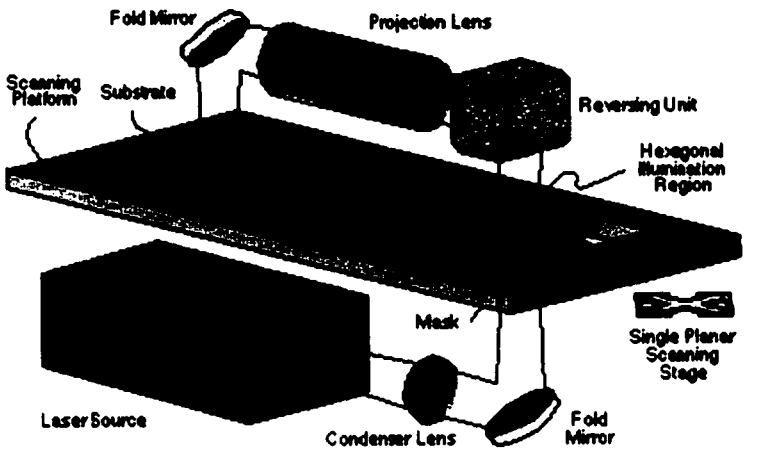


Figure 6.1 Illustration of an Anvik large-area patterning system. The mask and substrate are mounted on a single planar stage, which moves in x- and y-directions to scan the pattern across the substrate.

6.2 Process Description

The direct patterning method was successfully demonstrated in an initial experiment to pattern a thin silicon film using silicon-germanium (SiGe) as a sacrificial material. A description of the process follows.

A shadow mask with a transferable test pattern was fabricated. This mask was used to selectively expose the sample using a XeCl (λ=308nm) excimer laser. A 100mm-diameter double-polished quartz wafer was chosen as the mask substrate for its transparency and ability to withstand laser processing. First, pure Al was sputter-deposited to a thickness of 1μm. Next, a 200nm-thick SiO_2 film was deposited by PECVD. Using standard lithography procedures, a test pattern was formed on the quartz mask. The oxide was then dry-etched using an SF_6 plasma, and the Al was wet etched using a 40°C metal etchant bath. The finished mask contained various patterns (T- and L-shapes, interdigitated structures, etc.) with linewidths and spacings varying from tens of microns down to 1 μm.

The starting substrate for the sample was a thermally oxidized Si wafer. First, 50nm of amorphous silicon (a-Si) was deposited on the sample, followed by 50nm of $Si_{0.2}Ge_{0.8}$. The two films were deposited in-situ by LPCVD at 450°C. Next, the test mask was placed directly on top of the sample (the patterned Al side down), and a XeCl (λ=308nm) excimer laser was pulsed through the backside of the quartz wafer test mask and delivered to the sample. The energy from the laser caused the exposed Si and $Si_{0.2}Ge_{0.8}$ to mix and form a single alloy layer of $Si_{0.6}Ge_{0.4}$.[7] (The 200nm-thick oxide layer atop the Al pattern on the test mask served as an insulator and spacer to prevent the Al from reacting with the SiGe film. Figure 6.2 shows a schematic diagram of the process.) The laser fluences ranged from 150 mJ/cm^2 to 440 mJ/cm^2, and the number of laser pulses from 1 to 100. After exposure, the sample was immersed for 10 minutes in a standard "SC-1" cleaning solution (5:1:1 H_2O:H_2O_2:NH_4OH), which is a highly selective etch for SiGe.[8] Patterns of a-Si remained in the areas that were not exposed to the laser pulse.

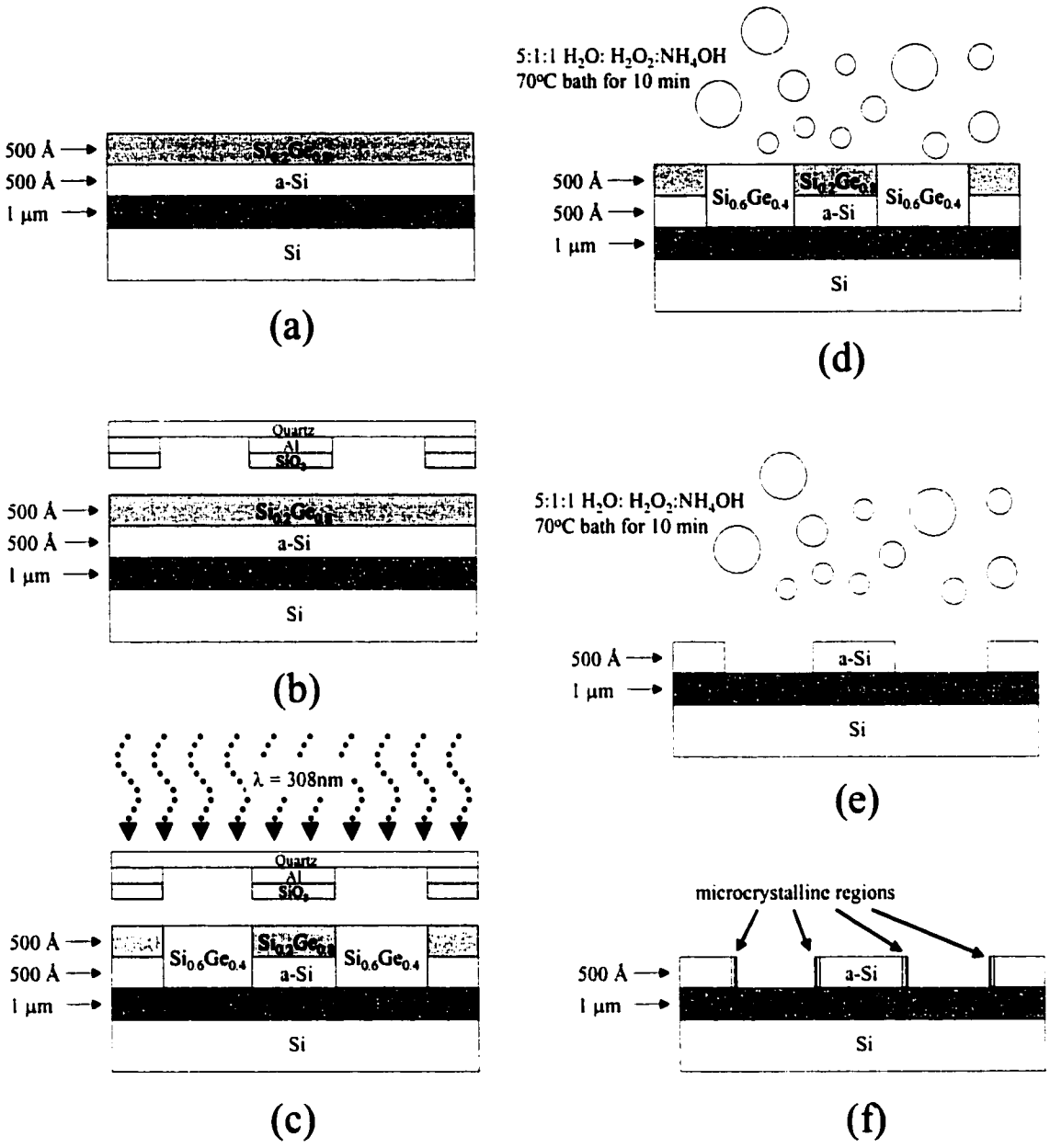
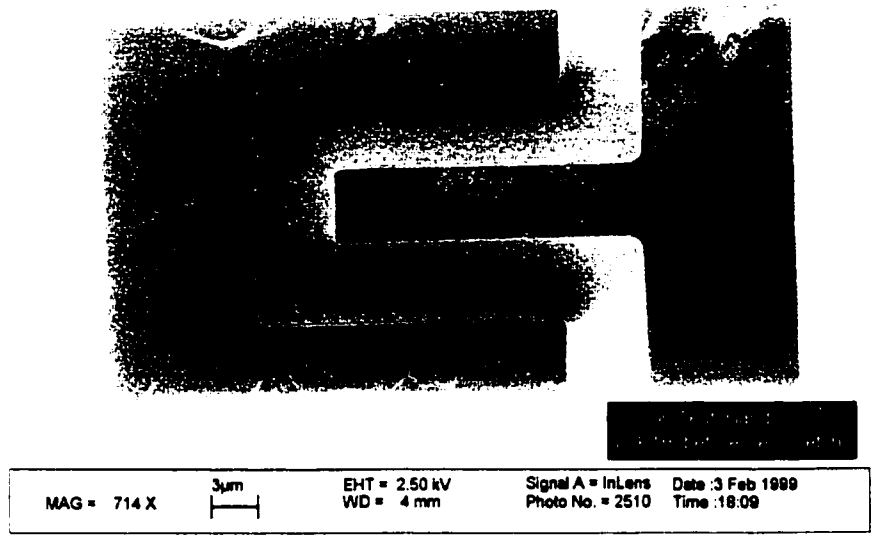


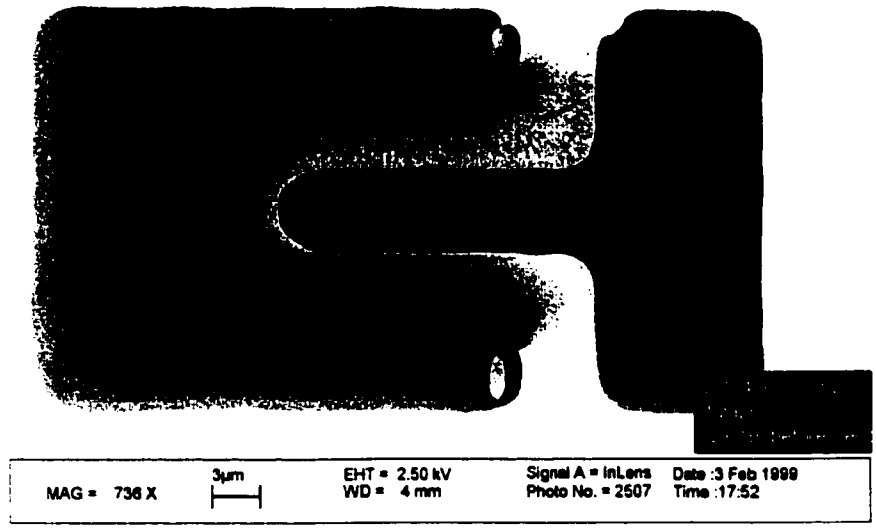
Figure 6.2. Schematic diagram of the direct patterning process flow. (a) The sample consists of a thermally oxidized wafer coated with 50nm of LPCVD a-Si followed by 50nm of LPCVD $Si_{0.2}Ge_{0.8}$ deposited in-situ. (b) The test mask is placed facedown on top of the sample and (c) then the sample is irradiated through the mask using a XeCl (λ=308nm) excimer laser. (d) The sample is then etched in a standard "SC-1" cleaning solution (e) to selectively remove the SiGe films. (f) The final pattern matches that of the test mask. The edges of a-Si islands are actually microcrystalline due to thermal conduction during laser crystallization.

6.3 Initial Results

After the direct patterning process was completed, the samples were examined using a scanning electron microscope (SEM). Figure 6.3 shows test patterns formed by (a) conventional resist-patterned lithography and dry etching compared with those formed by (b) the direct-patterning method using one pulse of an excimer laser at a fluence of 400mJ/cm^2. By conventional lithography, the narrow 4μm lines and corners on the test pattern were sharply defined. The direct patterning method reproduces the pattern reliably, but the sharpness of the corners suffers because of thermal conduction during the laser exposure. This heat conduction also leads to another phenomenon: a narrow band of microcrystalline Si exists around the perimeter of the patterned a-Si islands. (The film melts in the perimeter region due to its proximity to the exposed areas, but Ge is not mixed in with the Si.) This discovery provides an unexpected additional benefit. The microcrystalline region can serve as a seeding zone for subsequent grain growth when additional laser annealing is performed, leading to large lateral grain growth inward toward the center of the pattern, where the grains will meet and a single boundary will form. The active area of a poly-Si TFT can be used as the laser mask, so that self-aligned large-grained poly will form the channel region of the device.



(a)



(b)

Figure 6.3. SEM photographs of test patterns formed by (a) conventional photolithography and dry plasma etching and (b) the direct-patterning method using one pulse of an excimer laser at a fluence of 400 mJ/cm^2. Direct patterned features are rounded at the edges due to heat conduction that creeps inward during laser pulsing.

Multiple laser pulses were performed to determine the optimum number of shots for good pattern transfer. Figure 6.4 shows the same pattern but using five pulses of the laser at 400mJ/cm^2. The added pulses are detrimental to the patterning of the corner regions. At the corners, there is less Si film to conduct the heat away from the exposed regions. As a result, the corners and "ends" tend to absorb significantly more heat than the long edges. These areas become polycrystalline and Ge tends to diffuse further inwards with each laser pulse. Figure 6.5 shows a larger view of the corner region for a sample irradiated with five pulses. Unfortunately, this additional "creeping" of the Ge into Si is detrimental to good patterning. The SiGe compound is selectively removed by the SC-1 etch, and these areas then become holes in the desired pattern.

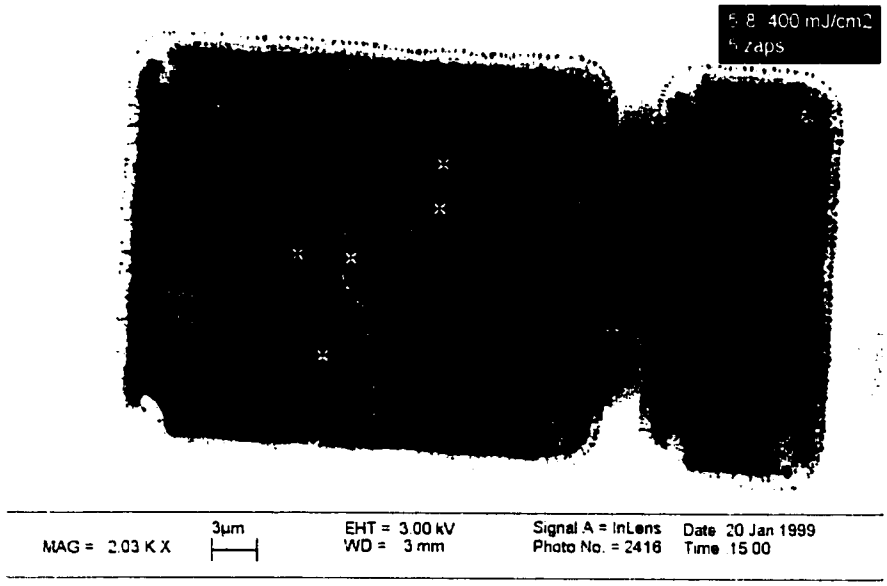


Figure 6.4. Direct patterned results using 5 laser pulses at 400mJ/cm^2.

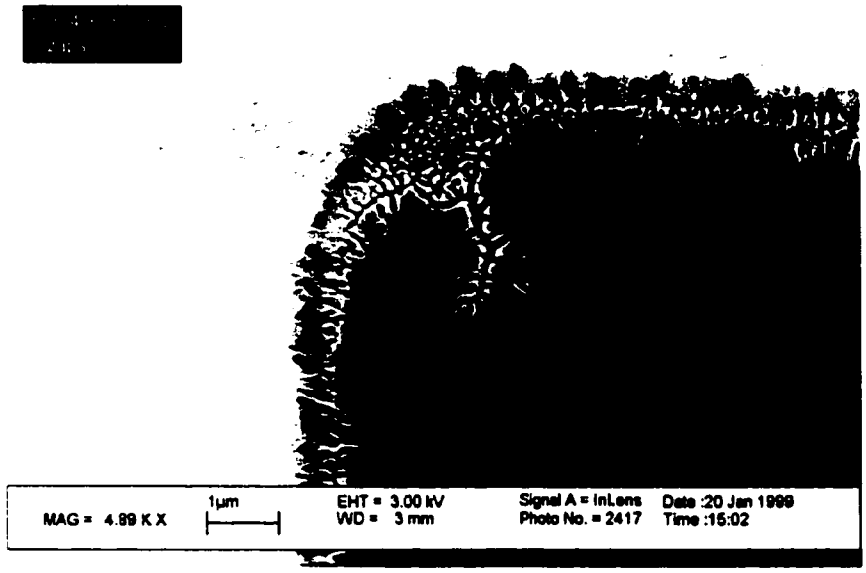
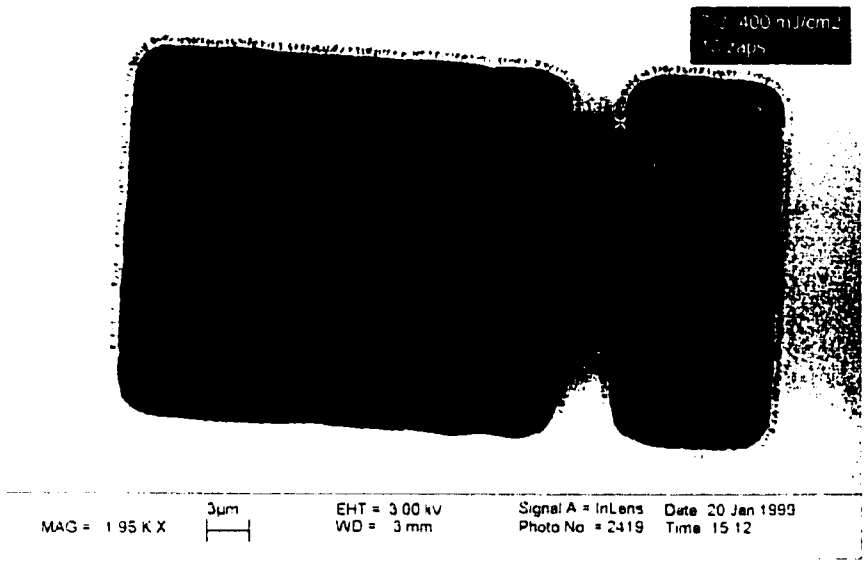
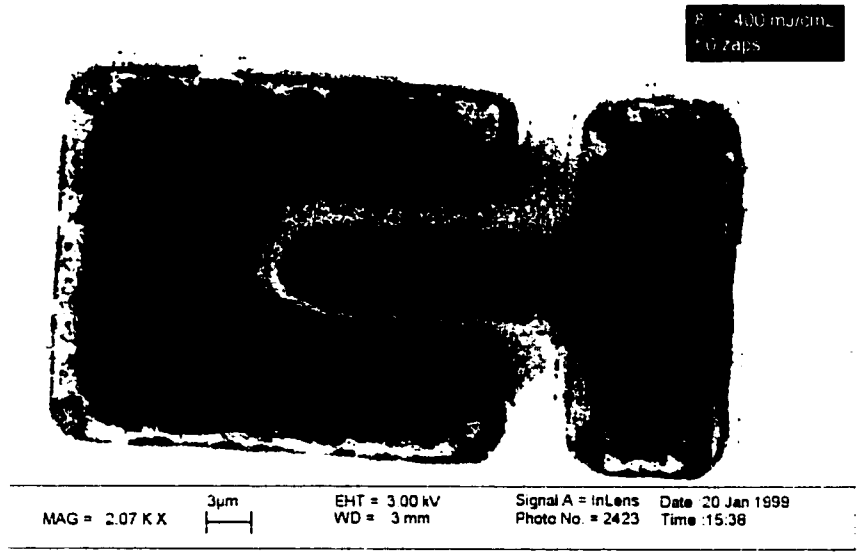


Figure 6.5. An enlarged view of the upper left corner of the test pattern in Figure 6.4. At the corners, there is less Si to remove heat, so additional mixing of the sacrificial layer creeps underneath the laser mask.

With additional pulses of the laser, the transferred pattern is progressively degraded. Figure 6.6 shows the pattern for 10, 50, and 100 pulses of the laser. There is no apparent advantage to using multiple laser shots. Even at lower energies, the same degradation of the test pattern occurs with a large number of pulses. Figure 6.7 shows the result from 100 pulses at 340mJ/cm^2.

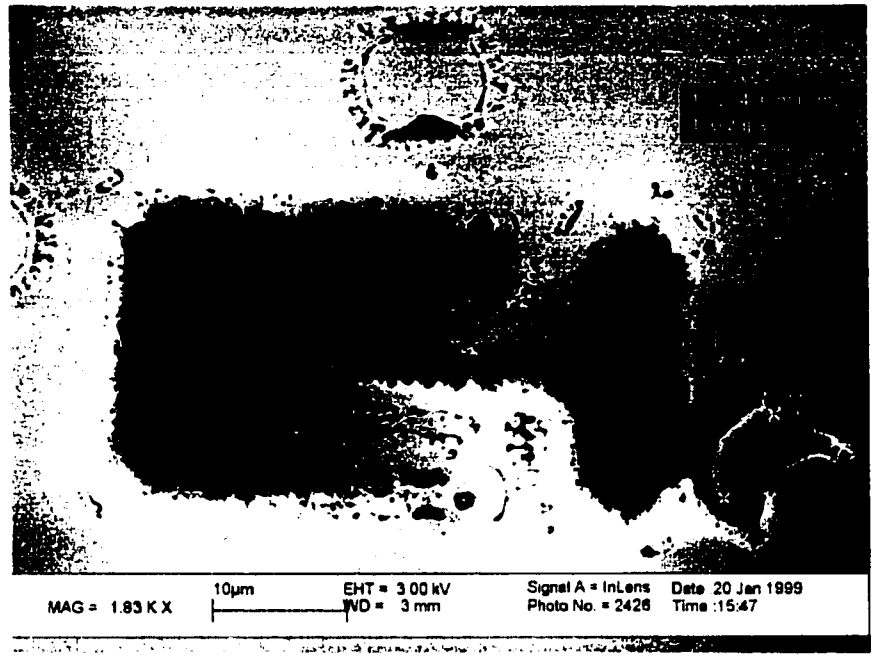


(a)



(b)

Figure 6.6 (a) & (b). *(continued on next page)*



(c)

Figure 6.6. Direct patterned results using 400mJ/cm^2 laser pulses with (a) 10 pulses, (b) 50 pulses, and (c) 100 pulses.

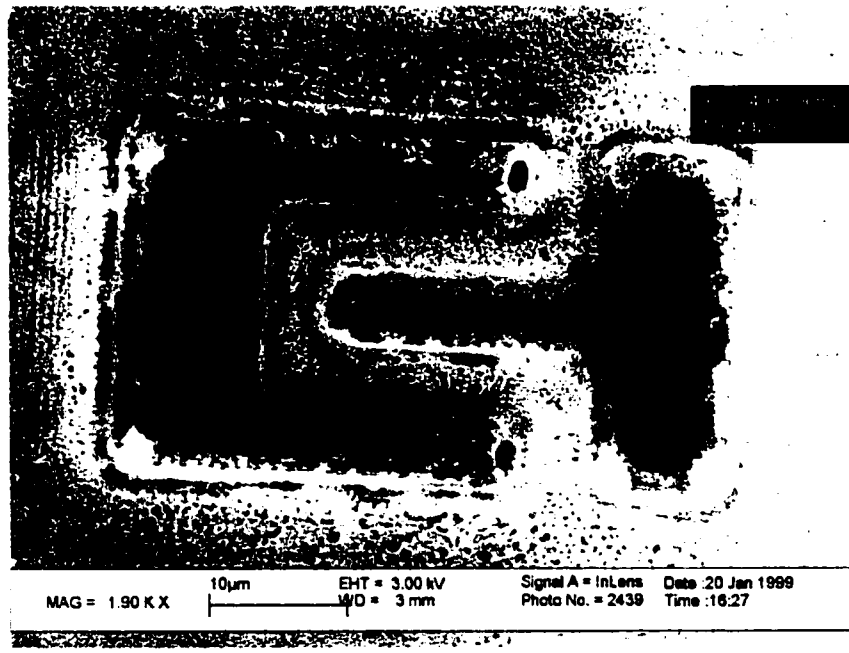


Figure 6.7. Direct patterned results with 100 pulses at a fluence of 340mJ/cm^2.

6.4 Conclusion

From our results, we determine that the optimum condition for the direct patterning method is to use one laser pulse at an energy that will fully melt both the sacrificial layer and the underlying layer to be patterned. If lower energies are used, the film to be patterned will not be completely cleared. Multiple shots cause the edges to become even less clearly defined.

Additional investigation is needed to achieve better edge profile control. It is possible that a more optimal sacrificial layer exists (different concentration of Ge or different thickness). Also, other materials commonly used in large-area electronics should be researched, e.g. indium tin oxide (ITO), Al, Ti, nitride and oxide. For large poly-Si TFTs, the method may yield high performance devices, since edge seeding may occur for significant lateral grain growth.

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Chapter 7

Conclusions

7.1 Summary

This dissertation has covered issues pertaining to the ultra-low temperature fabrication of poly-Si TFTs directly on plastic substrates for flexible, large area electronics applications. In this chapter the highlights of this work are summarized.

The use of high-density plasma CVD for gate dielectric formation at a maximum substrate temperature of 100°C was introduced. Compared to conventional parallel-plate RF PECVD reactors, ECR sources generate plasmas with densities two to three orders of magnitude higher and thus supply a higher ion flux to the substrate. This enhances surface reactions between the Si and O_2, yielding a high-quality Si/SiO_2 interface without elevating substrate temperature. A helicon source was also studied for comparison, and

similar improvements in interface quality were observed. Helicon sources generate plasmas that have similar characteristics to ECR source plasmas, but our particular helicon source PECVD oxide system had one substantial advantage over the ECR tool: The helicon chamber was part of a cluster tool that included a laser chamber for crystallizing poly-Si. In this configuration, the substrate was transferred directly to the helicon chamber immediately after laser annealing without breaking vacuum. Gate oxide deposition followed poly-Si formation without exposing the interface to air, theoretically eliminating the possibility of contamination and native oxide formation.

Poly-Si TFTs were fabricated at substrate temperatures below 150°C using ECR and helicon-source CVD gate oxides. The use of the ECR gate oxide yielded poly-Si TFTs with mobilities > $90cm^2/Vs$ and $V_T<10V$, the highest performance reported at the time for any TFT technology compatible with flexible polymer substrates (T_{MAX} = 150°C). By employing the *in-situ* helicon source gate oxide, poly-Si TFTs were fabricated at T_{MAX}=100°C with V_T=2.5V, $I_{ON/OFF}>10^6$, and mobilities ~$70cm^2/Vs$. These results were achieved without any post-fabrication passivation such as plasma hydrogenation, which requires temperatures higher than the melting point of plastic.

Next, the issue of ELC poly-Si film uniformity was investigated. Poly-Si formed by ELC produces high-quality grains (compared to solid phase crystallization), but the range of energy fluences in which large grain growth occurs is narrow. Outside of this super-lateral growth regime, poly-Si grains are small and uniform. Thus, conventional ELC of blanket Si films usually involves a tradeoff between achieving uniformly low-performance (small-grained poly) TFTs or high-performance (large-grained poly) TFTs with poor uniformity of device characteristics. A new method to realize uniformly large-

grained, high-performance poly-Si TFTs using ELC was introduced. Utilizing an anti-reflective (AR) capping layer method[1], poly-Si TFTs were fabricated with large grains self-aligned to the active channel region. The active layer mask was used to pattern the AR oxide cap prior to ELC. The resultant n-channel poly-Si TFTs exhibited drive currents that were about three orders of magnitude higher compared to the uncapped devices. These improvements were seen over a 50mJ/cm^2 range of laser energies. Our capping method provides improvement in device performance and uniformity while adding little complexity to the fabrication process.

In collaboration with Universal Display Corporation, a poly-Si TFT active-matrix organic light emitting diode (AMOLED) prototype display was designed. The 128x64 pixel monochrome display uses a simple two TFT pixel design to drive the OLEDs. Active-matrix (vs. passive-matrix) addressing is necessary to operate the OLEDs in constant current (vs. pulsed current) mode for peak efficiency and lifetime. In addition, poly-Si TFTs are better suited than a-Si TFTs for AMOLED displays, because current control of OLEDs is best accomplished by p-channel TFTs. To fulfill the drive requirements, p-channel TFTs should have hole mobility of at least 20cm^2/Vs, which is impossible with a-Si TFTs. While poly-Si TFT AMOLEDs have already been demonstrated on glass, a prototype flexible AMOLED fabricated on a polymer substrate would be an unprecedented accomplishment.

Lastly, a novel method for resist-free, direct patterning of Si films on large-area substrates was presented. Inexpensive, large-area lithography methods are a central goal in the FPD industry.[2] Currently, all patterning methods are performed by exposing a thin-film (~1μm) of photoresist that is subsequently developed and hardened to act as a mask

for etching. Photoresist is typically spin-coated, which uses less than 5% of the liquid film pre-cursor. Such low material usage is both expensive and environmentally unsound, so novel methods having more efficient usage are being developed.[3] A high-resolution patterning method that completely eliminates photoresist would be of great interest to the semiconductor electronics industry as a whole. A resist-free direct patterning method was demonstrated for the active silicon layer as follows: First, an excimer laser was used to selectively expose, melt and mix a sacrificial layer (Si_xGe_{1-x}) and the layer to be patterned (a-Si). Then, a highly selective wet etch was used to remove the SiGe films, leaving behind patterned a-Si. SEM photographs revealed that corners were not as sharp as those defined using conventional photolithography, but linewidths down to 3μm were easily obtained. For layers that contain only large feature sizes, the direct patterning method has many advantages. It reduces the number of required patterning steps from nine (conventional photoresist) to three (direct patterning). It does not require the use of photoresist, making the process clean and environmentally safe. The sacrificial film can be deposited *in-situ*, so the cost and time required for the additional deposition is minimal.

7.2 Contributions

The research presented in this dissertation has made significant contributions to the development of poly-Si TFT technology for large-area electronics applications. They are listed below:

- High-density plasma CVD oxides for use as gate dielectrics in poly-Si TFTs fabricated on plastic substrates. The use of ECR and helicon source

PECVD systems for oxide formation at room temperature yields high-quality Si/SiO_2 interface for high-performance poly-Si TFTs.

- Anti-reflective (AR) 50nm-thick patterned oxide capping layer for improved laser-crystallized poly-Si TFT performance and uniformity. A patterned AR oxide cap used prior to excimer laser annealing of Si films yields large-grain poly-Si that is aligned to the channel region. The method allows for significant grain growth to occur over a wide range of laser fluences and obviates the need to tradeoff performance for uniformity as is typical practice for ELC poly-Si TFTs.
- Resist-free, direct patterning method for large-area electronics. The use of an *in-situ* sacrificial film and selective excimer laser exposure simplifies the lithographic process for large-area electronics manufacture. By eliminating the need for photoresist, the introduced direct patterning method lowers cost by reducing material waste and reducing complexity. Initial experiments demonstrated feature sizes of a few microns for a-Si film patterning.

7.3 Suggestions for Future Work

The possibility for high-performance circuitry on plastic substrates has garnered a large amount of interest in the microelectronics industry. Presently, high-performance poly-Si TFTs have been demonstrated on a variety of flexible polymer materials.[4,5,6] The ultimate goal is to achieve a complete system-on-plastic, where the active-matrix display, driver circuitry, memory and logic circuits are all fully integrated on a single polymer

substrate. There exist many, many challenges before this goal can be realized, including issues that have yet to be discovered. The following section puts forth a few suggestions for work to follow up the research presented in this dissertation.

Ultra-Low Temperature Poly-Si TFT Process Development

The performance of poly-Si TFTs fabricated on plastic substrates is essentially dictated by the maximum substrate temperature. Device characteristics generally improve with high temperature processing, because both film and interface defects arising from strained or broken bonds are reduced significantly with annealing. For poly-Si TFTs on plastic, mimicking a high temperature anneal process through use of repeated laser pulses may improve film quality. Multiple laser pulses used on an absorbing layer (such as titanium nitride) could be used at key process points (e.g. after gate oxide deposition) to reduce defect density. Absorption layers lessen the impact of the high-energy laser and simultaneously localize the high-temperature treatment to the desired layers.

The ability to implement CMOS circuitry using poly-Si TFTs is important. To date, n-channel poly-Si TFTs fabricated on plastic exhibit superior performance to p-channel TFTs on plastic. Effective mobilities for n-channel poly-Si TFTs fabricated at 110°C are as high as $250cm^2/Vs$[6], compared to less than $30cm^2/Vs$ for p-channel poly-Si TFTs fabricated at the same temperature.[7] In addition, the threshold voltages are much higher for p-channel devices (>12V, compared to 2.5V for n-channel TFTs). The demonstration of a high-performance p-channel poly-Si TFT fabricated on plastic would pave the way for fully complementary circuits on plastic.

Poly-Si TFT performance on plastic suffers in part because there is no practical method for passivating the defects in the poly-Si film after the fabrication process is complete. Standard practice for poly-Si TFTs on glass is to perform a plasma hydrogenation at T≥300°C, which has the effect of improving all device parameters: i.e. lowering threshold voltage and leakage current, and increasing mobility and subthreshold slope. Additional research is needed to devise a method to incorporate passivating species into the poly-Si channel film at temperatures compatible with plastic. This remains a non-trivial problem, and the development of a 100°C passivation method would be a significant research contribution.

High-Density Plasma Source PECVD Oxides

In our study of the ECR and helicon source PECVD oxides, we gained a great deal of knowledge of the oxides' electrical properties. We found that the density of the deposited oxides could easily be controlled by changing plasma power and gas flow rates. Such control may prove useful for the buffer layer that isolates the TFT from the plastic substrate. These buffer dielectrics must be thick to protect the plastic from the laser pulses, and they ideally will have low residual stress. Conventional RF PECVD oxides deposited at 100°C to thicknesses greater than 1μm have high stress and cause the flexible plastic to curl. When the substrate cools, cracking often occurs, particularly for thick films. Using the helicon source PECVD system, we found that thick (>3μm) oxide films could be deposited on PET substrates with little stress and no cracking. However, the electrical and isolation properties of the oxide were untested. It would be interesting

to examine the mechanical vs. electrical properties of the ECR and helicon oxides for use as buffer layers on plastic.

Anti-Reflective Cap Layer for ELC Poly-Si

We presented preliminary results for poly-Si TFTs fabricated using the AR oxide cap layer. Because we needed to pre-specify the desired laser energies used for poly-Si crystallization, we found that we did not conclusively determine the lower bound of laser fluence that achieved large grained poly-Si. The upper bound was the point at which the oxide cap began to ablate, but it is unclear how wide a process window is achieved because the lower bound was not properly determined. The experiment should be repeated with lower fluences so that the actual process window improvement can be ascertained.

Direct Patterning of Films for Flat-Panel Display Manufacture

The preliminary results achieved indicate that the resistless lithography technique is promising for direct patterning of a-Si films. However, refinement of the process is needed to achieve better edge profile control. Our experiment assumed that the drawn pattern on the laser shadow mask would transfer directly to the film. It may be possible to obtain more precise corners and edges by tailoring the shadow mask patterns to account for thermal conduction changes based on surrounding features.

The microcrystalline region surrounding the patterns should be used to seed poly-Si grain growth, and investigations should be performed to determine whether this feature could be used for better grain growth control.

Additionally, in order for the method to be applicable to general flat-panel display manufacture, it must be demonstrated with commonly used materials such as indium tin oxide (ITO), aluminum, oxide, nitride, etc. Various sacrificial layers need to be used with these materials to determine the extent to which this method can be applied.

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Appendix A

AMOLED Process Runsheet

Run ID:
Start Date:
Description:
Starting Substrate Material: 4" square glass (obtained from UDC)

Barrier Layer Formation – SiO_2

Note: use devicegroup "clean" boat, lay samples flat with dummy support underneath

1. LPCVD oxide. 60 minutes @ 450°C in Tylan20 using VDOLTOD.020.
   O_2=90 sccm
   SiH_4=60 sccm
   Pressure = 300 mTorr
   Frontside
   SiO_2 thickness: _____ (target > 3μm)

2. LPCVD oxide. 60 minutes @ 450°C in Tylan20 using VDOLTOD.020.
   O_2=90 sccm
   SiH_4=60 sccm
   Pressure = 300 mTorr
   Backside
   SiO_2 thickness: _____ (target > 3μm)

Lithography – Zero level

UDC pattern and etch trenches in oxide (alignment marks for subsequent layers).

Active Layer Formation – LPCVD Si

LPCVD Si: 8.5 minutes @ 450°C in Tylan19 using SIGEVAR.

Si thickness: _____ (target = 500Å at 60Å/min dep rate)

Lithography – Island level

spinner1 – standard I-line resist; 15sec @ 0.60 krpm, 45sec at 4.1krpm

ksaligner – "active" layer mask

Note: Use double-sided tape to attach dummy wafer to 4" square sample (4 pieces usually secures the bond)

"soft contact" program

Parameters: Time = 8 sec
Al. Gap = 15μm

Note: *Perform alignment with gap > 75μm, reduce gap to 15μm just prior to exposure*

Inspection/General Comments:

Si etch – island definition

Ptherm – SF_6 plasma etch

SF_6 flow = 100 sccm, Power = 250W, Time = 8 sec for 500Å Si etch

Pressure ≈70 mTorr

Resist removal

Ptherm – O_2 plasma

O_2 flow = 100 sccm, Power = 250W, Time = 2 min for complete resist removal

Pressure ≈60 mTorr

Lithography – Capacitor mask

spinner1 – NEGATIVE resist:

1. spin HMDS 45 sec @ 5.0 krpm
2. spin resist 15 sec @ 0.6 krpm
3. spin resist 45 sec @ 5 krpm
4. softbake resist 1min @ 90°C

ksaligner – "capacitor" layer mask

Note: Use double-sided tape to attach dummy wafer to 4" square sample (4 pieces usually secures the bond)

"soft contact" program

Parameters: Time = 30 sec (total dose required is 1.4J at 365nm)
Al. Gap = 15μm

Note: *Perform alignment with gap > 75μm, reduce gap to 15μm just prior to exposure*

Inspection/General Comments:

Capacitor Ion Implantation – Core Systems special request

BF_2 implant (for shallow implant depth, less expense)

Dose = 5e15

Energy = 20 keV

Gate SiO_2 Formation – LPCVD SiO_2

Need to reduce dep rate to control oxide thickness (because sample is laid flat).

Use recipe VDOLTOI.020 and reduce SiH_4 flow rate to 10 sccm.

LPCVD oxide. 5 min. 53 sec @ 450°C in Tylan20 using VDOLTOD.020.

O_2=90 sccm

SiH_4=10 sccm

Pressure = 300 mTorr

SiO_2 thickness: _____ (target = 700Å at dep rate = 119Å/min)

Gate / Scan line metal deposition (Mo)

Molybdenum e-beam evaporation by Xiaofan Meng.

Total target thickness = 1500Å

Lithography – gate level

spinner1 – standard I-line resist; 15sec @ 0.60 krpm, 45sec at 4.1krpm

ksaligner – "gate/scan" layer mask

Note: Use double-sided tape to attach dummy wafer to 4" square sample (4 pieces usually secures the bond)

"soft contact" program
Parameters: Time = 5 sec (reduced time because Mo is reflective)
Al. Gap = 15μm
Note: *Perform alignment with gap > 75μm, reduce gap to 15μm just prior to exposure*
Inspection/General Comments:

Mo gate etching

NO WET ETCH!! Control is extremely difficult. Use ptherm for dry etch.
ptherm – SF_6 plasma etch
SF_6 flow rate = 100 sccm
Power = 50W
Pressure = 60mTorr
Time ≈10 min.
NOTE: Etch for short time intervals, open chamber, and inspect sample. Etch rate can vary significantly from run to run.

Resist removal

S1165 wet bath – see Xiaofan Meng for this stripper (which will not attack Mo)
Use on hot plate for faster resist stripping. Do not use high temps, or else S1165 will boil.

Source/Drain Ion Implantation – Core Systems special request

B implant
Dose = 5e15
Energy = 23 keV

Passivation oxide deposition

pqecr – standard recipe: (SiH_4=100sccm, O_2=20sccm, Ar=120sccm, Power = 350W)
SiO_2 thickness: _____ (target = 5000Å, time = 910sec)

Dopant activation anneal / passivation oxide densification

tylan14 – 14anneal; N_2 flow, modify to run at 600°C
Anneal for 15 hrs.

Lithography – contact level

spinner1 – standard I-line resist; 15sec @ 0.60 krpm, 45sec at 4.1krpm
ksaligner – "contact" layer mask
Note: Use double-sided tape to attach dummy wafer to 4" square sample (4 pieces usually secures the bond)
"soft contact" program
Parameters: Time = 5-8 sec
Al. Gap = 15μm
Note: *Perform alignment with gap > 75μm, reduce gap to 15μm just prior to exposure*
Inspection/General Comments:

Data line metal deposition

cpa – Ti/TiN/Al/Ni 4-layer contact metal
Ti: 20mTorr, 80cm/min, 2.5 kW, ~450Å/pass (1 pass)
TiN: 15mTorr Ar, 5mTorr N_2, 80cm/min, 2.5kW, ~200Å/pass (1 pass)
Al: 6mTorr, 66cm/min, 4.5 kW, ~366Å/pass (3 passes)
Ni: 15mTorr, 80cm/min, 1.0kW, ~200Å/pass (2 passes)
Total thickness **(use witness wafer)**: _____

Lithography – Data line level

spinner1 – standard I-line resist; 15sec @ 0.60 krpm, 45sec at 4.1krpm
ksaligner – "vdd / data" layer mask
Note: Use double-sided tape to attach dummy wafer to 4" square sample (4 pieces usually secures the bond)
"soft contact" program
Parameters: Time = 5 sec
Al. Gap = 15μm

Note: *Perform alignment with gap > 75μm, reduce gap to 15μm just prior to exposure*

Inspection/General Comments:

Metal1 Etching

sink8 – use heated Al etchant bath to clear *both* Ni and Al.

Time ~ 2min 15sec

sink7 – HF: H_2O_2: H_2O (1:1:20) for 35 sec or until Ti/TiN clears

Inspection Comments:

TESTING: Probe TFT test structures to determine whether devices work

"Spin-on-glass" deposition – taper layer

pqecr – dual layer: 4500Å "dense" SiO_2 + 500Å "porous" SiO_2

1. "dense" SiO_2 recipe: SiH_4=40sccm, O_2=75sccm, N_2=150sccm, Power=800W
   a. To get ~4500Å, perform 10 cycles of this recipe at
      i. gas stabilization (60sec)
      ii. deposition (300 sec)
      iii. cooling (60 sec)
2. "porous" SiO_2 recipe: SiH_4=100sccm, O_2=20sccm, Ar=120sccm, Power=350W, Time = 80sec

SiO_2 thickness: _____ (target = 5000Å)

Lithography – Via

spinner1 – standard I-line resist; 15sec @ 0.60 krpm, 45sec at 4.1krpm

ksaligner – "via" layer mask

Note: Use double-sided tape to attach dummy wafer to 4" square sample (4 pieces usually secures the bond)

"soft contact" program

Parameters: Time = 5 sec
Al. Gap = 15μm

Note: *Perform alignment with gap > 75μm, reduce gap to 15μm just prior to exposure*

Inspection/General Comments:

Tapered Via etch

Use 5:1 dilute BHF to get tapered sidewalls – see Yong-Sang for etch details

Send to UDC for ITO & backend OLED deposition

Appendix B

TFT Mask Layouts

B.1 Simplified Two Mask Set TFT Layout

Notes: This is a non-CMOS layout. Wafers will have either all n- or all p-channel TFTs.
The minimum probe-able dimension is $\lambda = 50\mu m$.

W'=50μm (Note: this is always the case)

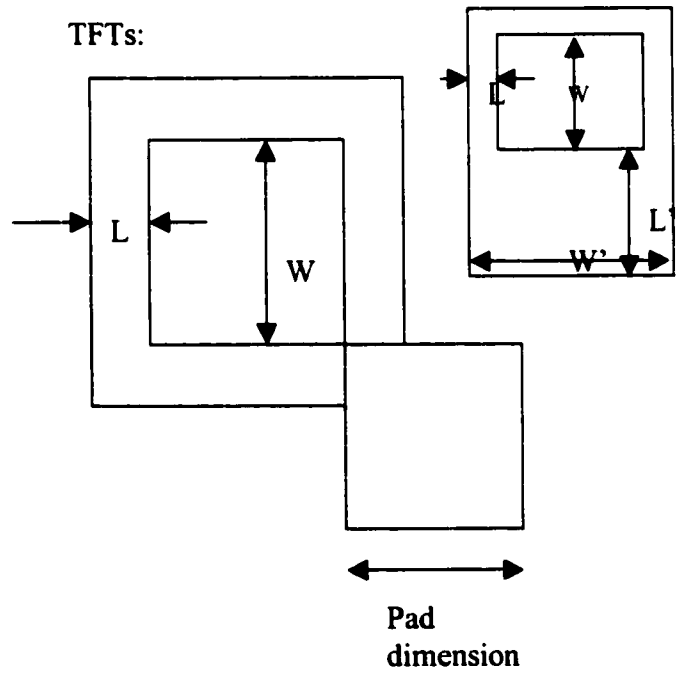
L' = 50μm
W=50μm; L=10, 8, 5, 3, 2.5, 2, 1
W=100μm; L=10, 8, 5, 3, 2.5, 2, 1
W=150μm; L=10, 8, 5, 3, 2.5, 2, 1

L' = 75μm
W=50μm; L=10, 8, 5, 3, 2.5, 2, 1
W=100μm; L=10, 8, 5, 3, 2.5, 2, 1
W=150μm; L=10, 8, 5, 3, 2.5, 2, 1

L' = 100μm
W=50μm; L=10, 8, 5, 3, 2.5, 2, 1
W=100μm; L=10, 8, 5, 3, 2.5, 2, 1
W=150μm; L=10, 8, 5, 3, 2.5, 2, 1

For L<10μm

Pad Size = 50μm x 50μm
W=50μm; L=50, 20, 15
W=75μm; L=50, 20, 15
W=100μm; L=50, 20, 15



Pad Size = 75μm x 75μm
W=50μm; L=50, 20, 15
W=75μm; L=50, 20, 15
W=100μm; L=50, 20, 15

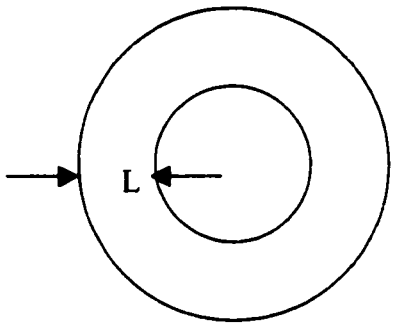
Pad Size = 100μm x 100μm
W=50μm; L=50, 20, 15
W=75μm; L=50, 20, 15
W=100μm; L=50, 20, 15

Circular Ring TFTs:
W/L = 20

L = 50μm, 100μm, 200μm
W_{eff}=1000μm, 2000μm, 4000μm

R_S=54.2μm, 135.5μm, 270.9μm, 541.8μm

SEM structures:
Lines for cross-section (L=2mm) W=10, 5, 2, 1



R_S is the inner radius

B.2 Conventional TFT Mask Set Structures List

Test TFTs: (n- and p-channel)

W=1; L=50, 20, 15, 10, 8, 5, 4, 3, 2, 1
W=1.5; L=50, 20, 15, 10, 8, 5, 4, 3, 2, 1
W=2; L=50, 20, 15, 10, 8, 5, 4, 3, 2, 1
W=5; L=50, 20, 15, 10, 8, 5, 4, 3, 2, 1
W=10; L=50, 20, 15, 10, 8, 5, 4, 3, 2, 1
W=50; L=50, 20, 15, 10, 8, 5, 4, 3, 2, 1
W=100; L=50, 20, 15, 10, 8, 5, 4, 3, 2, 1
TOTAL: 20 columns (check to see if W=100 will fit in between the contact pads!!)

Body Contact TFTs: (n- and p-channel)

W=5; L=50, 20, 15, 10, 8, 5, 4, 3, 2, 1
X=20, 10, 8, 5, 4, 2, 2, 1, 1, 1 (corresponding to the L's)

* take care when laying out the body contact
TOTAL: 4 columns

Double-Gate TFTs: (n- and p-channel)

W=50; L_G=10, 5, 4, 2, 1; separation = 2μm
TOTAL: 2 columns

Offset HV TFTs: (n- and p-channel)

W=50; L=15 offset: 5, 2, 1 (one of each 2, 1 with channel contact)
TOTAL: 2 columns

Reliability TFTs: (n- and p-channel)

W=50; L=15, 10 (5 each)
TOTAL: 4 columns

Uniformity TFTs: (n-channel only)

W=50; L=50, 5, 2, 1 (5 each)
W=1; L=50, 5, 2, 1 (5 each)
TOTAL: 8 columns

Cross Bridge Kelvin Structures:

Met1 – doped poly: 2x2, 2x2, 3x3, 4x4, 5x5
Met1 – gate: 2x2, 2x2, 3x3, 4x4, 5x5
TOTAL: 3 columns

Sheet resistance:

Island (n and p), Gate, Met1: 200/40, 200/10, 200/5, 100/10, 100/5

Capacitors: (use gate finger structure as in TFT07)

gate – n+ island: 200μm x 200μm, 1mm x 1mm

SEM structures:

Lines for cross-section (L=2mm) W=10, 5, 2, 1
Spaced lines (gate level): 10 + 10 (space) + 10, etc for the different sizes
Island, Gate, Met1

Inverters:

NMOS Load: 50/20, 10/4
CMOS: 50/20, 10/4

Verniers: (both x- and y-directions)

75um x 25um
Down (or Right)– 1.6um lines, 2.0um spaces
Up (or Left)– 2.0um lines, 1.7um spaces

Miscellaneous Notes:

Use 1um design rules

Mask levels:

1. Island
2. Body contact (use N+ and P+ masks)
3. Gate
4. N+
5. P+
6. Contact
7. Metal

Standard contact hole size is $3x3um^2$
Metal to Island – 2um
Contact to Metal – 2um
Gate overlap – greater than 5um

Pads are 120um with 80um spacing between