**Reliability Studies of Micro-Relays for Logic Applications**

by

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# Abstract

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The semiconductor industry is now struggling with an integrated-circuit “chip” power density crisis due to the non-scalability of the thermal voltage ($k_BT/q$), which sets the minimum subthreshold swing (SS) of a metal-oxide-semiconductor transistor and hence limits reductions in transistor threshold voltage and hence chip operating voltage. In contrast to electronic switches, mechanical switches (“relays”) operate by making/breaking physical contact and therefore offer the ideal characteristics of zero off-state leakage current and abrupt transition between on/off states, which provide for zero static power dissipation and (in principle) lower operating voltage, so that they potentially can provide a means for overcoming this crisis. In order to fully realize their promise, however, miniaturized relays must operate with sufficient reliability to be viable for ultra-low-power digital logic applications.

In this work, the reliability of micro-relays designed for digital logic applications is systematically investigated. Contact resistance ($R_{on}$) instability is identified as the limiting factor for micro-relay endurance. Due to surface oxidation, $R_{on}$ of prototype relays with tungsten (W) contacting electrodes increases with the number of operating cycles. This phenomenon is affected by relay operating conditions, including switching frequency and contact force. Larger contact force is found to be beneficial for stable operation, possibly due to breakdown of the insulating oxide layers. An alternative contact electrode material, ruthenium (Ru), is demonstrated to ameliorate the problem of metal surface oxidation; however, friction polymer formation and material transfer become dominant contact reliability issues, which eventually degrade $R_{on}$. An inkjet-printed micro-shell encapsulation process is used to provide an isolated ambient environment for the logic relays, and demonstrated to result in improved $R_{on}$ stability by 100× as compared to devices tested in atmospheric conditions.

In complementary logic circuits, slower switch turn-off than turn-on results in undesirable "crowbar” current, causing transient power dissipation during signal transitions and potential reliability issues. The effects of the contact electrode material mechanical properties, relay design parameters, and relay operating conditions on contact

detachment delay ($\tau_{CD}$) are experimentally studied and theoretically explained. Specifically, $\tau_{CD}$ is compared for logic relays with tungsten, ruthenium or nickel contacting electrode materials, and tungsten is found to provide for the smallest $\tau_{CD}$.

*To my family*

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| | |
|---|---|
| AES | Auger Electron Spectroscopy |
| ALD | Atomic Layer Deposition |
| CMOS | Complementary Metal-Oxide Semiconductor |
| ESD | Electro-Static Discharge |
| DC | Direct Current |
| GHz | Gigahertz |
| ICP | Inductively Coupled Plasma |
| kHz | Kilohertz |
| LPCVD | Low Pressure Chemical Vapor Deposition |
| LTO | Low Temperature Oxide |
| MEMS | Microelectromechanical Systems |
| MHz | Megahertz |
| $N_2$ | Nitrogen |
| Ru | Ruthenium |
| $RuO_2$ | Ruthenium Dioxide |
| SEM | Scanning Electron Micrograph |
| Si | Silicon |
| $SiO_2$ | Silicon Dioxide |
| $TiO_2$ | Titanium Dioxide |
| $V_{DD}$ | Supply Voltage |
| W | Tungsten |

# ACKNOWLEDGEMENTS

Professor Tsu-Jae King Liu, my advisor, who led me into this field, deserves the most credits and my sincere gratitude goes to her. She provided me much guidance as she could while leaving me the freedom to explore my own interests. Her care, patience and leadership qualities could not be matched. I would like to thank Professors Ming Wu and Liwei Lin as well for their valuable feedback as members of my qualifying exam and thesis committee. Their lectures on microelectronics and mechanical transducers were well-presented and laid a strong foundation for my graduate studies.

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# Chapter 1

# Introduction

Transistor off-state leakage current hinders reductions in transistor threshold voltage and hence operating voltage, so that power density management constrains the design and performance of integrated circuits (ICs) implemented with nanometer-scale complementary metal-oxide-semiconductor (CMOS) transistor technologies. In contrast to a transistor, a mechanical switch can achieve zero OFF-state leakage current to provide for zero static power dissipation; also, its abrupt switching behavior facilitates reductions in operating voltage for ultra-low dynamic power dissipation. Owing to advancements in planar processing techniques, miniaturize mechanical switches (relays) now can be fabricated on Si wafers to implement ultra-low-power digital logic ICs. They can be used to implement core processors, *e.g.* in autonomous sensor motes [1], or can be used in conjunction with transistors, *e.g.* as power gates to eliminate undesired power consumption of CMOS circuit blocks in "sleep" mode [2]. In particular, electrostatically actuated relays are promising for these applications due to their faster switching speed, smaller size, and lower operating power as compared with other relay designs.

## 1.1 CMOS Scaling Challenge

Transistor miniaturization ("scaling") and other advancements in CMOS technology over the past few decades have led to tremendous gains in integrated-circuit "chip" performance and functionality, with reductions in cost per function. Due to the non-scalability of the thermal voltage ($V_T = k_B T/q$) as to the OFF-state current, the transistor operating voltage ($V_{DD}$) has not scaled proportionately with transistor dimensions [3], so that power density has increased and now constrains chip design [4].

The OFF-state leakage current ($I_{OFF}$) flowing between the drain and source regions in a MOSFET is related to the transistor threshold voltage ($V_{th}$) by the following equation:

$$I_{OFF} \propto e^{-V_{th}/S} \tag{1.1}$$

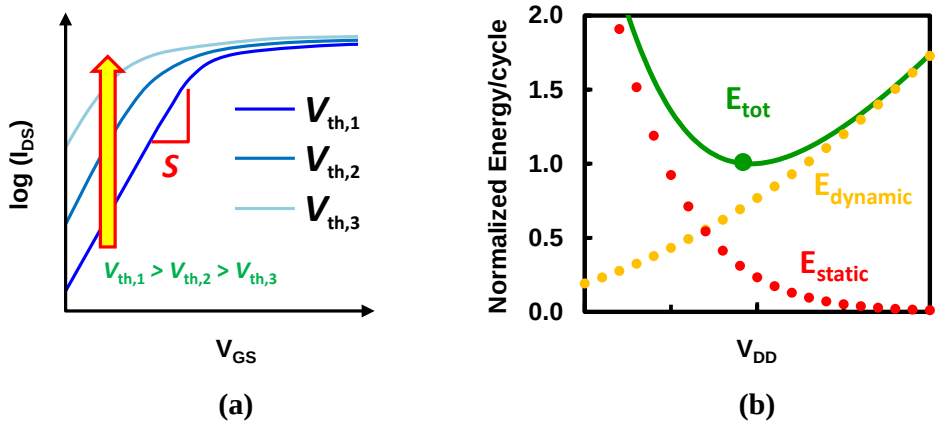



Figure 1-1. (a) Illustration of transfer ($I_{DS}$ *vs.* $V_{GS}$) characteristics of an n-channel MOS transistor, for different values of threshold voltage $V_{th}$. (b) Energy per operation for a CMOS digital logic circuit.

where $S$ is the subthreshold swing, *i.e.* the inverse slope of $\log(I_D)$ versus $V_{GS}$, which represents the steepness of the transition from the OFF state to the ON state and is fundamentally limited to be no less than $V_T \times \ln(10) = 60$ mV/dec at room temperature.

The dynamic power consumption of a CMOS digital logic circuit is proportional to $V_{DD}^2$ and hence can be reduced by lowering $V_{DD}$. In order to maintain the same gate overdrive voltage ($V_{DD}-V_{th}$) for high performance, $V_{th}$ should be reduced together with $V_{DD}$. However, this would undesirably raise $I_{OFF}$ (cf. Eq. (1.1) and Fig 1−1 (a)) and hence the static power consumption which is proportional to $I_{OFF} \times V_{DD}$. Therefore, $V_{DD}$ scaling has slowed dramatically with CMOS technology advancement beyond the 90 nm node.

To forestall a CMOS power density crisis as more transistors are packed into a given area, parallelism (*i.e.* multi-core processing) has been adopted to facilitate reductions in $V_{DD}$ (and hence increases in transistor density) while achieving improvements in overall chip performance. However, this approach will cease to provide for improved energy efficiency when $V_{DD}$ is reduced to $V_{th}$ [5]. As depicted in Fig. 1−1 (b), the total energy consumed per operation ($E_{tot}$) starts to increase as $V_{DD}$ decreases below an optimum value ($V_{th}$). In other words, the energy efficiency of CMOS technology has a fundamental limit due to transistor OFF-state leakage current. To overcome this limit, an alternative logic switch that can operate with higher ON/OFF current ratio than a MOSFET is needed.

## 1.2 Mechanical Switches for Computing

Among the candidate switching devices, miniature mechanical switches ("relays") based on metal-to-metal contacts are perhaps the most intriguing ones. The "mechanical transistor" is realized by replacing the channel with a narrow air gap and the body (or gate) electrode with a suspended movable assembly. The conduction of currents now necessitates physical mating of metal (or any conductive material in general) contacts

instead of formation of the inversion layer. Relays already are used today for a wide variety of industrial applications including automatic testing equipment (ATE), telecommunication networks and power management systems [6]. With continuing progress in planar processing technology and surface micromachining technology, micro/nanometer-scale relays that bridge the electrical and mechanical domains can be constructed directly on Si wafer substrates. With materials and process optimization, the co-fabrication of CMOS circuitry and micro-electro-mechanical devices (MEMS) can provide for improvements in energy efficiency as well as reductions in integrated system size and cost, for many consumer electronics applications [7].

Due to a physical air gap which exists between the conducting (output) electrodes in the OFF state, a relay exhibits zero $I_{OFF}$, which would eliminate static power consumption. Also, since a mechanical switch exhibits abrupt turn-ON/turn-OFF behavior, in principle it can be designed to operate with very small voltage swing ($V_{DD}$), which would provide for low dynamic power consumption. Therefore, microrelay technology has attracted significant interest for digital integrated circuit application in recent years [1], [8]. It has been projected that a scaled relay technology can provide for more than 10× improvement in energy efficiency compared to CMOS technology at the same node [9].

## 1.3 Actuation Mechanisms

The actuator is the heart of a micromechanical relay, which converts an electrical input signal into mechanical displacement. MEMS actuators fall into four main categories: magnetic, thermal, piezoelectric and electrostatic. The latter three will be reviewed below.

### 1.3.1 Electrothermal

Joule heating caused by passing a current through a conductor can result in a net change of its length/width, where the change is proportional to the material's coefficient of thermal expansion. This change in dimensions can be tailored to provide strain as well as displacement. A variety of different structures can take advantage of this type of actuation, and a method of augmenting the displacement is an essential part of thermal actuators. Fig. 1−2 depicts four examples of utilizing constrained thermal expansion to achieve amplified motions in micro-actuators.

Bimetallic actuators use two materials with different coefficients of thermal expansion that are vertically stacked together [10]. Any elevation in temperature would lead to a thermal expansion difference between the two layers, resulting in a bending moment to create vertical displacement (c.f. Fig. 1−2 (a)).

On the other hand, pseudo bimorphs exploits asymmetrical expansion with a thermal gradient by raising the temperature at a local spot [11]. The beam with smaller cross-

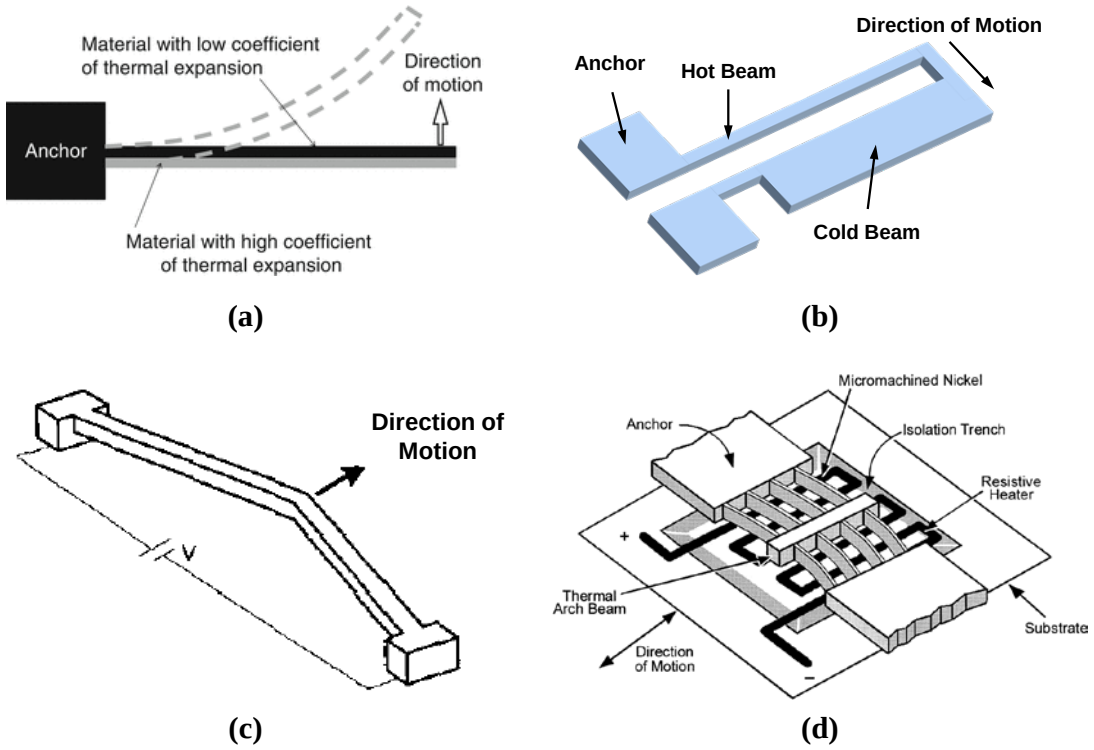



Figure 1-2. Examples of thermal actuator designs, including (a) bimorph [10], (b) pseudo-bimorph (U-shaped) [11], (c) geometry-based (V-shaped/chevron style) [12], and (d) a thermal arch beam microactuator (TAB) [13].

section area exhibits a higher electrical resistance, and would experience a more rapid increase in temperature when subjected to a given voltage bias. As the "hot" leg expands more than the "cold" leg, an in-plane rotation is introduced in the direction shown in Fig. 1−2 (b).

Another thermal actuation approach is to employ geometric constraints to create an affinity for the actuator to move in the desired direction [12]. An example of this type of amplification is the "V-shaped" actuator, illustrated in Fig. 1−2 (c). The pre-buckled shape ensures that the beam moves outward when the beam is heated up and expands. Actuators can be connected in parallel to linearly increase the contact force (but not the displacement). Streeter *et al.* [13] proposed a thermal arch beam actuator (TAB) that exploits similar concept. This in-plane thermal actuator combines an external heater (polysilicon resistors) underneath to induce an initial displacement, and an internal heater (arch beams) to provide additional tuning. The shuttle moves in the predefined direction upon further arching of the coupled beams due to thermal expansion.

High contact force (~mN) can be attained easily by electrothermal actuation in principle, which offers the advantages of low contact resistance and good contact reliability [14]. A standard comb-drive actuator (with 100 fingers and 2 μm thick structure) yields a force density of 20 μN/mm$^2$ while an U-shaped thermal actuator can reach 450 μN/mm$^2$ [15]. However, thermal actuators are plagued by relatively slow

switching speed (typically on the order of ms) and high operating power since continuous current is needed to maintain displacement unless the device accommodates some latching mechanisms [16]. Although they are not attractive candidates for low-power logic applications, electrothermal microrelays are potentially suitable for RF switching and analog systems (such as ATE).

### 1.3.2 Piezoelectric

Piezoelectricity is the linear coupling between electric polarization ($P_i$) and mechanical strain ($\varepsilon_{ij}$) or stress ($\sigma_{ij}$). The induced stress/strain is in general perpendicular to the direction of the applied electric field. For example, under the presence of a vertical electric field across the piezoelectric material, an in-plane strain would develop internally owing to the effective $d_{31}$ ($e_{31,f}$) piezocoefficient. Piezoelectric materials therefore can be used to implement actuators in which displacement is induced by an applied electric field ($E_k$).

A common method to achieve amplified deflection in a piezoelectric actuator is to employ a bimorph structure [17], similarly as in the aforementioned thermal actuators. Recently, an aluminum-nitride (AlN) piezoelectric relay based on this operating principle has been proposed and demonstrated by researchers at the University of Pennsylvania [18], [19]. The device utilizes a multi-layered beam comprising two AlN layers sandwiched by three metal electrode layers, as shown in Fig. 1−3. This electrode configuration generates in-plane strains of different polarity (tensile and compressive) to induce a bending moment about the neutral axis of the beam, resulting in out-of-plane motion to turn ON/OFF the switch. A dual beam design wherein the output electrodes each comprise the same multi-layer material stack provides for better immunity to residual stress gradient, as both electrodes experience the same deflection to achieve a

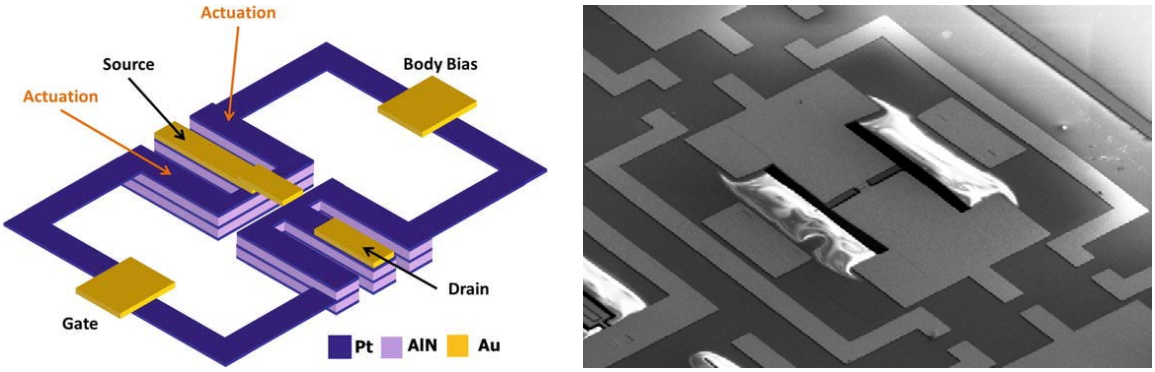



Figure 1-3. (a) 3D schematic view and (b) scanning electron micrograph (SEM) of the dual-beam piezoelectric switch [18], [19].

fairly consistent initial (zero-bias) contact gap upon device release.

An advantage of the piezoelectric actuator stems from the fact that the beam deflection is linearly controlled by the applied electric field across the piezoelectric layers. This is in contrast to an electrostatic actuator which can enter an unstable regime of operation (air gap-dependent) and causes the actuated beam to snap into the ON state, resulting in a large hysteresis voltage. In a piezoelectric relay, hysteretic switching behavior is due only to contact surface adhesive force, so that the hysteresis voltage can be very small. As demonstrated by Sinha *et al.* [19], the AlN relay can operate with sub-100 mV gate voltage swing, with a body bias voltage applied. This relay technology offers better switching speed (< 1 μs) and lower active power consumption (as compared with electrothermally actuated relays), with a low gate leakage current density of 2 $nA/cm^2$ for an applied voltage of 1 V across a 100 nm-thick AlN film [20]. Thus, piezoelectric microrelay technology is a viable candidate for low-power mechanical computing.

### 1.3.3 Electrostatic

Electrostatic (capacitive) actuation is perhaps the simplest means to implement in a microscale relay, since conductive electrodes and an air gap are the only required elements to envision an electrostatic actuator. Moreover, the structure/electrode materials are usually CMOS compatible. Coulomb's law dictates that the force between two electrodes that are oppositely charged is inversely proportional to their separation distance, and proportional to their overlap area. The actuator typically comprises a suspended electrode (which is supported by one or more beams) and a fixed electrode, as shown in Fig. 1−4. In essence, the electrostatic force induced by the electric field (resulting from a voltage applied across the two electrodes) works against the mechanical (spring) restoring force of the suspension beam(s) to displace the suspended electrode and initiate contact closure.

The spring restoring force increases linearly with the displacement, whereas the electrostatic force increases super-linearly. Once the applied voltage is such that the displacement exceeds 1/3 of the initial actuation air gap thickness [23], the electrostatic

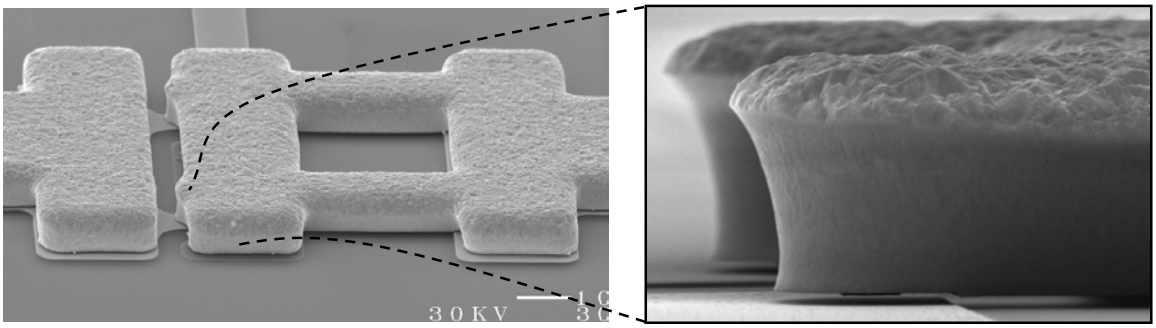



Figure 1-4. SEM images of an electrostatic microswitch based on a double cantilever beam [21], [22].

force exceeds the spring restoring force so that the suspended electrode snaps down toward the fixed actuation electrode. The air gap thickness in the contact region is usually engineered to be smaller than the air gap thickness in the actuation region, to prevent the suspended electrode from coming into contact with the actuation electrode. The applied voltage then must be reduced below the "pull-in" voltage for the spring restoring force to overcome the electrostatic force (and surface adhesive force) to turn OFF the relay, resulting in hysteretic switching behavior which ultimately limits reductions in the relay operating voltage. It should be noted that pull-in mode operation can be avoided (and hence the hysteresis voltage can be substantially reduced) by designing the contact "dimple" gap to be less than 1/3 of the actuation gap. This is not easy to achieve in practice for a planar structure, however, due to out-of-plane deflection caused by residual stress and strain gradient which increase the contact/actuation gap ratio. The square-law electrostatic force can be linearized by using differential electrostatic actuation. This is commonly achieved with comb-drive actuators, which remove the dependence of force on deflection with a dc bias voltage and ac input signal. As shown in Figure 1−5, they consist of interdigitated fingers (combs), with one set of combs being stationary and the other set of combs attached to a compliant suspension.

Though constrained by the nature of nonlinear motion, electrostatic microrelays can achieve relatively fast switching speed (~100 ns) and smaller form factor as compared with other relay designs, which are desirable for digital integrated-circuit applications. Moreover, electrostatic micro-relays have been demonstrated to have the highest contact reliability (under hot-switching conditions) to date, >10 billion cycles [22], [25], so that they show promise for future low-cost, ultra-low-power electronics applications.

## 1.4 Reliability Challenges

Although microrelays have been shown to offer advantages over CMOS transistors as

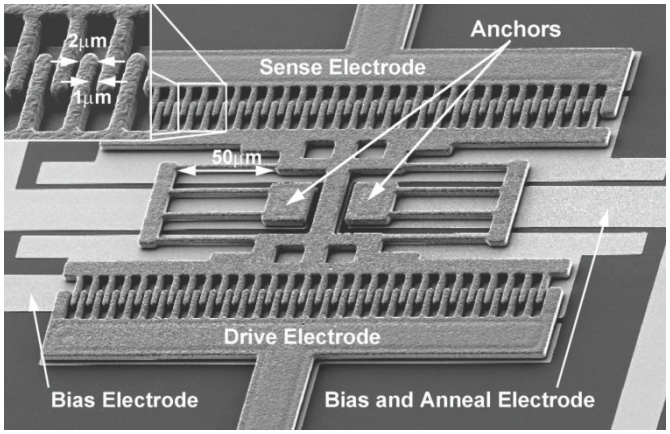



Figure 1-5. SEM image of an electrostatic comb-drive actuator (resonator) [24].

logic switches, they have yet to demonstrate sufficient reliability in ON-state resistance/current to be practical for computing applications. For comparison, the projected hot-carrier dc lifetime for MOS transistors is usually targeted at 10 years for 10 % of degradation in $I_d$. But the most reliable ohmic-contact microrelays demonstrated to date ([22], [25]) can operate stably for merely one month (assuming switching continuously at a frequency of 10 kHz). The lack of a standard process flow and reliability characterization methodology further hinders the development of a fundamental understanding of the predominant reliability failure mechanism for logic relays.

## 1.5 Thesis Outline

This research focuses on the characterization and investigation of the reliability of micro-relays designed for digital logic applications. Chapter 1 provides the motivation behind this work and reviews various MEMS actuation mechanisms. Chapter 2 discusses in detail the design, modeling, and microfabrication process for electrostatic logic micro-relays. Chapter 3 covers different schemes for characterizing the reliability of a micro-relay, showing that contact resistance instability is the limiter for relay endurance. Chapter 4 describes various methods for improving metal contact stability, and the influence of contact force. Experimental results for relays with ruthenium (Ru) contacts, as well as for a novel packaging technology utilizing inkjet-printing, are included. Chapter 5 presents a study of contact detachment delay, which previously has not been studied in detail. Chapter 6 summarizes the contributions of this work and suggests some possible future research directions.

# Chapter 2

# Design, Operation and Microfabrication of Logic Relays

## 2.1 Introduction

The logic micro-relays studied in this work are vertically actuated capacitive transducers. They have the advantage of modest actuation gap thickness, which is easily defined by the sacrificial layer thickness instead of the resolution of the photolithography process. As a result, their operating voltage is generally smaller than that of laterally actuated relays.

Fig. 2–1 presents the structure and operation of the four-terminal (4T) relay design for digital logic applications [26]. When a sufficiently large voltage is applied between the movable body electrode and the underlying gate electrode (*i.e.* $|V_{GB}| \geq |V_{PI}|$), the body is actuated downward sufficiently to bring the channel (a metallic strip attached to the underside of the body via an intermediary insulating layer) into contact with the source

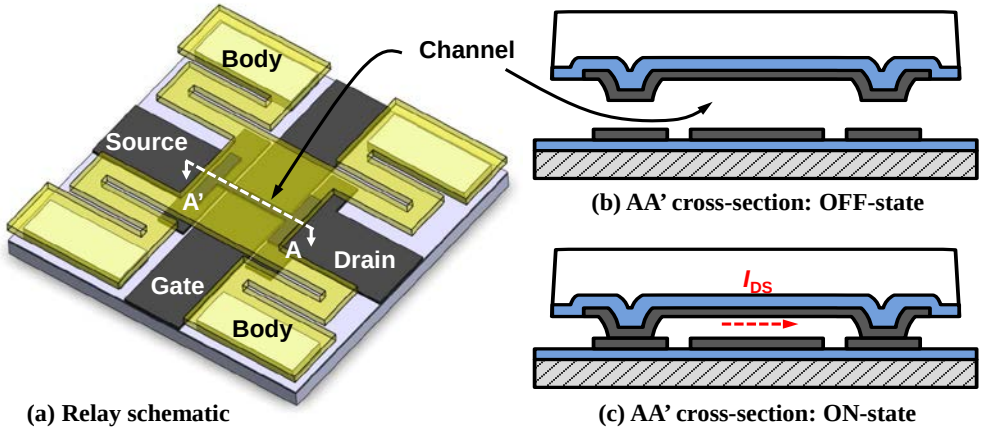



Figure 2-1. Schematic illustrations of the four-terminal logic relay used in this work: (a) Plan view illustrating the various terminals (b) Cross-sectional view along A-A' in the OFF state and (c) in the ON state.

and drain electrodes (which are coplanar with the gate electrode) so that current can flow ($|I_{DS}| > 0$) and hence the relay is ON. When $|V_{GB}|$ is lowered back down to below the release voltage ($|V_{RL}|$), the spring-restoring force of the folded-flexure suspension beams overcomes the attractive (electrostatic and adhesive) forces to actuate the body upward, bringing the channel out of contact with the source/drain electrodes so that no current can flow; hence the relay is OFF.

Serpentine beams are employed as the mechanical springs because they are relatively compact and can support a large range of motion. Also, as compared to straight suspension beams, the meandering beams have smaller peak stress under flexure and are robust against the effect of residual stress, so that $V_{PI}$ does not significantly change with process variations [27]. Analytical solutions for the stiffness $k_z$ of serpentine springs have been developed based on the virtual work method (for number of meanders $N = 1$) [28]:

$$k_z = \left[ \frac{8a^3 + 2b^3}{3EI_x} + \frac{ab(3b+8a)}{3GJ} - \frac{a^2\left(\frac{2a}{EI_x} + \frac{3b}{GJ}\right)^2}{2\left(\frac{a}{EI_x} + \frac{b}{GJ}\right)} - \frac{b^2}{2}\left(\frac{a}{GJ} + \frac{b}{EI_x}\right) \right]^{-1} \tag{2.1}$$

where $a$ is the connector beam length; $b$ is the primary beam length; $E$ is the effective Young's modulus of the composite structure; $I_x$ is the x-axis moment of inertia given by $w \cdot t^3/12$ where $w$ is the beam width for both beams and $t$ is the membrane thickness; $G$ is the shear modulus, and $J$ is the torsion constant.

## 2.2 Fabrication Process

As illustrated in Fig. 2–2, a five-mask fabrication flow, compatible with standard CMOS process, was utilized to fabricate the electrostatic logic microrelays.

First, as shown in Fig. 2–2 (a), an insulating layer of 80-nm-thick aluminum oxide ($Al_2O_3$) was deposited by atomic-layer-deposition (ALD) onto the Si (100) wafer substrate. Then a 70-nm-thick metal electrode layer was sputtered onto the insulated substrate. As will be discussed in Chapter 3, tungsten (W) is selected as the electrode material since it has very high hardness and melting point. The W was patterned using $SF_6$-based inductively coupled plasma (ICP) etching, which has a good selectivity (~10) to the $Al_2O_3$ layer underneath. Afterwards a first sacrificial layer of low-temperature oxide (LTO) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 400˚C. The source and drain contact regions (1 $\mu m^2$ in area each, unless otherwise noted) were then defined by removing the LTO in these regions using masked $CF_4$-based ICP

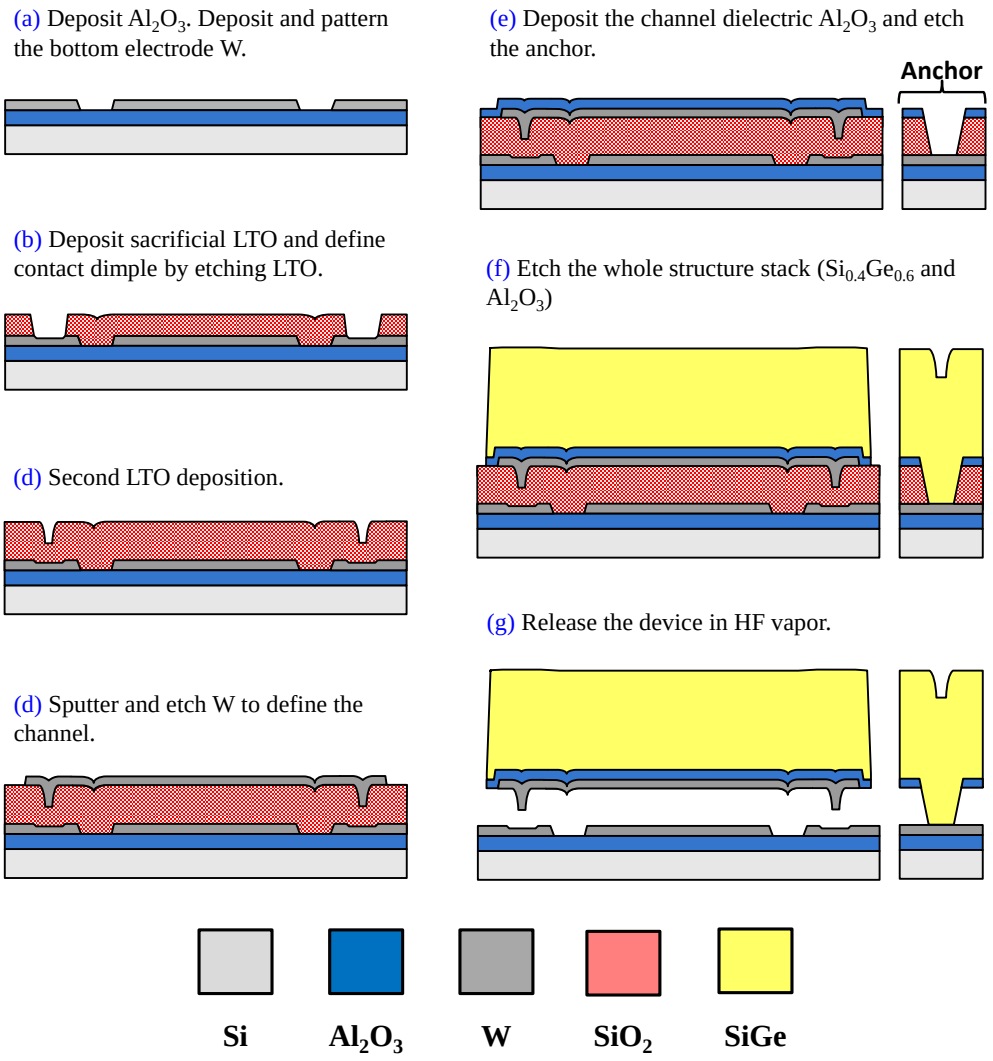



Figure 2-2. Cross-sectional process flow for the electrostatic logic microrelay.

etching, as shown in Fig. 2–2 (b). Subsequently a second sacrificial layer of LTO was deposited. Its thickness (80 nm) defines the nominal contact gap thickness, whereas the total thickness of the two sacrificial LTO layers (160 nm) defines the nominal actuation gap thickness, as shown in Fig. 2–2 (c).

Using the same material (W) as the source and drain electrodes, the channel was then formed by sputter deposition (note that the channel is dimpled in the contact regions) and patterning as depicted in Fig. 2–2 (d). Both the bottom electrodes and the top electrodes can be formed using alternative metallic materials, using a lift-off process that is detailed in Chapter 4. The anchor regions were defined by etching through the $Al_2O_3/SiO_2$ stack after deposition of a 55-nm-thick $Al_2O_3$ insulating layer (to electrically isolate the channel from the body), as shown in Fig. 2–2 (e). Note that if the anchor pads are drawn sufficiently large, this step can be omitted since the remaining oxide underneath could

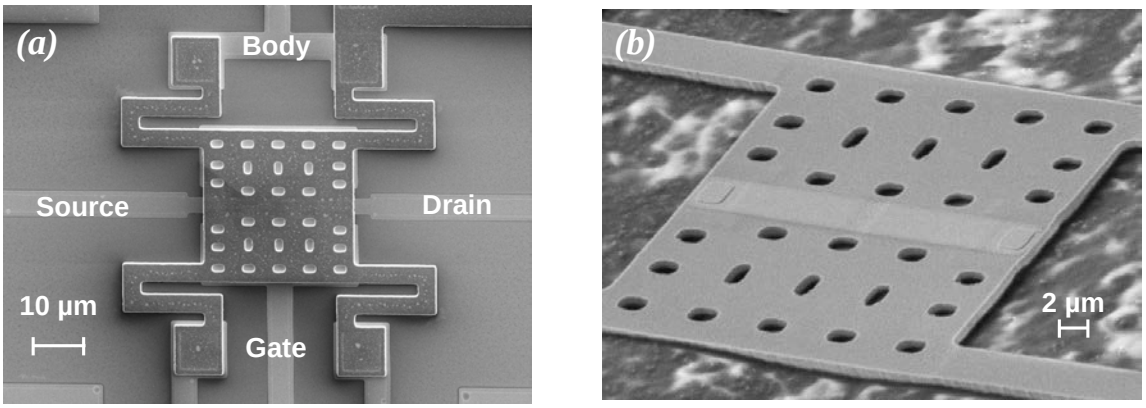



Figure 2-3. Scanning electron (SEM) micrographs of a micro-relay (a) as fabricated, and (b) structural portion lifted off and flipped over to show the dimpled channel.

serve to anchor the structure, to reduce the number of masks to 4. Serving as the main structural layer, *in-situ* boron-doped polycrystalline silicon-germanium (poly-$Si_{0.35}Ge_{0.65}$) was deposited by LPCVD at 410˚C and patterned by $HBr/Cl_2$-based transformer coupled plasma (TCP) etching, as shown in Fig. 2–2 (f). Finally, the sacrificial LTO layers were selectively removed in HF vapor to release the structure, as shown in Fig. 2–2 (g).

Fig. 2–3 (a) shows a scanning electron microscopy (SEM) image of a fabricated micro-relay with W electrodes. Fig 2–3 (b) is a SEM image of the underside of the movable structure, showing the channel with two distinct contact dimples.

## 2.3 Relay Operating Characteristics

This section details the electrical measurements including dc transfer curves and frequency response as well as some modeling results of the logic relay.

### 2.3.1 Static Characteristics

Fig. 2−4 (a) shows a typical $I_{DS}$-$V_{GB}$ characteristics for a logic micro-relay comprising p-type poly-SiGe as the structural material and W as the contacting electrode material. Two phenomena account for the hysteretic switching behavior: contact surface adhesive force, and bi-stability due to the pull-in phenomenon. Contact adhesion arises from the van der Waals force and molecular interaction between the deformed contacting asperities. The bi-stable phenomenon results from an imbalance between the mechanical spring restoring force and the electrostatic actuation force. The quadratic growth of electrostatic force prevails over the linearly increasing elastic force as the actuation voltage exceeds the pull-in voltage $V_{PI}$. A second solution to the system requires $V_{RL}$ <

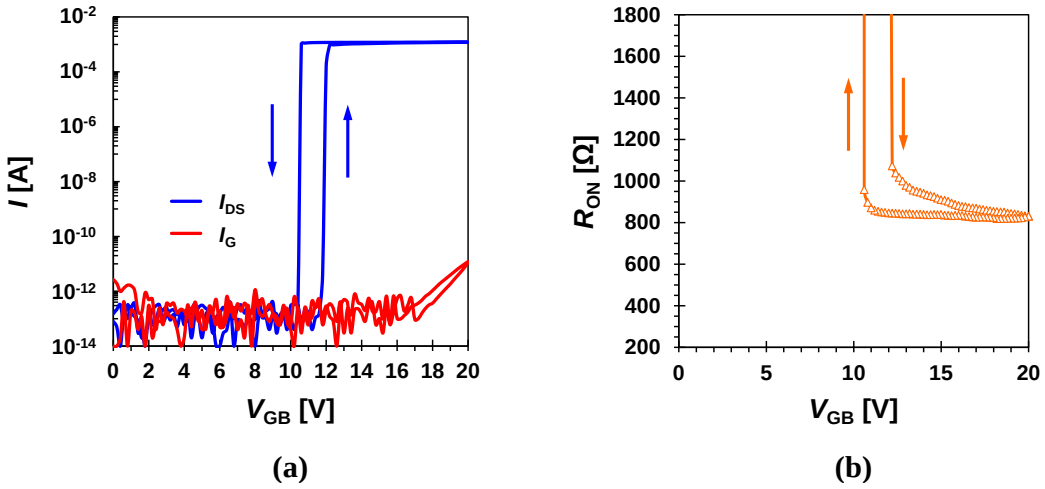



Figure 2-4. (a) Measured $I_{DS}$-$V_{GB}$ characteristics of a 4T relay, with $V_D$ = 1 V and $V_S$ = $V_B$ = 0 V ($L_{BEAM}$ = 9 μm). (b) $R_{ON}$ versus the gate-to-body voltage $V_{GB}$.

$V_{PI}$, yielding the hysteretic behavior [29]. The classical equation for the pull-in voltage of a parallel-plate capacitive actuator is

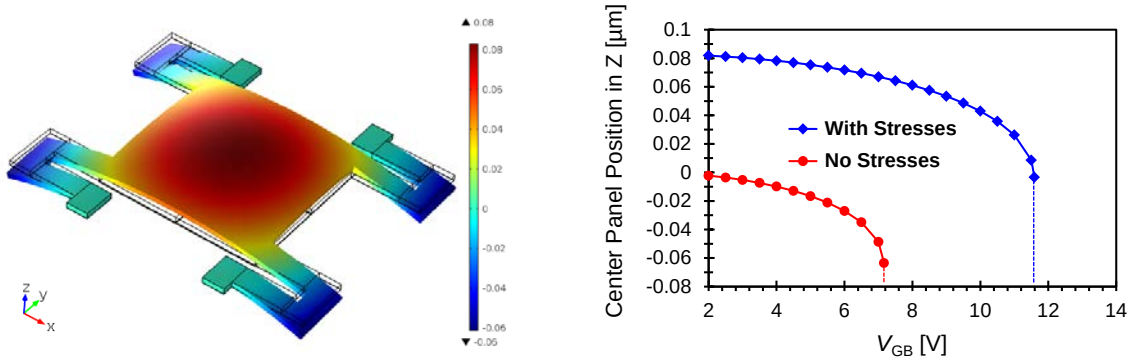
$$V_{PI} = \sqrt{\frac{8}{27} \cdot \frac{k g_0^3}{\varepsilon_0 A}} \tag{2.1}$$

where $k$ denotes the effective spring constant; $g_0$ is the initial (as-fabricated) actuation gap; $\varepsilon_0$ is the permittivity of air, and $A$ represents the actuation area [23]. As discussed in [30], the release voltage $V_{RL}$ is given by

$$V_{RL} = \sqrt{\frac{2k}{\varepsilon_0 A} \cdot (g_0 - g) \cdot g^2} \tag{2.2}$$

where $g$ is the initial contact dimple gap thickness. Without surface adhesive force, hysteresis-free dc characteristics ($V_{RL}$ = $V_{PI}$) could be realized by engineering $g$ to be less than or equal to (2/3)$g_0$, in theory. In practice, however, out-of-plane deflection due to the non-zero strain gradient and stress difference within the membrane stack makes it difficult to precisely control the gap ratio.

Fig. 2−4 (b) shows the evolution of $R_{ON}$ during a load-unload cycle (extracted from the measured $I_{DS}$-$V_{GB}$ curve in Fig. 2−2 (a)). It appears to be less sensitive to contact force during the unloading (turn-off) phase as compared to the loading (turn-on) phase, and remains roughly constant until the electrodes are nearly separated. In general, the real contact area initially remains constant during unloading (which is equivalent to the




**(a)** **(b)**

Figure 2-5. Simulated (a) initial out-of-plane warpage due to residual stress/stress gradient, (b) static pull-in behavior of the micro-relay.

elastic unloading of a flat punch), until a minimum-level load $F_m$ is reached. If the contact radius $a$ is larger than the minimum stable radius $a_{min}$, the area of real contact begins to decrease till $a = a_{min}$, at which brittle separation occurs [31]. This model explains the gradual increase in $R_{ON}$ (as $V_{GB}$ is reduced to below $V_{RL}$) before the moment when separation occurs; this phenomenon will be revisited in more depth in Chapter 5.

The commercial finite-element-analysis (FEA) tool *COMSOL Multiphysics* is used to study the static pull-in behavior of micro-relays. The $Al_2O_3$ layer deposited by atomic layer deposition (ALD) has an intrinsic tensile stress of 200 MPa [32], and it is assumed to have no stress gradient. In contrast, the poly-SiGe film has an average compressive stress of −100 MPa (approximated using an array of fixed-fixed beams) and also has 100 MPa/μm linear stress gradient in the thickness direction. The bending moment caused by the poly-SiGe/$Al_2O_3$ bi-layer stress difference (negative gradient) dominates the one caused by the positive stress gradient within the poly-SiGe film. This net bending moment results in a vertical deflection of the movable electrode and the suspension beams upon release, as shown in Fig. 2–5 (a). The initial actuation gap is increased due to this warpage, which increases $V_{PI}$ according to Eq. 2–1. Note that the spring stiffness ($k$) can be augmented by the biaxial residual (tensile) stress, further increasing $V_{PI}$ [30]; this effect is captured by the COMSOL simulation as well. Fig. 2–5 (b) shows the simulated static pull-in behavior of relays with *vs.* without residual stress and stress gradient. $V_{PI}$ for the ideal case is 7.1 V, and for the realistic case with residual stress and stress gradient it is projected to increase to approximately 11.6 V, which matches the experimental results closely.

### 2.3.2 Frequency Response

Fig. 2–6 (a) shows the simulated out-of-plane motion of a logic micro-relay (with $L_{BEAM}$ = 9 μm) in its fundamental vibration mode, corresponding to a mechanical resonant frequency of 1.215 MHz. Fig. 2–6 (b) presents narrow-band frequency characteristics

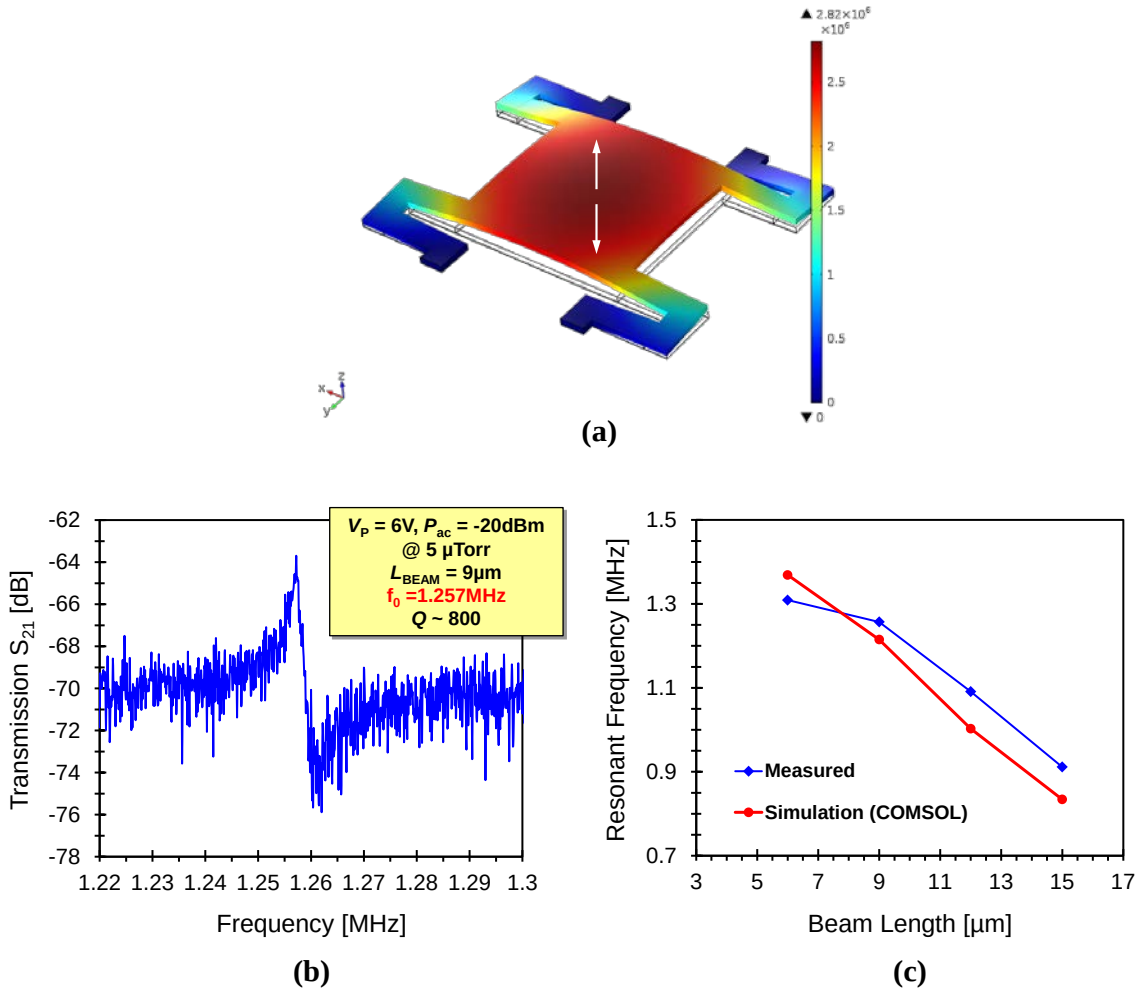



Figure 2-6. (a) First vibration mode shape of the micro-relay. (b) Measured narrow-band frequency response. (c) Comparison between simulated and measured fundamental resonant frequencies.

measured using a vector network analyzer (VNA) for a micro-relay (same $L_{BEAM}$); the measured resonant peak is at 1.257 MHz and the quality factor $Q$ is about 800.

Poly-SiGe MEMS resonators have been reported to have $Q$ values in excess of 20,000 [33]. The micro-relay is not optimized to operate with minimum energy loss, and its $Q$ is possibly limited by interface losses due to the composite structure (poly-SiGe/$Al_2O_3$). A large $Q$ value generally results in longer settling time due to ringing upon turn-off [30]; therefore, low quality factor is favored for faster operation as in a digital switch. Fig. 2–6 (c) compares measured *vs*. simulated dependence of the fundamental resonance frequency as a function of $L_{BEAM}$. It can be seen that the measured results agree well with the modeling results obtained with COMSOL.

# Chapter 3

# Reliability Characterizations of the Micro-relays

To be practical for integrated circuit (IC) applications, micro-relays must operate with sufficient endurance and adequately low ON-state resistance ($R_{ON}$). For embedded microcontroller applications, a logic switch should operate reliably for 10 years at 100 MHz clock frequency with a 0.01 average transition probability, which corresponds to approximately 300 trillion ($3\times10^{14}$) switching cycles. In this chapter, we will investigate various failure modes and related mechanisms that can limit the reliability of electrostatically actuated micro-relays with metallic contacting electrodes.

## 3.1 Pull-in Voltage Stability

One important reliability metric for logic micro-relays is the stability of the pull-in voltage, $V_{PI}$. A change in $V_{PI}$ directly alters the overdrive voltage ($V_{OV} = V_{GS} - V_{PI}$) and hence the switching delay. Relaxation of the intrinsic residual stress within the thin-film structural layer, plastic deformation under large strain, and fracture can all detrimentally affect the integrity of an electro-mechanical transducer (especially if it has flexural components) and thereby $V_{PI}$ and eventually cause mechanical failure. Dielectric charging and temperature variation also can result in $V_{PI}$ variation.

In this section we will focus on changes in $V_{PI}$ rather than the release voltage ($V_{RL}$) because the latter is dependent on the contacting surface properties and should be decoupled from the former. The logic micro-relays were all tested in a Lakeshore® TTPX vacuum probe station as shown in Fig. 3−1. Unless otherwise noted, in this sealed vacuum chamber, the temperature, pressure, and relative humidity are maintained at 300 K, ~5 μTorr, and ~0%, respectively.

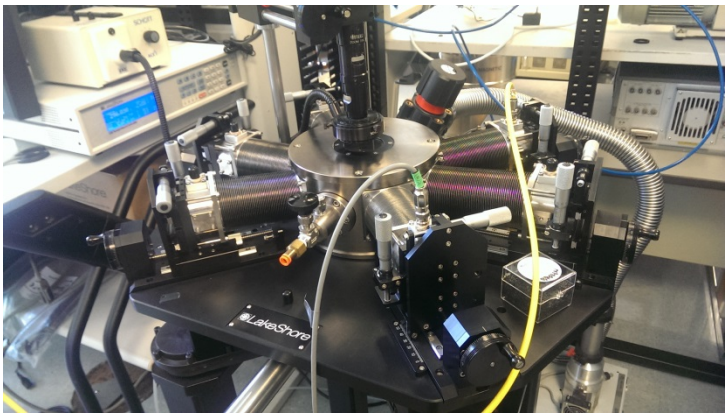



Figure 3-1. Lakeshore TTPX probe station.

### 3.1.1 Mechanical Aging/Fracture

Logic micro-relays may be subjected to rapid cyclic loading at frequencies up to 1 MHz. Due to grain boundaries and defects, polycrystalline thin films can suffer from stress corrosion cracking (SCC), which can be assisted by the formation of compressive native oxide [34]. Therefore, if the suspension beams of a micro-relay are subjected to significant mechanical strain (approaching the fracture strength) in the ON state, cracks can form and propagate with increasing number of ON/OFF switching cycles, reducing the effective spring constant ($k_{eff}$). Such structural fatigue would be manifest as a steady reduction in $V_{PI}$ over the device operating lifetime and can eventually result in catastrophic failure, limiting relay endurance. In this work, the effective length of the folded-flexure suspension beams is 34 μm and their maximum "tip" deflection is nominally 65 nm (essentially the as-fabricated contact gap), the maximum induced strain is less than 0.2%, so that fatigue should not be an issue for the micro-relays considered herein. To confirm this, a relay was cycled ON/OFF periodically using a 300 kHz square-wave Gate signal, swinging from 0 V to a positive peak voltage of $V_{PP}$, with the Source biased at 0 V and the Drain biased at 0.5 V.

Fig. 3−2 (a) shows how $V_{PI}$ and $V_{RL}$ evolve over the relay operating lifetime, for $V_{PP}$ = 18 V. $V_{PI}$ is seen to change only slightly (by 0.4 V) over 10 billion cycles, which is a good indication of fatigue-free operation. More significant changes are seen in $V_{RL}$, due to changes to the contacting surfaces that result in reduced surface adhesive force ($F_{adh}$) and hence smaller hysteresis voltage ($V_{hysteresis} = V_{PI} - V_{RL}$). Fig. 3−2 (b) compares the surface topologies for a fresh contact *vs*. a cycled contact (after $10^{10}$ ON/OFF cycles), and a slight decrease in root-mean-square (RMS) surface roughness ($R_q$) is observed. Asperity blunting increases the real contact area and hence should increase $F_{adh}$. A possible explanation for the observed reduction in $V_{hysteresis}$ is that contact surface oxidation reduces surface energy and hence decreases $F_{adh}$ (will be discussed in Section 3.2 and Chapter 5). More detailed discussions on the evolution of metal contact surface

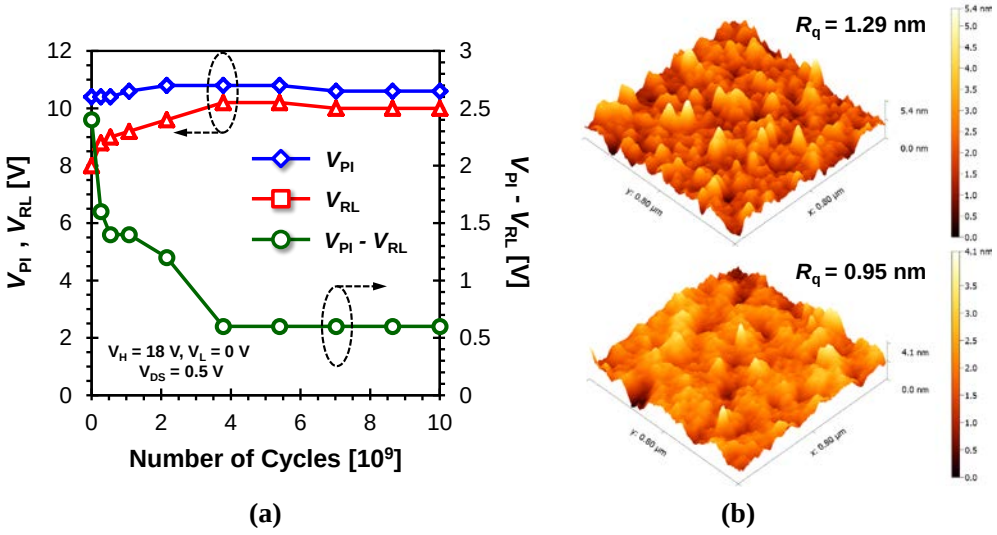



Figure 3-2. (a) Evolution of $V_{PI}$, $V_{RL}$ and hysteresis voltage with number of ON/OFF switching cycles. (b) Atomic force microscopy images of metal contact surfaces from a fresh relay ($R_q$ = 1.29 nm) *vs.* a cycled relay ($R_q$ = 0.95 nm).

properties with the number of hot-switching cycles will be provided in Section 3.2 and Chapter 4.

### 3.1.2 Dielectric Charging

Another cause of $V_{PI}$ instability is charge-trapping in the insulating dielectric layer between the gate and body electrodes induced by an applied voltage across this layer. (In the ON state, this layer must sustain the Source-to-Body voltage and Drain-to-Body voltage within the narrow channel region, cf. Fig. 3−3 (a).) A sufficiently large density of trapped charge can alter $V_{PI}$ and $V_{RL}$ such that the relay is stuck on or cannot be actuated on, depending on the polarity of the trapped charges.

Charges can be injected into the dielectric layer from the channel. Over time, these can diffuse within the dielectric layer into the regions between the gate and body electrodes to affect $V_{PI}$ and $V_{RL}$. The electrical and mechanical properties of the dielectric layer each can directly impact the rate of charge-trapping. PECVD nitride ($Si_3N_4$) and silicon-dioxide ($SiO_2$) have been used extensively in RF MEMS switches as post-metallization dielectrics, but their applications are limited for reliability reasons due to high defect density. The UC Berkeley Marvell Nanofabrication Laboratory (Nanolab) has the capability to conformally deposit $Al_2O_3$ thin films by atomic layer deposition (ALD), which is advantageous for logic relay technology for the following reasons: $Al_2O_3$ has a larger dielectric constant (9 vs. 3.9 for $SiO_2$ and 6.5 for $Si_3N_4$) which provides for higher electrostatic actuation force; $Al_2O_3$ is resistant to HF vapor (whereas $SiO_2$ and $Si_3N_4$ are attacked by HF vapor) which is used for the structural release process; ALD provides for higher-quality thin films (vs. PECVD). As shown by Allers *et al.* [35], ALD $Al_2O_3$ also provides for the lowest leakage current density among candidate dielectric

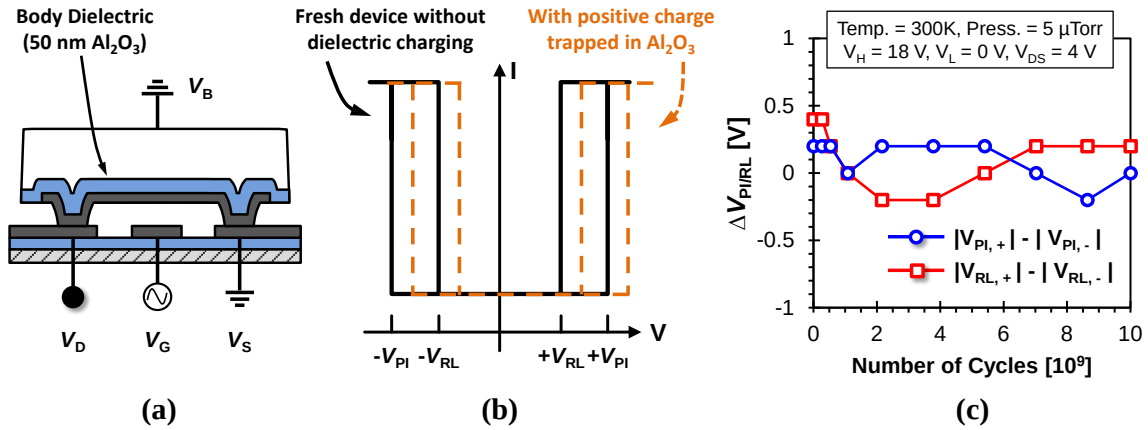



Figure 3-3. (a) Schematic cross-section along the channel region of the logic relay in ON state, showing how a voltage difference can develop across the body dielectric layer. (b) Illustration of the Drain-to-Source current ($I_{DS}$) *vs.* Gate-to-Body voltage ($V_{GB}$) characteristic, showing how trapped charge in the body dielectric would cause a shift, resulting in asymmetric (about $V_{GB}$ = 0 V) switching voltages. (c) Difference between measured $|V_{PI}|$ values or between measured $|V_{RL}|$ values.

materials ($SiO_2$, $Si_3N_4$ and $Ti_2O_5$). Therefore, ALD $Al_2O_3$ is used as the body dielectric material for the micro-relays in this work.

To investigate the potential issue of charge trapping in the $Al_2O_3$ dielectric layer, a micro-relay was cycled ON/OFF periodically using a 300 kHz square-wave Gate signal, swinging from 0 V to a positive peak voltage of 18 V, with the Source biased at 0 V and the Drain biased at 4 V. The cycling was interrupted periodically to monitor the values of the positive and negative pull-in voltages ($V_{PI,+}$ and $V_{PI,–}$ respectively) as well as the positive and negative release voltages ($V_{RL,+}$ and $V_{RL,–}$ respectively) using the parameter analyzer. Any charge trapping within the dielectric layer would have opposite effects on $V_{PI,+}$ *vs.* $V_{PI,–}$ (and on $V_{RL,+}$ *vs.* $V_{RL,–}$) so that the difference between $|V_{PI,+}|$ and $|V_{PI,–}|$ (and the difference between $|V_{RL,+}|$ and $|V_{RL,–}|$) would deviate from 0 V with the number of cycles as shown in Fig. 3−3 (b). Fig. 3−3 (c) shows how $|V_{PI,+}| – |V_{PI,–}|$ and $|V_{RL,+}| – |V_{RL,–}|$ evolve with the number of ON/OFF cycles. The relatively small values and non-monotonic behavior of these differences indicate that dielectric charging is not an issue for the operating voltage conditions used in this study.

In order to maximize the ON-state capacitance $C_{ON}$, a fairly large dielectric contact (usually metal-to-dielectric contact) area is employed in conventional RF capacitive switches, which enhances the probability of charge-trapping, assuming a fixed areal density of traps. The logic micro-relay herein uses a dimpled contact design, which prevents direct contact of the underlying actuation (gate) electrode with the dielectric layer underneath the movable (body) electrode, *i.e.* the body dielectric and the gate metal electrode are separated by an air gap even when the relay is in the ON state. The dielectric contact area is simply the channel area (58 $\mu m^2$ for a standard design). The relatively small dielectric contact area also helps to minimize dielectric charging in the micro-relays.

Ideally, the maximum voltage drop that the body dielectric would need to sustain is $V_{DD}$. In principle, a relay can be designed to operate with a gate voltage swing as small as $V_{hysteresis}$, so that $V_{DD}$ can be as low as $V_{hysteresis}$. For the relays studied in this work, the electric field within a 50 nm-thick dielectric layer would be less than 0.8 MV/cm for $V_{DD}$ < 4 V. In general, the dielectric layer thickness can be increased in order to reduce the electric field across the thin film.

### 3.1.3 Temperature Effects

Due to differences between the thermal expansion coefficients of the structural film materials and the substrate, internal stress within micromachined structures can be dependent on temperature. As a result, a temperature-induced change in $V_{PI}$ is closely related to the linear coefficient of thermal expansion (CTE). Thermally induced variation can be a concern for stable device operation, as integrated circuits should operate reliably within a temperature range from −40˚C to +80˚C.

Due to CTE mismatch, out-of-plane deflection (hence $V_{PI}$) can change with the temperature. Material properties for the micro-relay structural film used in this work are summarized in Table 3−1. Both Poly-SiGe and $Al_2O_3$ have a larger CTE than the Si substrate ($2.16\times10^{-6}$/K). As a result, an increase in temperature should lead to increased compressive stress exerted by the fixed anchors, while a decrease in temperature should

Table 3-1. Membrane material properties.

| | Poly-SiGe | $Al_2O_3$ |
|---|---|---|
| Thermal expansion coefficient $\kappa$ ($10^{-6}$/K) | 4.13 | 5.4 |
| Young's modulus $E$ (GPa) | 160 | 400 |
| Poisson ratio | 0.22 | 0.22 |

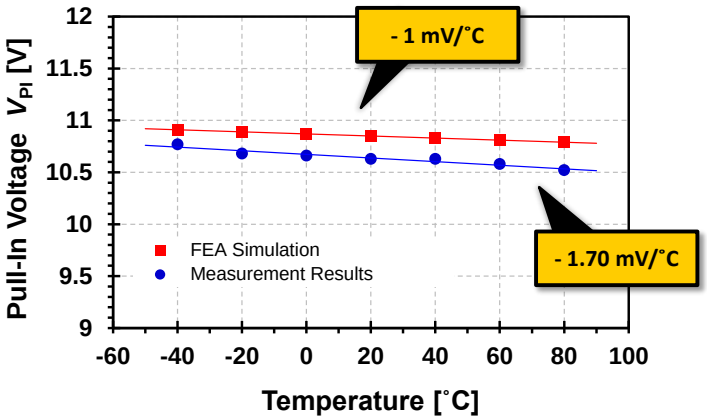



Figure 3-4. Simulated *vs.* measured $V_{PI}$ as a function of temperature.

lead to less compressive (or more tensile) stress in the structure. Measured $V_{PI}$ is plotted as a function of temperature in Fig. 3−4; the temperature coefficient (TC) is −1.70 mV/˚C within the desired operating temperature range (−40˚C to 80˚C). This relatively small dependence can be attributed to the following two factors: 1) relatively small CTE mismatch between the structure and the substrate, and 2) the folded-flexure suspension beam design relieves the impact of stress within the structural film.

Let us now consider the case for the threshold voltage ($V_T$) of a metal-oxide-semiconductor field-effect transistor (MOSFET), for comparison. The Fermi potential is given by

$$\Phi_F = \pm \frac{k_B T}{q} \ln\left(\frac{N_A}{n_i}\right), \tag{3.1}$$

where $n_i$ is the intrinsic carrier concentration which is also temperature dependent [36]:

$$n_i^2 = 3.9 \times 10^{16} \times T^{3/2} \exp\left(\frac{-E_g}{2k_B T}\right) \tag{3.2}$$

It can be seen that the Fermi potential varies with temperature. Depending on the dopant concentration and other device parameters, the TC is usually about ±2 mV/˚C. Although the two logic switch devices have similar temperature coefficients, thermal variation poses a greater challenge for the MOSFET because $V_T$ is approximately 300 mV whereas for the relay $V_{PI}$ exceeds 5 V. Also, the off-state leakage of a MOSFET varies exponentially with $V_T$, whereas it does not vary with $V_{PI}$ (so long as $V_{RL} > 0$). In conclusion, the very small dependence of $V_{PI}$ on temperature is not a major reliability concern. A corrugated structure could be implemented if necessary to minimize thermally induced variation, due to reduced bending moment [37].

## 3.2 Contact Resistance Stability

Another crucial reliability metric for logic micro-relays is the stability of the ON-state resistance, $R_{ON}$. $R_{ON}$ dictates the RC time constant and thus the electrical delay in logic circuits.

### 3.2.1 Tungsten as the prototype contact material

Since high endurance is a requirement for IC applications, contacting electrode materials with Mohs hardness > 6 are preferred since a hard material can better withstand repeated impact with minimal physical wear. For a contact radius greater than the electron mean

free path, the Maxwell spreading resistance model can be used to calculate the constriction contact resistance (neglecting surface contamination). The contact resistance $R_c$ is described by the following equation:

$$R_C = \frac{\rho}{2a_f}, \tag{3.3}$$

where $\rho$ is the resistivity and $a_f$ is the contact radius. The contact radius can be obtained using an asperity deformation model

$$a_f = \sqrt{\frac{F}{\pi H}}, \tag{3.4}$$

where $F$ is the applied force, $H$ is the hardness of the material. Eqn. (3.3) predicts that hard metals will result in higher contact resistance than soft metals, for comparable contact force. This is not an issue for logic relays, because they are used to charge or discharge relatively small nodal capacitances. $R_{ON}$ can be as high as 10 kΩ for a 100 fF load capacitance ($C_{LOAD}$), because the throughput of an optimally designed relay-based digital IC is limited by the mechanical pull-in time (typically ~ 10 ns for nanometer-scale relays, and ~1 μs for the relays studied in this work) rather than the electrical charging delay ($R_{ON} \times C_{LOAD}$) [9]. In addition to physical wear, atomic diffusion at the contacting points enhanced by Joule heating is a concern because it can lead to increased contact adhesive force so that the relay eventually becomes stuck on, *i.e.* $V_{RL}$ falls below 0 V. Given these concerns, refractory metals are good candidate electrode materials for logic relays. Tungsten (W) was used as the electrode material in the first prototype micro-relays because of its high hardness, high melting point as a refractory metal, and resistance to arc discharges (as tungsten has the highest minimal arcing current among the most common/important contact materials [38]) which is a common cause of material transfer.

Although W electrodes are more resistant to mechanical wear, they are also more susceptible to chemical reaction, in particular, oxidation [38]. Surface oxide formation increases $R_{ON}$ and eventually can result in circuit failure (when the electrical delay is comparable to or greater than the mechanical switching delay). Oxidation of exposed W electrode surfaces occurs if there is any ambient oxygen, and the rate of oxidation increases exponentially with increasing temperature. When a freshly released relay is conducting current in the ON state, physical contact between the conducting electrodes is made at multiple asperities, since the electrode surfaces are not perfectly smooth; Joule heating occurs in the presence of non-zero drain-to-source potential difference ($V_{DS}$). When the relay is turned OFF, the electrode surfaces become separated and hence are exposed so that oxidation can occur most rapidly at those heated asperities [39]. Subsequently, when the relay is turned on again, $R_{ON}$ will be larger due to the surface oxide layers. As the surface oxide layers become thicker with exposure time and/or the

number of ON/OFF cycles, oxygen can diffuse more easily (through the oxide layers) to the W surfaces at the contacting asperities, exacerbating the oxidation problem.

### 3.2.2 Testing Setup

$R_{ON}$ was monitored using the resistive-load inverter test setup as depicted in Fig. 3−5 (a). To study $R_{ON}$ stability, a square-wave voltage waveform $V_{DRIVE}$ with 100 ns ramp-up/ramp-down times (this was achieved by a 2 kΩ series resistor between the signal generator and the gate terminal to protect the devices from potential ESD damage) is used to drive the gate electrode, causing the relay to turn ON and OFF periodically. The amplitude of $V_{DRIVE}$ is set at 15 V, which is about 1.5 times the relay pull-in voltage. The frequency and duty cycle of $V_{DRIVE}$ were varied to separately adjust the ON-time and OFF-time per cycle from device to device. Details of the splits are summarized in Table 3−2. The drain electrode is connected to the power supply ($V_{DD}$) through a load resistor ($R_L$), while the source electrode is grounded. When the relay is OFF, the drain voltage is at $V_{DD}$; when the relay is ON, the output voltage ($V_{OUT}$) at the drain is dictated by the voltage divider formula: $V_{OUT} = V_{DD} \cdot (R_{ON} / (R_{ON} + R_L))$ shown in Fig. 3−5 (b). Thus, the evolution of $R_{ON}$ with the number of ON/OFF cycles can be derived from the value of $V_{OUT}$ with each switching cycle. Testing was halted when $R_{ON}$ exceeded the upper limit of 10 kΩ for a reasonable circuit performance. Notice that all the devices were still functional after the cycling test.

### 3.2.3 Results and Discussion

Fig. 3−6 (a) shows the evolution of $R_{ON}$ with the number of switching cycles for relays driven at various frequencies and duty cycles such that their OFF-times per cycle are all 20 μs. It can be seen that $R_{ON}$ stability degrades with increasing ON-time per cycle. This

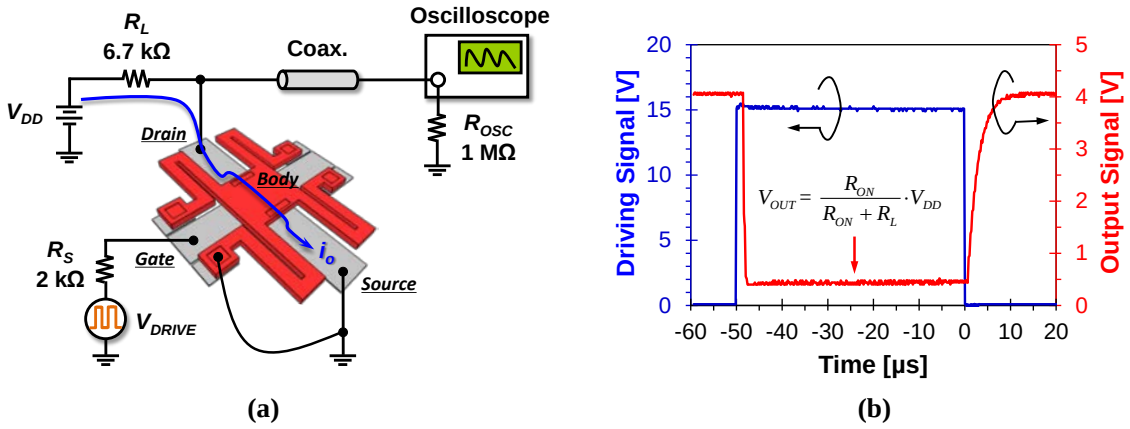



Figure 3-5. (a) Schematic showing the setup for monitoring micro-relay ON-state resistance ($R_{ON}$) in this work. (b) Measured input and output (the drain terminal) voltage waveforms. This figure was taken with a driving signal of 10 kHz.

is because Joule heating occurs at the contacting asperities in the ON-state; the volume of material heated increases with the ON-time, so that it takes longer for the contacting surfaces to cool after the relay is turned OFF, resulting in more thermal oxidation of the contacting surfaces. Fig. 3−6 (b) shows the evolution of $R_{ON}$ with the number of switching cycles for relays driven at various frequencies and duty cycles such that their ON-times per cycle are all 20 µs. It can be seen that $R_{ON}$ stability degrades with increasing OFF-time per cycle. This is also due to increased oxide formation: when a relay is in the off state, the contacting surfaces are exposed to residual oxygen in the environment; the longer the OFF-time, the more oxide that forms. In general, metal contact stability depends on not only the number of switching events, but also ON/OFF time of each operation cycle.

The micro-relay electrodes were examined in a scanning electron microscope (SEM) before and after ON/OFF cycling, and exhibited no major change in topography. Similar to the results presented in section 3.1.1, the cycled W electrodes were found to have slightly smaller surface roughness (possibly due to mechanical wear) which should result in lower contact resistance due to an increase in real contact area. It is likely that the

Table 3-2. Details of the waveform used to generate different ON/OFF time combinations.

| | Duty Cycle (%) | ON Time (µs) | OFF Time (µs) |
|---|---|---|---|
| 1 kHz | 2 | 20 | 980 |
| | 98 | 980 | 20 |
| 5 kHz | 10 | 20 | 180 |
| | 90 | 180 | 20 |
| 25 kHz | 50 | 20 | 20 |

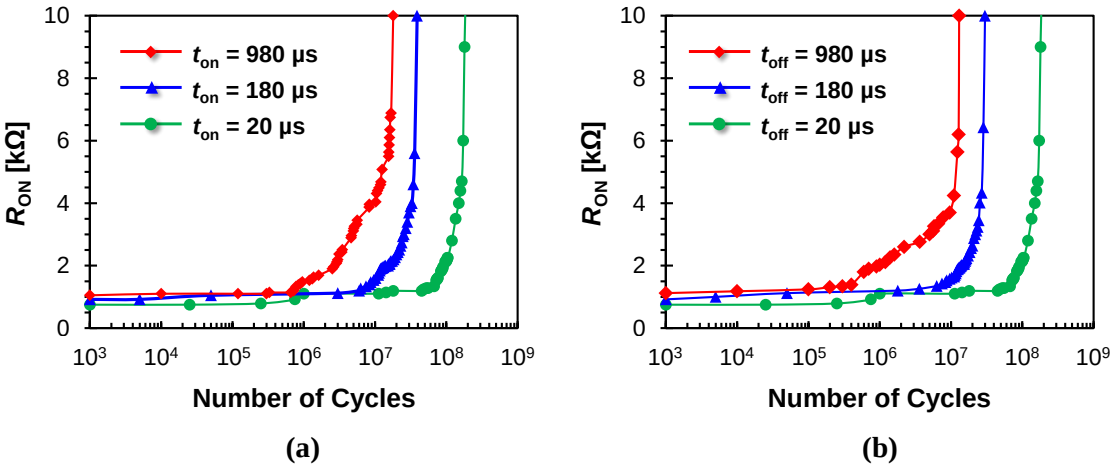



Figure 3-6. (a) Evolution of $R_{ON}$ with the number of ON/OFF switching cycles, for relays driven at various frequencies and duty cycles such that their OFF-times per cycle are all 20 µs. (b) Evolution of $R_{ON}$ with the number of switching cycles, for relays driven input at various frequencies and duty cycles such that their ON-times per cycle are all 20 µs.

chemical properties of the contacting surfaces after cycling are altered. Auger Electron Spectroscopy (AES) was used to analyze the elemental composition of the contacting surface, for devices with low $R_{ON}$ (fresh) *vs*. high $R_{ON}$ (after $5\times10^7$ ON/OFF cycles). From the AES analysis one can determine the principal chemical agents that reacted with the W surface and the relative concentrations of these contaminants. By comparing the Auger spectra in Fig. 3-7 (a) and Fig. 3-7 (b), it can be seen that the W peaks are significantly attenuated for the cycled device. The higher [O]/ [W] ratio is indicative of surface oxidation. Analysis of an electrode from a cycled device after thin (5 nm) surface-layer removal (via ion milling) in Fig. 3-7 (c) shows the lowest [O]/[W] ratio among the 3 cases, as expected (since there exists native oxide on the W electrode surfaces of an un-cycled device). Tungsten and oxygen concentrations extracted from the Auger spectra and their ratios are summarized in Table 3-3 for the three cases.

Based on these results, one would conclude that shorter ON-time as well as shorter OFF-time should provide for more stable $R_{ON}$ with respect to the number of ON/OFF switching cycles. To verify this, relays were driven at different frequencies (1 kHz, 5 kHz, 25 kHz and 60 kHz) with the same duty cycle (50%). The allowable driving frequency that can be used for the measurements is only up to ~25 kHz, which is limited by the electrical RC delay due to the load parasitic capacitance (~250 pF) from the embedded miniature coaxial cable in the manipulator arms and the external coaxial cable. As shown in Fig. 3-8, a simple unity-gain buffer based on OPA-633 [41] was employed at the output port of the probe station, which effectively removed ~150 pF of coaxial capacitance. However, it could not be placed right at the tip end because there was not much room in the chamber to insert the circuit board, and routing for the power supply was not trivial. As a result, the inverter circuit still drives a large load capacitance ~100

Table 3-3. Atomic concentration from Auger spectra.

| Figure | [O] | [W] | [O]/[W] |
|---|---|---|---|
| 3-7 (a) | 35±3.5 | 15±1.5 | 2.33±0.33 |
| 3-7 (b) | 25±2.5 | 1±0.1 | 25±3.54 |
| 3-7 (c) | 15±1.5 | 45±4.5 | 0.33±0.05 |

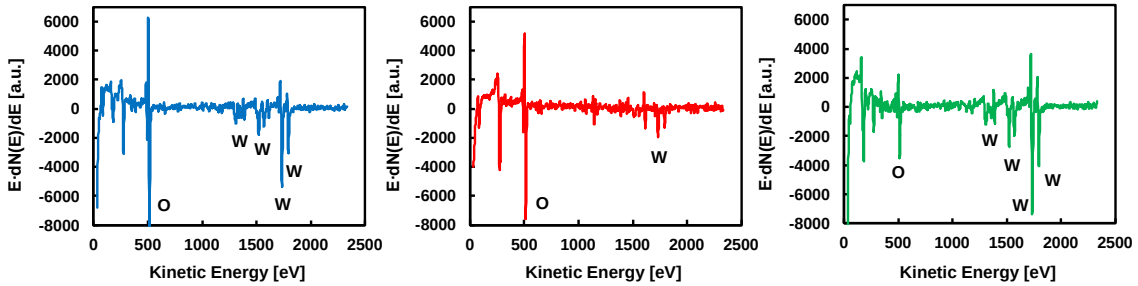



Figure 3-7. AES spectra of the tungsten electrode surface (a) from a fresh relay, (b) from a relay that went through $5\times10^7$ on/off cycles, (c) from a relay that was cycled $5\times10^7$, after ion milling to remove 5 nm from the surface.

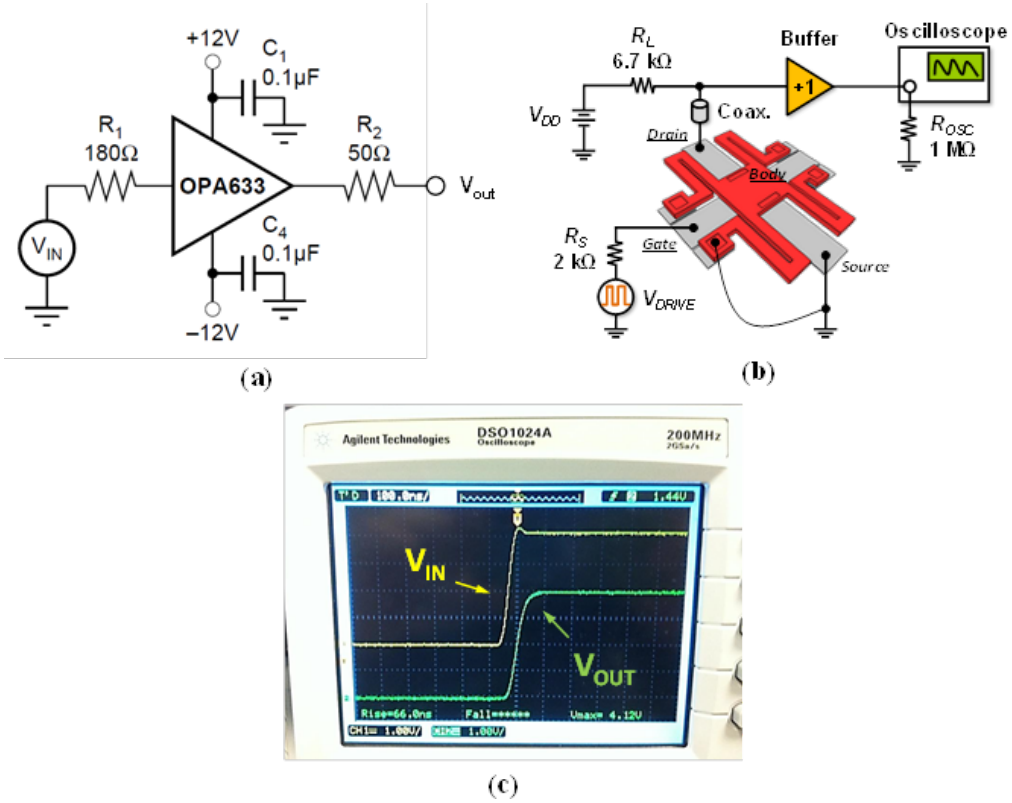
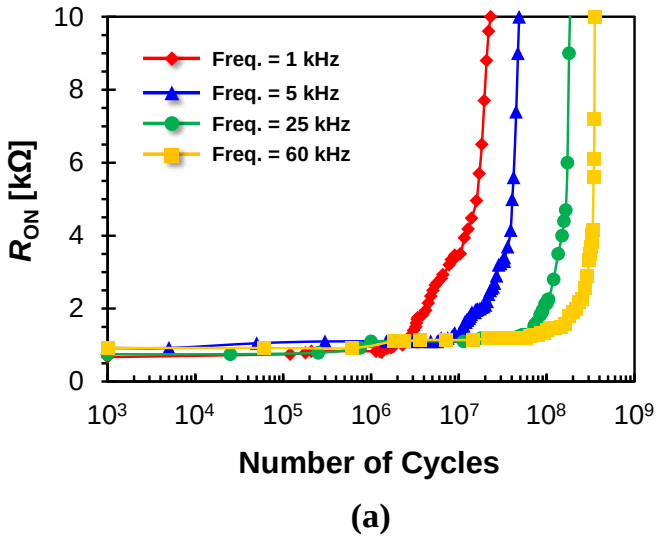



Figure 3-8. (a) Schematic of the buffer amplifier implemented with OPA-633. (b) Improved test setup with the buffer amplifier. (c) Output waveform verifying the functionality of the buffer amplifier.

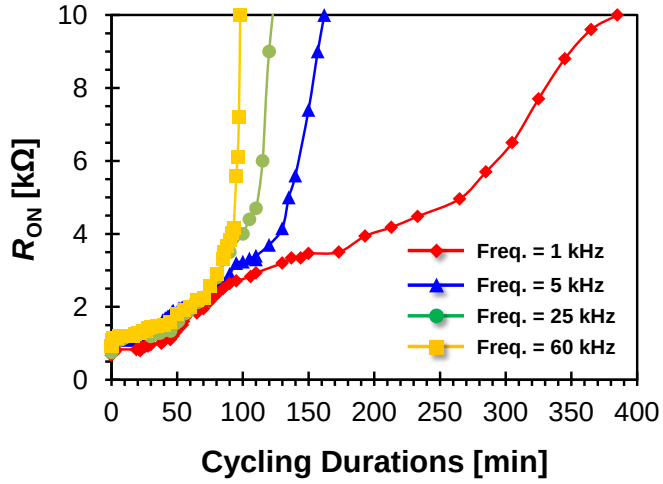
pF of the embedded coaxial cable. It should be noted that in an integrated relay-based logic circuit, the output node only needs to charge/discharge $C_{GB}$ of the micro-relays in the following stage, along with the interconnect capacitance (overall ~ 100 fF) − which is about 3 orders of magnitude smaller than the parasitic capacitance in the non-ideal test setup − so that the electrical delay would not limit the device operating frequency.

As shown in Figure 3-9 (a), $R_{ON}$ is indeed more stable, with respect to the number of switching cycles, under higher frequency operation. When the device is operated at 60 kHz, the contact resistance does not reach 10 kΩ until ~$3.5\times10^8$ cycles, which is one order of magnitude better than for operation at 5 kHz (~$2\times10^7$ cycles). However, with regard to lifetime (actual timespan of device operation within specifications), operating at higher frequency is not advantageous. As can be seen from the comparison in Figure 3-9 (b), the micro-relay operating at 1 kHz reaches 10 kΩ after 380 minutes, while the micro-relay operating at 60 kHz reaches 10 kΩ within 100 minutes. In other words, lifetime is degraded when a relay is operated at higher frequency.

Contact resistance variation ($R_{ON}$ instability) is therefore identified to be the reliability limiter for logic micro-relays. In the following chapter, methods for enhancing metal contact stability are discussed.




**(a)**




**(b)**

Figure 3-9. Evolution of $R_{ON}$ at frequencies 1 kHz, 5 kHz, 25 kHz and 60 kHz (all with 50% duty cycle) (a) with the number of ON/OFF switching cycles (in log scale) (b) with cycling time (in linear scale).

# Chapter 4

# Methods of Improving Metal Contact Stability

Metal contacts are critical components of a logic relay, as their properties affect ON-state resistance ($R_{ON}$) as well as the useful device operating lifetime. In this chapter, $R_{ON}$ degradation mechanisms and approaches to mitigate them are investigated.

## 4.1 Contact Force and Reliability

Since the contacting surfaces are not perfectly smooth (cf. Fig. 2(b)), physical contact in the ON state is made between the conducting electrodes only at a relatively small number of asperities. Higher contact force can provide for increased real contact area and hence lower contact resistance. A certain amount of force is required to achieve a clean metal contact with stable resistance; once the (material dependent) threshold level of force has been reached, the resistance decreases only slightly upon further increase in contact force [42]. It has been postulated that contact closure events can facilitate mechanical breakdown of thin insulating films on electrode surfaces [42], [43]. A direct implication

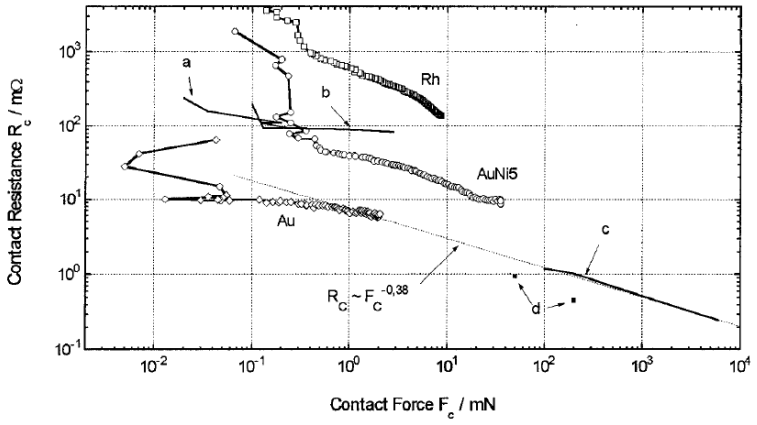



Figure 4-1. Measured characteristic contact resistance versus applied contact force for various metals [42].

of this is that the contact force should deterministically affect $R_{ON}$ stability for tungsten (W) electrodes, since surface contaminants appear to dominate $R_{ON}$ for W electrodes.

Let us first consider the static contact force $F_{contact}$ in the ON state. $F_{contact}$ increases with the electrostatic actuation force, which increases super-linearly with increasing gate driving voltage:

$$F_{contact} = \frac{1}{N_C}(F_{elec} - F_{spring}) + F_{adh}$$
$$= \frac{1}{N_C}\left(\frac{V_{GB}^{\,2}}{2}\frac{\varepsilon_0 A}{\left(g_0 + \left(\frac{t_{ox}}{\varepsilon_r}\right) - g_d\right)^2} - k_{eff}\, g_d\right) + F_{adh} \quad (4.1)$$

where $N_C$ is the number of contacts, $g_0$ is the as-fabricated actuation gap thickness, $t_{ox}$ is the body dielectric thickness, $\varepsilon_r$ is the relative permittivity of the body dielectric, $A$ is the actuation area, and $g_d$ is the as-fabricated contact gap thickness (which is also the vertical displacement of the flexure beams). The total contact force is assumed to be distributed equally to each of the contacts.

$F_{contact}$ (ignoring the surface adhesion force) for the 4T relay (with 2 contacts) studied in this work is plotted *vs.* $V_{GB}$ in Fig. 4-2(a). Notice that, in comparison with Eqn. (4.1), finite-element simulation (Coventorware®) predicts a greater increase in $F_{contact}$ with increasing gate voltage, because it accounts for deformation of the actuated electrode in the ON state which results in a smaller actuation air gap thickness.

To study the effect of contact force on contact resistance and its evolution, $R_{ON}$ was monitored for different values of Gate driving voltage $V_{PP}$ at a driving frequency of 5

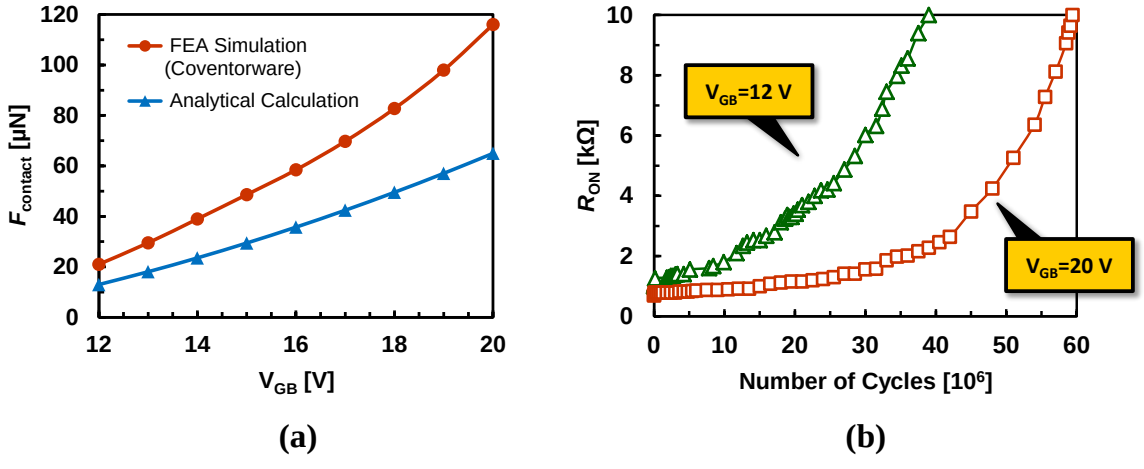



Figure 4-2. (a) Calculated contact force *vs.* $V_{GB}$ for a 4T relay. (b) Impact of Gate driving voltage on $R_{ON}$ stability, for a 4T relay.

kHz, with $V_{DD}$ = 4 V and $V_{GB}$ = 15 V. Improved $R_{ON}$ stability is seen for higher actuation force, as shown in Fig. 4-2(b). The device tested with an actuation voltage of 12 V reaches 10 kΩ in approximately 35 million cycles, whereas the one with 20 V actuation voltage exceeds the $R_{ON}$ maximum specification after 60 million cycles. This is consistent with the intuition that a native oxide film is easier to break physically with higher force. Another possible explanation is the change in the dielectric breakdown strength due to applied mechanical stress. The compressive stress exerted on the thin dielectric film (tungsten oxide in this case) in the ON-state can lead to reduction of charge-to-break down voltage, followed by the degradation of dielectric reliability [44].

Mechanical design can also affect the contact force. We will now examine the $R_{ON}$ stability for relays of three different designs: the six-terminal (6T) relay, the four-terminal (4T) relay, and the improved 4T relay. A 6T relay comprises two sets of channel/Source/Drain electrodes, with a total of four contacts, whereas the 4T relay comprises one set of channel/Source/Drain electrodes, with a total of two contacts. The 6T relay and the 4T relay have the same actuation area; thus the same amount of electrostatic force is applied to the movable structure. Due to the extra set of drain/source

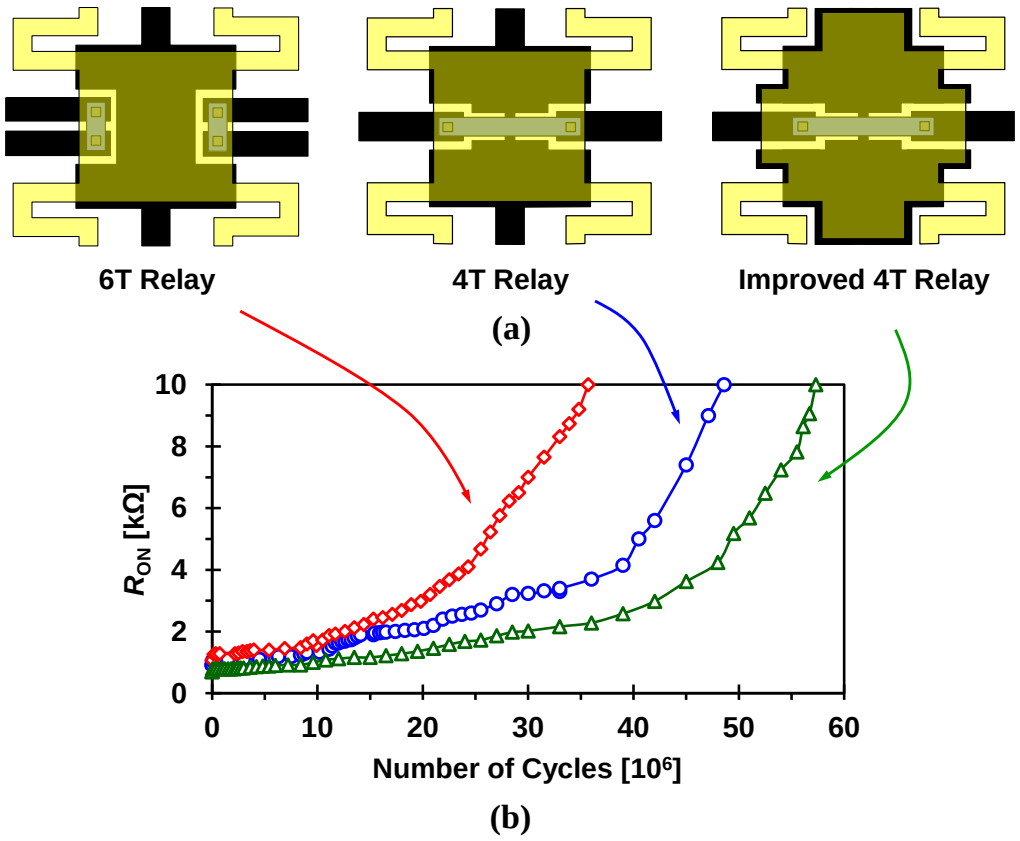



Figure 4-3. (a) Plan-view illustrations of the 4T relay, 6T relay and improved 4T relay structures studied in this work. The 6T relay comprises two sets of Channel/Source/Drain electrodes to allow for more compact implementation of complex logic circuits. (b) Comparison of $R_{ON}$ stability for a 4T relay *vs.* a 6T relay *vs.* an improved 4T relay operated with the same Gate driving voltage.

contacts, the contact force per contact is lower by a factor of two in a 6T relay. The improved 4T relay has ~60% larger effective actuation area, within the same device footprint (cf. Fig. 4-3(a)), which corresponds to a ~ 40% increase in the contact force compare to a regular 4T relay. In short, the ratio of contact forces on a single contact dimple for the 6T, 4T, and improved-4T relay designs is 0.5:1:1.6.

Fig. 4-2(b) compares $R_{ON}$ stability for 6T *vs*. 4T *vs*. improved 4T relays, under the same operating conditions. As expected, the relay designs which provide for higher contact force show better $R_{ON}$ stability. These results do not imply that $R_{ON}$ stability improves with increasing contact force indefinitely, however. Under very large contact forces (> 1 mN), other issues such as brittle fracture, fatigue and fretting could limit the endurance of the metal contacts.

## 4.2 Alternative Contact Material: Ruthenium

Another approach to improve $R_{ON}$ stability is to use an alternative material for the contacting electrode surfaces. Besides better immunity to the effects of surface oxidation, it is also desirable for the material to have similar mechanical properties as W, including high hardness, high yield strength, and a high resistance to physical wear.

### 4.2.1 Selection of Alternative Contact Material

The physical properties of candidate contact electrode materials are compared in Table 4−1. Gold is a noble metal, but its low hardness and low melting point make it susceptible to contact wear, stiction (excessive surface adhesion) and material transfer. Gold-nickel alloy (AuNi) provides a reasonable trade-off between electrical conductivity and hardness/adherence force [43]. Also AuNi has been shown to achieve stable contact properties under ~30 μN contact force [42], which would be adequate for a scaled micro-relay (since contact force also scales with device dimensions). Gold and its alloys are not compatible with CMOS processing technology, however. Therefore, AuNi is only suitable for stand-alone RF/analog switching (*vs*. integrated circuit) applications.

Titanium nitride (TiN) is widely used as a surface coating material in precision machinery and biocompatible implant parts (joints, hips) due to its low friction coefficient, excellent wear resistance and high chemical stability. TiN coating can effectively improve the durability of mechanical components that need to operate under repetitive physical impact, such as sliding bearings and other friction units. Ceramic materials in general are insulating, which restrict them from usage as electrical contacts. However, TiN exhibits moderate electrical conductivity that is only ~10 times lower than that of common metals used for electrical contact (c.f. Table 4−1). Requirement for contact resistance in logic microrelays is more relaxed than conventional RF switches, and ideally the resistance can be compensated with a thicker film.

Table 4-1. Physical properties of the potential contact metals [38].

| | **AuNi** | **TiN** | **Ru** | **Units** |
|---|---|---|---|---|
| Young's modulus, *E* | 130 [44] | 550 [46] | 430 | ( GPa ) |
| Estimated hardness (thin-film), *H* | 7 [44] | 30 [46] | 15.28 [48] | (GPa) |
| Electrical resistivity @ 20˚C, $\rho$ | ~12 [43] | 40-70 [47] | 6.71 | (μΩ·cm) |
| Melting point | ~1040 [43] | 2930 | 2350 | (°C ) |

Table 4-2. Recipes used for TiN deposition in Novellus® m2i sputtering system.

| Sample | **Ar Flow (sccm)** | **$N_2$ Flow (sccm)** | **Deposition Power (kW)** | **Temp. (˚C)** | **Back Bias (V)** | **Resistivity (μΩ-cm)** |
|---|---|---|---|---|---|---|
| #1 | 55 | 35 | 6 | 400 | 0 | 211 |
| #2 | 55 | 35 | 6 | 400 | -50 | 168 |
| #3 | 55 | 35 | 6 | 400 | -80 | 118 |
| #4 | 55 | 35 | 6 | 400 | -100 | 86 |

TiN thin films were deposited by physical vapor deposition (PVD) in a Novellus® m2i sputtering system. The nitrogen ($N_2$) and argon (Ar) gas flows in this DC reactive deposition system can be adjusted separately to control the film stoichiometry and properties. Table 4−2 summarizes the measured resistivity of TiN thin films for various deposition process conditions. A negative substrate bias was used to minimize contamination on the substrate surface. It can be seen that the resistivity is lowered as this bias voltage increases in magnitude. The resistivity of the sputtered TiN film with −100 V substrate bias is still about 4 times higher than that of sputtered W (experimental results from Chapter 2), however. Witvrouw *et al*. [49] showed that TiN is only slightly attacked under HF vapor etch at 35˚C (etch rate ~0.06 nm/min). However, pinholes were observed in a sputtered TiN film after ~20 minutes exposure to HF vapor in an Idonus® HF vapor phase etcher in the Berkeley Nanolab. The film was attacked by HF vapor such that its conductivity degraded significantly. These results may be due to differences in TiN thin-film stoichiometry and quality. Thus, TiN was determined to be incompatible with the established microrelay fabrication process, but it could be used for laterally actuated relays which are fabricated by first releasing the movable microstructures and then coating them with metal [50].

Generally speaking, platinum-group metals such as platinum (Pt), ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), and iridium (Ir) are chemically inert (especially resistant to oxidation and corrosion). Among these, Ru, Rh, Os and Ir are unique in that they can form conductive oxides [51]. The bulk resistivity of $RuO_2$ is 35 μΩ·cm [52], which is only 6 times higher than the bulk resistivity of Ru (6.71 μΩ·cm). $R_{ON}$ instability due to surface oxidation could be mitigated by employing these metals as contact materials. Ru has the advantage of high hardness/melting point (c.f. Table 4−1)

Table 4-3. Sputtering conditions for Ru thin film deposition.

| Ar Flow (sccm) | Pressure (mTorr) | RF Power (kW) | Dep. Rate (nm/min) | Resistivity (μΩ-cm) | Stress (MPa) |
|---|---|---|---|---|---|
| 137 | 5 | 1.4 | ~15 | ~22 | ~200 |

and is much less costly compared to the other metals [53]. In this work, Ru thin films were prepared using the Randex sputter deposition tool; the process parameters and results are summarized in Table 4−3. Sputtered Ru thin films were found to survive the HF vapor test with no degradation in resistivity or change in surface morphology. Therefore, Ru is investigated as an alternative contact material for micro-relays, in the following sections.

### 4.2.2 Integration Issues with Ru

Although Ru appears to be a promising candidate for achieving better $R_{ON}$ stability in logic micro-relays, its integration into the established fabrication process flow is not trivial. First, it is difficult to dry-etch Ru films. It has been shown that Ru dry etching in oxygen ($O_2$) plasma is effectuated by the formation of the volatile by-product $RuO_4$, and that this process can be facilitated by adding Ar and chlorine (Cl-) based gas to the $O_2$ plasma [54]. However, the use of $O_2$ plasma for Ru etching would require an additional hard mask layer since photoresist is rapidly removed during the Ru etch process [55]. In this work, a lift-off process is used avoid the need to dry-etch Ru. The metal lift-off process utilizes a bi-layer (DUV and LOR 3A) photoresist film to ensure clean patterned metal edges. The LOR 3A layer is undercut more than the DUV layer during the development process, which is beneficial for preventing direct contact of the sputtered metal film with the LOR 3A sidewall, resulting in smoother metal trace features. The Ru thin-film patterning procedure is as follows:

- Standard HMDS prime bake with program 1 at SVGCOAT6.
- Spin LOR 3A at 2000 rpm (targeting at a film thickness of 400 nm) [56].
- Soft-bake LOR 3A at 180˚C for 300 seconds (temperature can be adjusted to meet different undercut requirements).
- Spin DUV resist (program 1 at SVGCOAT6 without HMDS bake) followed by standard soft-bake and exposure in ASML DUV stepper.
- Standard post-exposure bake and develop using programs (8, 8) dedicated to DUV resist process at SVGDEV1.
- Ru thin-film sputter deposition.
- Lift-off using PRS3000 at 70˚C in an ultrasonic bath.

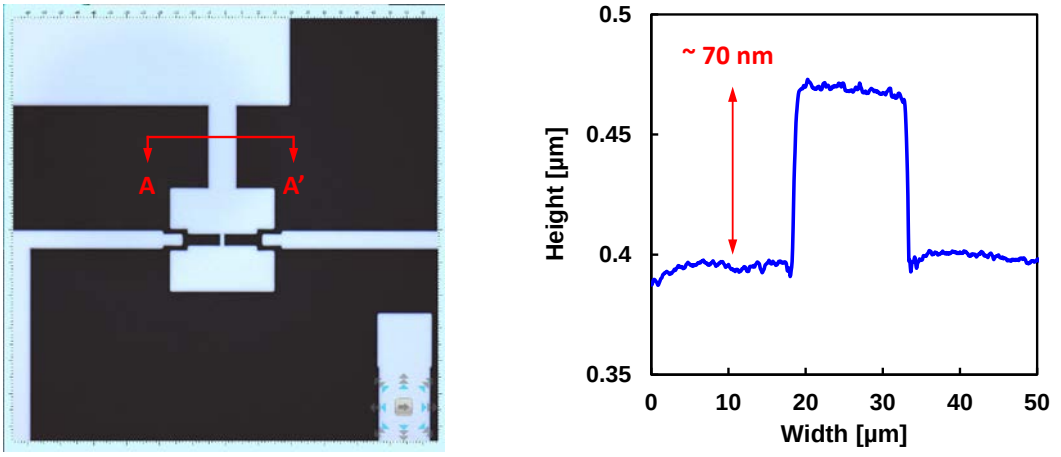



Figure 4-4. (a) Ru features (bottom electrodes) achieved with the lift-off process. (b) Step height measurement across A-A'.

Microscope image of metal patterns defined by lift-off process is shown in Fig. 4−4 (a). Fig 4−4 (b) presents the step profile along the A-A' cross-section measured with Alpha-Step IQ (Asiq) surface profilometer.

Another process integration issue is that sputtered Ru adheres poorly to $SiO_2$. Specifically, a sputtered Ru thin film peels off relatively easily without any external influences, not to mention under standard wafer cleaning processes such as quick-dump-rinse (QDR) and spin-rinse-dry (SRD). This practical problem poses a major challenge to the formation of the channel top electrode on top of the $SiO_2$ sacrificial layer. To promote adhesion of Ru, the surface of the $SiO_2$ was coated with an ultra-thin layer (0.94 nm measured using a Sopra spectroscopic ellipsometer) of titanium-dioxide ($TiO_2$) by atomic layer deposition (ALD, 30 cycles). Ru adheres better to the $TiO_2$ layer, which is later removed during the HF vapor etch microstructure release process. It was reported that thermal annealing of the $Ru/TiO_2/SiO_2$ stack under vacuum can further promote adhesion of Ru [55]. This extra annealing step is omitted from the lift-off metal film formation process, since the heat treatment would harden the photoresist and thereby make it difficult to remove afterwards.

### 4.2.3 Electrical Characteristics of Ru-contact Relays

The fabrication process flow for Ru-contact relays is identical to the one described in Chapter 2, except that the patterned metal layers are formed by a lift-off process rather than by reactive ion etching (RIE) as illustrated in section 4.2.2. Fig. 4−5 (a) shows the scanning electron microscope (SEM) image of a fabricated (released) 4T relay with Ru electrodes. Fig. 4−5 (b) shows typical measured current-*vs*.-voltage ($I_{DS}$-$V_{GB}$) characteristics for the Ru-contact relay with $V_B$=0 V and $V_{DS}$=1 V. Measured values of $V_{PI}$ and $V_{RL}$ are 12 V and 9V, respectively. $I_G$ is below 1 pA even for high gate overdrive.

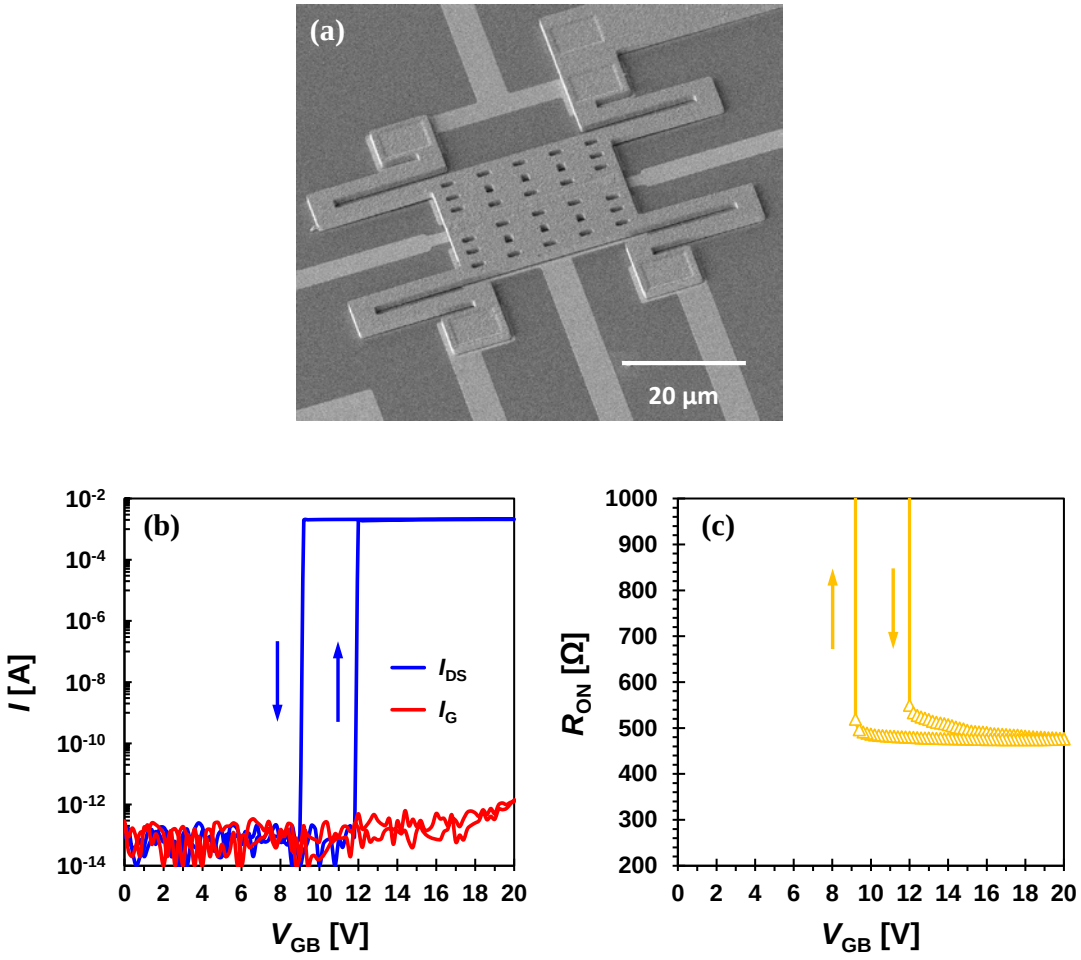



Figure 4-5. (a) SEM image of a released 4T relay with Ru contacting electrodes ($L_{BEAM}$ = 15 µm). (b) Measured $I_{DS}$-$V_{GB}$ characteristics of a 4T relay with Ru contacting electrodes, with $V_D$ = 1 V and $V_S$ = $V_B$ = 0 V. (c) $R_{ON}$ versus the gate-to-body voltage $V_{GB}$.

An on-state resistance of 480 Ω is achieved with Ru contacting electrodes as shown in Fig. 4−5 (c). This is not surprising since a sputtered Ru film has slightly smaller resistivity than a sputtered W film; also Ru has lower hardness than W (ref. Chapter 5), so that the real contact area is larger under the same load.

### 4.2.4 Reliability of Ru-Contact Electrodes

Cycling tests for Ru-contact micro-relays were performed using the same resistive-load inverter setup described in Chapter 3. Unless otherwise specified, the amplitude of the actuation voltage is set to be 15 V, the supply voltage $V_{DD}$ is set to be 4 V and the cycling frequency is fixed at 5 kHz. The characterizations are performed in a Lakeshore vacuum probe station with a controlled pressure of 5 µTorr.

$R_{ON}$ increases slowly but steadily with the number of hot-switching cycles. A sticking-like failure is observed after 5 million switching events. Although $R_{ON}$ remains below 10 kΩ after $5\times10^6$ cycles (c.f. Fig. 4−6 (a)), the output node does not fully swing back to $V_{DD}$ (4 V) when the micro-relay is turned off, and the off-state resistance $R_{OFF}$ is of the same order of magnitude as the on-state resistance, as shown in Fig. 4−6 (b). This simply means the open state is not reached, and the relay is now either permanently stuck down or the contacts are somehow shorted. Such a dramatic decrease in $R_{OFF}$ means an undesirable reduction in the $I_{ON}/I_{OFF}$ ratio, so that the micro-relay fails to operate well as a switching device.

To investigate the Ru-contact relay failure mechanism, cycled contacts (bottom electrodes) were examined by SEM. SEM images of the contacting surfaces of the drain

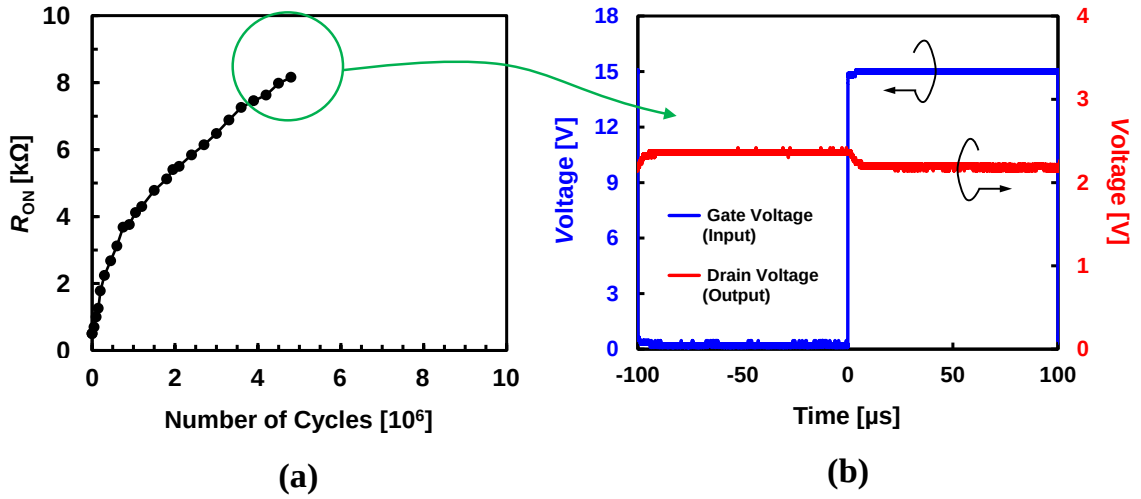



Figure 4-6. (a) Evolution of $R_{ON}$ in a Ru-contact 4T micro-relay with hot-switching cycles (plotted with a linear scale). (b) Output voltage waveform that indicates micro-relay operation failure.

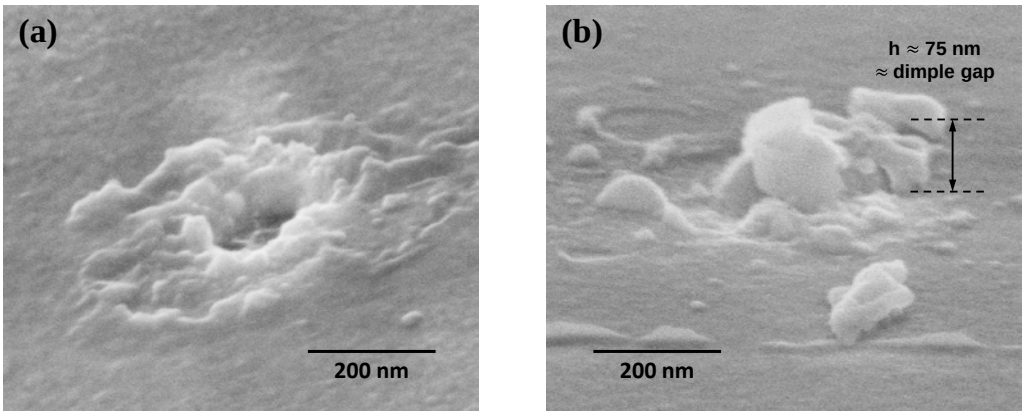



Figure 4-7. SEM micrographs (with 45˚ tilt) of the fixed (bottom) contact electrode surfaces after ~5 million hot-switching cycles: (a) drain electrode (b) source electrode.

electrode and the source electrode are shown in Figs. 4−7 (a) and (b), respectively. Intriguingly, a crater is seen in the drain electrode surface, while hillocks/flakes are seen on the source electrode surface. These surface topologies result in uneven contact in the ON state, reducing the real contact area and resulting in increased $R_{ON}$ as observed.

The measured height of the source electrode hillock is 75 nm, which is about the same height as the contact dimple gap as fabricated. Once the hillock on the source (and/or the material deposited at the edges of the crater on the drain) is large enough to occupy a substantial portion of the space between the channel contact dimple and the bottom electrode, it can short them together. From then on, and a current conduction path always exist between the top electrode and the bottom electrode regardless of the applied gate bias, and a change in the actuation voltage merely modulates the conductivity of the sandwiched material.

Material transfer due to arcing as a relay is turned OFF can be explained by the particle sputtering and deposition (PSD) model proposed by Chen and Sawa [57]. Since the electrode surfaces are not perfectly smooth, physical contact in the ON state is made at a few asperities; current only flows through these constriction points. As the load

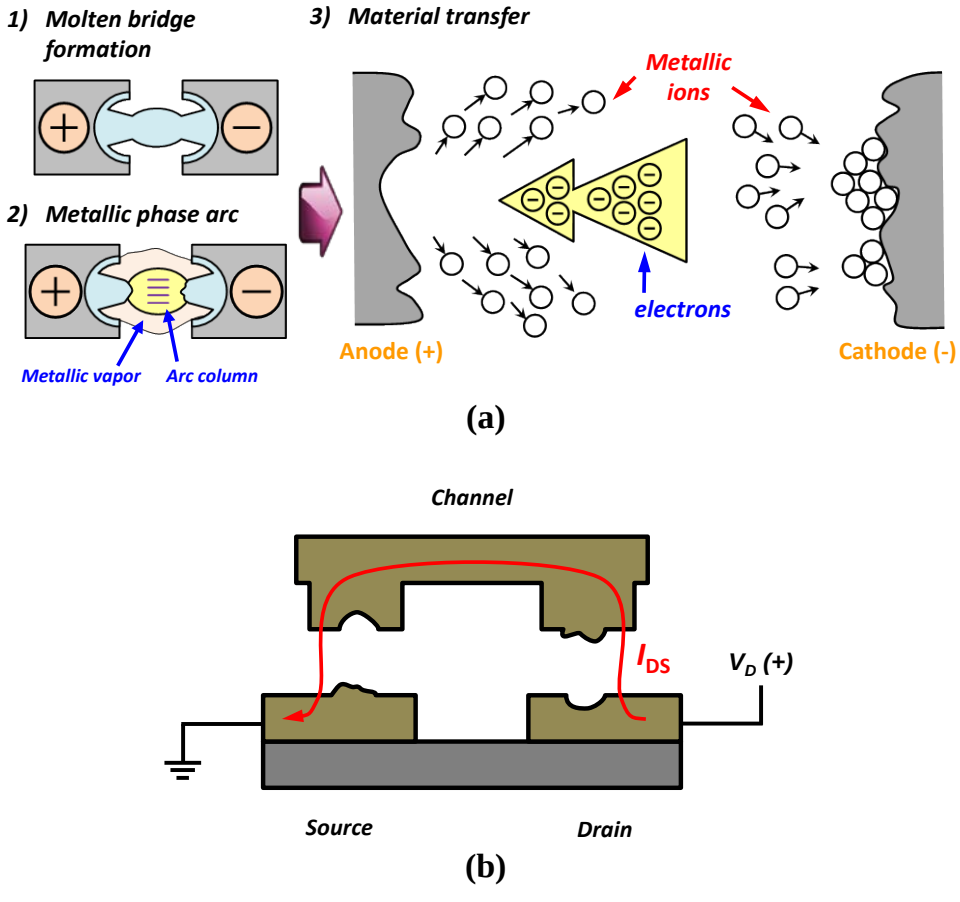



Figure 4-8. (a) Schematic illustration of arc formation explained by the PSD model [57]. (b) Schematic illustration showing the direction of material transfer between Ru electrodes in a 4T relay.

decreases, the area of the metal-metal contact drops (necking), and Joule heating increases rapidly. The softened metal is pulled into a molten bridge. Once the bridge is ruptured, the heated asperities serve as sources of thermal-field (T-F) electron emission. The electrons emitted from the hot cathode then get accelerated by the strong electric field and bombard the anode surface. The mobilized metal ions subsequently redeposit on the cathode surface. This process is illustrated in Fig. 4−8 (a).

Material transfer is recognized as one culprit for contact degradation. Based on the PSD model, the direction of material transfer should depend on the direction of the electric field, *i.e.* material transfer occurs from one contacting electrode to the other in the direction of the electric field. As depicted in Fig. 4−8 (b), in the ON state electrons flow through the relay from the drain (right) electrode, then the drain contact dimple, then the source (left) contact dimple, and then the source electrode. An electric field is developed between the contact dimples and the source/drain electrodes when the relay is turned OFF. For the drain contact, the electric field points toward the contact dimple; for the source contact, the electric field points toward the source electrode. Cycling tests for Ru-contact micro-relays were conducted using a negative DC voltage supply ($V_{DD}$ = −4 V), and material transfer in the reverse direction was observed, which verifies the field-dependent process. Similar results were reported in [58].

Metallic vapor arc-induced material transfer only occurs under hot-switching events. Cold-switching, which refers to opening and closing the relay with zero instantaneous current (power dissipation) through the contacts, was conducted to provide more insight into $R_{ON}$ stability issues for Ru contact electrodes. The supply voltage $V_{DD}$ is programmed to be a 5 kHz square wave synchronized with the actuation voltage signal $V_{GB}$: $V_{DD}$ ramps up 5 µs after $V_{GB}$, and ramps down 5 µs before $V_{GB}$, as shown in Fig. 4−9 (a). Under this driving scheme, current ($I_{DS}$) flows only after contact is made, and is shut off before contact is broken, to avoid hot switching. Fig. 4−9 (b) compares the evolution of $R_{ON}$ for hot-switching *vs.* cold-switching; the results clearly indicate the benefit of

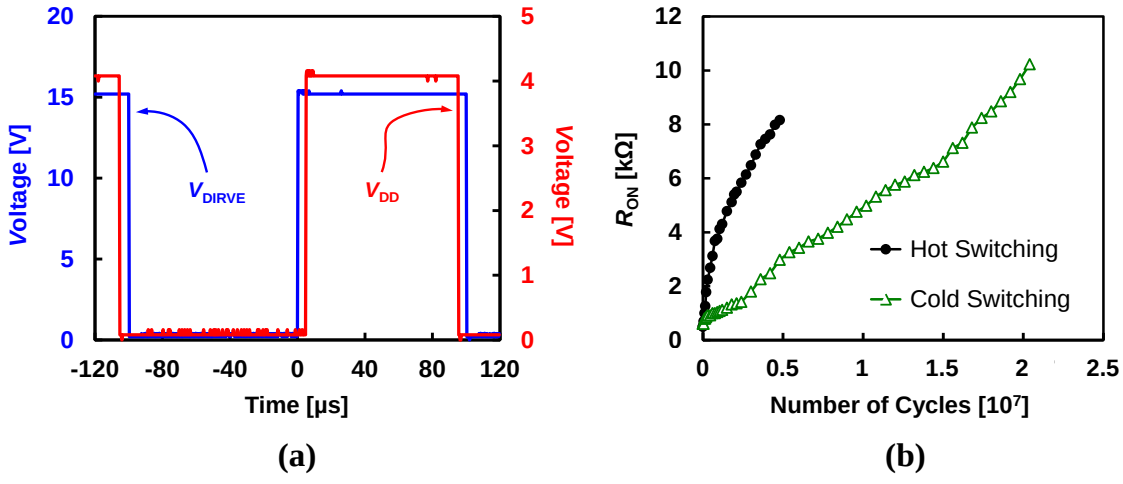



Figure 4-9. (a) Voltage waveforms used for the cold-switching test. (b) Comparison of $R_{ON}$ stability performance between a hot-switched relay and a cold-switched relay.

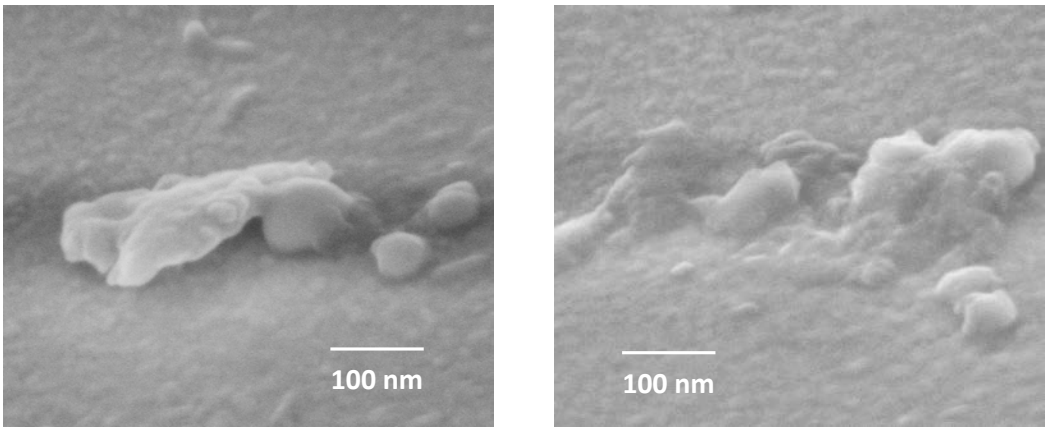



Figure 4-10. SEM images of electrodes after ~ $2\times10^7$ cycles of cold-switching: (a) drain electrode, (b) source electrode.

cold-switching. The increase in $R_{ON}$ is more gradual and it does not reach the 10 kΩ limit until ~ $2\times10^7$ cycles.

SEM analysis reveals a more homogeneous topography evolution of the drain and source electrodes after cold-switching (Fig. 4−10). Crater formation is not observed, and both contacting surfaces show similar accumulation of material ("bumps"). The chemical composition of the contacting surfaces was analyzed by Auger spectroscopy. Fig. 4−11 (a) and (b) present the Auger spectra for pure Ruthenium and Carbon, respectively. Fig. 4−11 (c) plots the Auger spectrum of a fresh (uncycled) Ru electrode. Notice that it resembles the reference Ru spectrum, with a major peak at 273 eV (which overlaps with the carbon peak) and a secondary peak near 231 eV [59]. Fig. 4−11 (d) shows the Auger spectrum of a Ru electrode of a cycled relay. The Ru peaks near 231 eV are significantly attenuated, and it is clear that the spectrum is now more analogous to that of the carbon reference, with a lingering Ru trace near 100 eV. It can be concluded that the contact surfaces are contaminated with carbon. Notice that an oxygen peak near 500 eV is also observed; due to the conductive nature of ruthenium oxide, it should have minimal impact on $R_{ON}$ as compared with insulating carbon films. Being a catalytic material, Ru is susceptible to friction polymerization [60]. Organic contaminants can originate from the fabrication process (*e.g.* photoresist residue) or the device testing chamber. In short, carbonaceous deposits cause the contact resistance to increase with the number of switching events.

$R_{ON}$ stability under cold-switching is found to be improved at higher device operating temperature (400 K vs. 300 K), as shown in Fig. 4−12. This is consistent with the findings reported by Brand *et al.* [61]. It is speculated that elevated temperature inhibits deposition of carbon contaminants. Another possibility is that the reliability of the carbon-based insulating film degrades at higher temperatures, which facilitates its electrical breakdown.

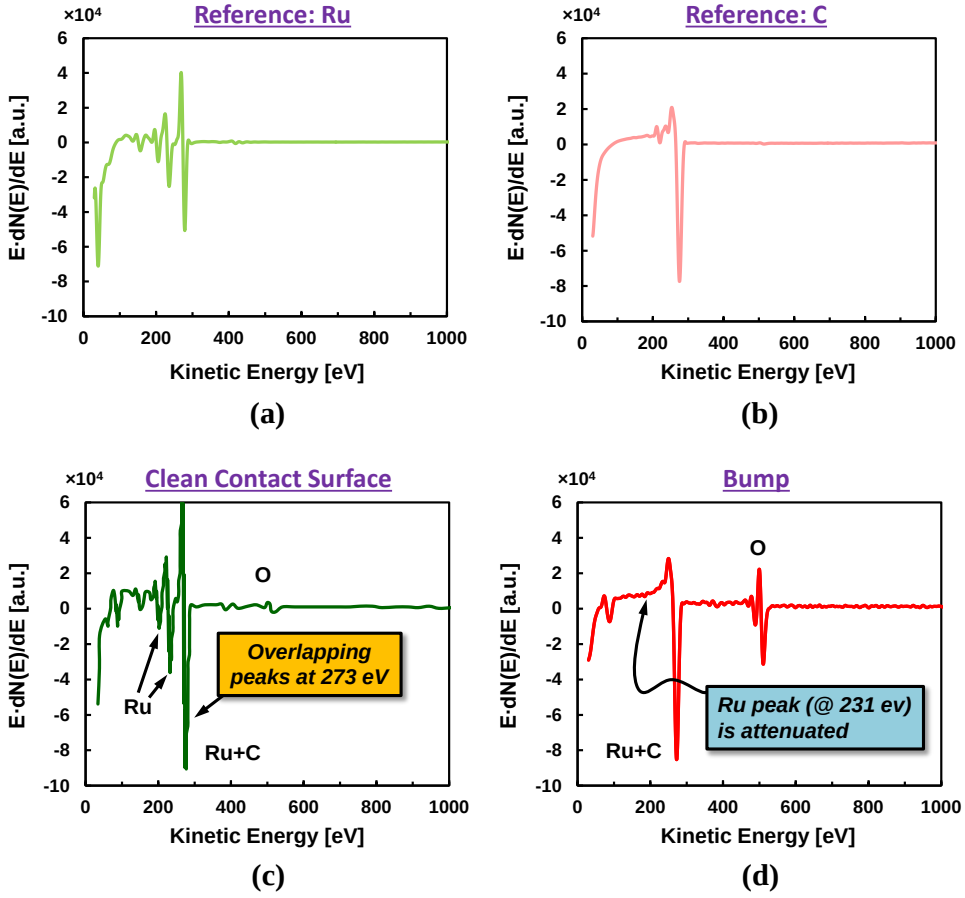



Figure 4-11. Auger spectra: (a) ruthenium reference, (b) carbon reference, (c) fresh Ru electrode, (d) cycled Ru electrode.

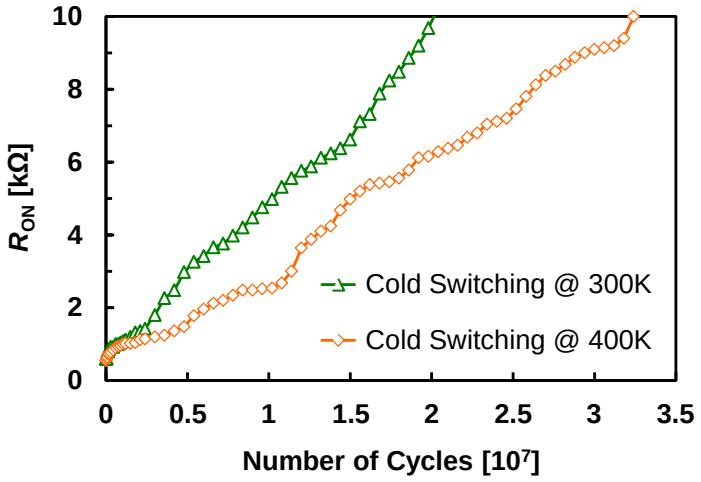



Figure 4-12. $R_{ON}$ stability of Ru-contact relays under cold-switching at different temperatures.

## 4.3 Microshell Encapsulation

As shown in the previous sections, an increase in relay ON-state resistance ($R_{ON}$) over time is highly correlated to chemical agents that react with the contact metal surfaces. The elimination of ambient oxygen, moisture and hydrocarbon contaminants is necessary to avoid oxide formation and friction polymerization. Hermetic packaging is necessary to achieve stable $R_{ON}$.

### 4.3.1 Background

There are two common approaches to wafer-level packaging of micro-electro-mechanical (MEM) devices. The first employs wafer bonding, which requires the formation of a bonding ring peripheral to the device region followed by anodic/solder/glass frit sealing of the capping wafer. This approach significantly increases the device footprint and results in a high-aspect-ratio package [62]. The second employs thin-film deposition to more compactly encapsulate the MEM device(s) in a microshell. Polycrystalline-silicon (poly-Si) and silicon-nitride can be used as the microshell structure and sealing layer materials, respectively [63]; however, they are deposited by low-pressure chemical vapor deposition (LPCVD) at temperatures exceeding 600$^{o}$C, which precludes monolithic integration with CMOS circuitry [64]. Therefore, low-thermal-budget microshell encapsulation methods have been explored by various research groups. For example, Stark and Najafi investigated thin-film metal electroplated over a sacrificial photoresist layer [65], and Monajemi *et al*. investigated a polymer membrane microshell structure with a thin metal sealing layer [66]. PECVD or sputter deposition can be used to deposit the sealing layer at 300 $^{o}$C [67].

Recently a nanoparticle inkjet-printed microshell technology was proposed to provide the advantages of a low thermal process budget (maximum substrate temperature $\leq$ 200$^{o}$C) and additive processing (eliminating the need for lithography and etching of the microshell structure and sealing layers) as compared with other wafer-level packaging technologies [68]. Pursuant to improving the $R_{ON}$ stability, this work employs a CMOS-compatible hermetic packaging technology to encapsulate micro-relays to mitigate the issue of contact oxidation.

### 4.3.2 Experimental Procedures

Fig. 4−13 illustrates the relay encapsulation process steps. Note that an underlying layer of metal (60 nm W) is used to route signals to/from the relay electrodes through an inter-layer dielectric (80 nm $Al_2O_3$). After the relay is fabricated (Fig. 4−13 (a)), an additional layer of sacrificial LTO (low-temperature oxide, 800 nm) is deposited and patterned to define the microshell anchor regions before the microshell is printed (Fig. 4−13 (b)) using silver (Ag) nanoparticle (50 nm diameter) ink. The sacrificial LTO is then selectively removed through the porous microshell with reduced-pressure (120 Torr) vapor HF etch, after which the microshell is sealed.

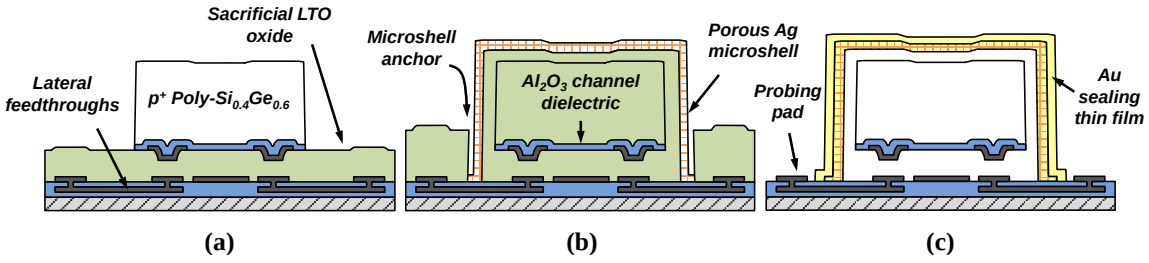



Figure 4-13. Schematic cross-sections illustrating the relay encapsulation process: (a) completed relay with connections to electrodes routed through an underlying layer of $Al_2O_3$; (b) deposition and patterning of a capping sacrificial layer to define microshell anchor regions, followed by Ag nanoparticle inkjet printing to form a porous microshell; (c) vapor HF etch to release the structure though the microshell, followed by Au nanoparticle inkjet printing to seal the microshell.

Smaller nanoparticles can be used as the sealant. In this work, gold (Au) nanoparticle (5 nm diameter) ink was printed over the Ag microshell in room ambient and subsequently annealed at 200 ˚C in a glovebox (pressure level ~ 5 Torr) to facilitate Au nanoparticle flow and solidification in the outermost pores of the microshell to make it impermeable. (It is important to prevent the sealant from penetrating through the microshell and affecting the encapsulated device(s). It was shown in [68] that only the outermost pores of the printed silver film are effectively filled by the smaller gold nanoparticles.)

Alternatively, a polymeric material can be used as the sealant. In this work, the amorphous cyclic transparent optical polymer (Cytop), which has very low oxygen permeability ($8.34\times10^{-10}$ $cm^3\cdot cm/cm^2\cdot s\cdot cmHg$) was investigated as an alternative sealant. For demonstration purposes, it was deposited by spin-coating (to a thickness of ~1 μm) inside the glovebox and cured *in situ* at 200 ˚C. (Since it is a dielectric polymer, with resistivity > $10^{17}$ Ω·m, it can be deposited over the entire chip area without causing any electrical shorting of the signal lines/electrodes.) In principle, Cytop also can be inkjet-printed.

### 4.3.3 Results and Discussion

Fig. 4−14 shows a scanning electron microscopy (SEM) image of a single MEM relay encapsulated within a Au-sealed microshell. The length of the microshell can be made arbitrarily large if the width is less than ~100 um [68]. In this work, multiple relays (up to 6) were successfully encapsulated within a single long microshell. Fig. 4−15 shows surface topography measurements of a microshell after selective removal of the sacrificial oxide in HF vapor to release the encapsulated relay structure. This particular microshell encapsulates 6 relays, although only one is seen in Fig. 4−15 (a). The line profile in Fig. 4− 15 (b) shows that the microshell pops up after release (*i.e.*, it has a convex shape) due to a negative stress gradient within the printed film; thus, the height of the microshell above the relay is greater than the thickness of the capping sacrificial LTO layer (ref. Fig. 4−13 (b)).

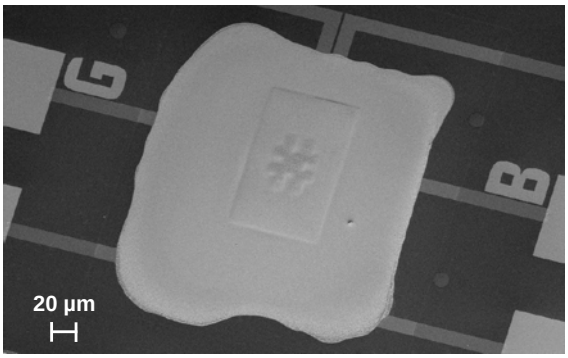



Figure 4-14. SEM image of a single encapsulated relay.

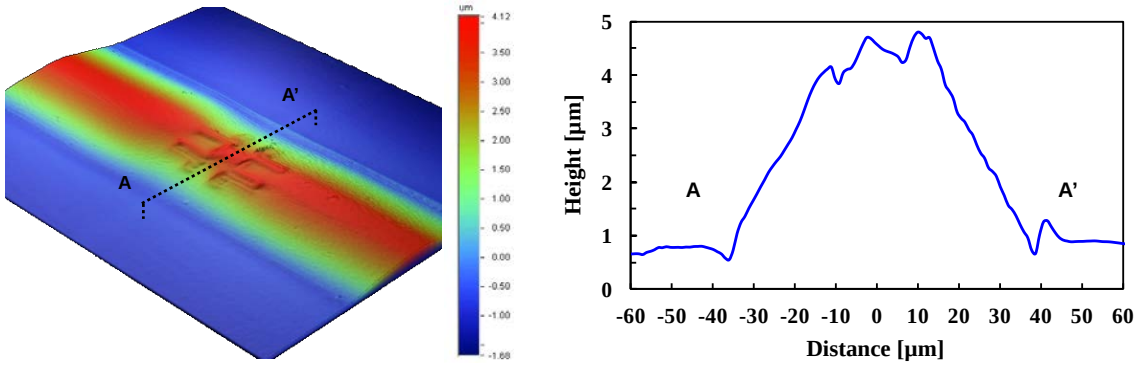



Figure 4-15. Wyko NT3300 white-light interferometer images of a microshell-encapsulated MEM relay: (a) 3D topography map, and (b) corresponding surface height profile.

Measured current-*vs*.-voltage characteristics for bare *vs*. encapsulated devices are compared in Fig. 4−16, which shows that the encapsulation process has negligible impact on the relay switching voltages. The Lakeshore vacuum probe station was used to electrically characterize the relays. The test setup used to study the evolution of ON-state resistance with the number of switching cycles is illustrated in Fig. 4−17 (a). Fig. 4−17 (b) shows how $R_{ON}$ increases with the number of switching cycles, due to oxidation of the W electrode surfaces. It can be seen that $R_{ON}$ for the bare (unencapsulated) relay increases relatively rapidly and crosses over this threshold at ~$10^5$ cycles. In contrast, the encapsulated devices show stable $R_{ON}$ up to ~$10^7$ cycles, so that the effective relay operating lifetime is enhanced by ~100× with encapsulation. Since the Cytop sealing process was performed entirely in a glovebox, it likely resulted in lower trace amounts of oxygen within the sealed microshell and hence superior $R_{ON}$ stability than the Au-nanoparticle sealing process which was performed partly in room ambient.

It should be noted that some contamination may result from the microshell sealing process. The Au nanoparticles are originally covered with an organic material (ligands) to prevent them from aggregating within the ink; when the printed ink is dried/ solidified by thermal annealing, this organic material vaporizes and some of it may diffuse through

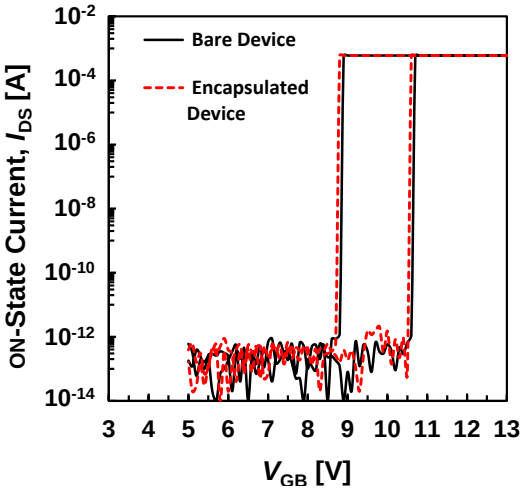



Figure 4-16. Comparison of measured *I-V* characteristics for a bare relay *vs.* an encapsulated relay.

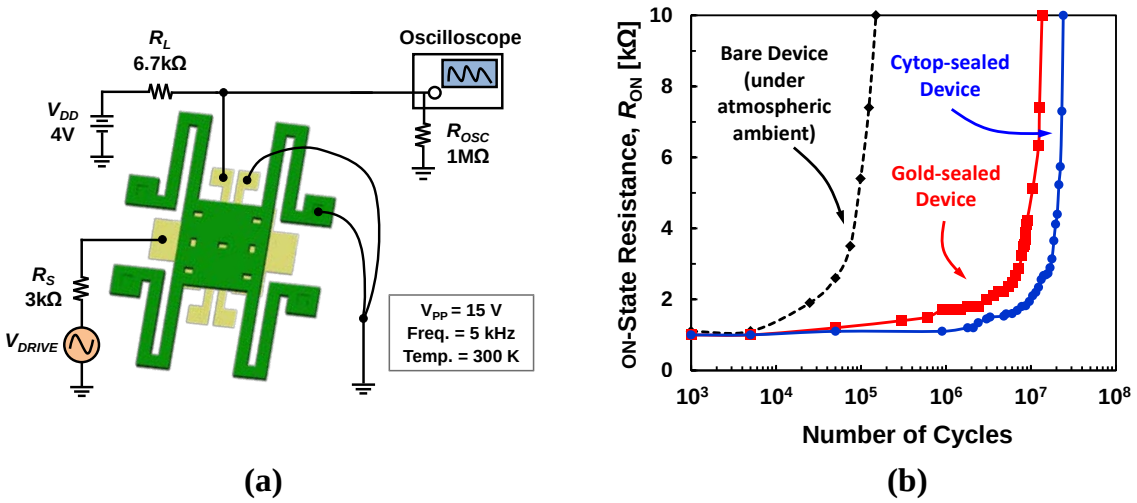



Figure 4-17. (a) Test setup for monitoring relay ON-state resistance over many hot-switching cycles. (b) Evolution of contact resistance with the number of hot-switching cycles, for bare vs. encapsulated relays.

the pores of the Ag film into the microshell cavity. Cytop is only available in perfluorinated solvents, which outgas during thermal annealing and may end up in the microshell cavity as well. Differences in the outgassing levels for Au nanoparticle ink *vs.* Cytop might also account (in part) for the superior $R_{ON}$ stability of the Cytop-sealed relay.

# Chapter 5

# Experimental Studies of Contact Detachment Delay $\tau_{CD}$

The abrupt switching behavior of mechanical switches makes it imperative to ensure that they turn off more rapidly than they turn on. In a complementary logic circuit, slower turn-off than turn-on could lead to the formation of a direct current path between the power supply and the ground, which would result in undesirable dynamic power dissipation during signal transitions. In this chapter, the contact detachment delay ($\tau_{CD}$) of micro-relays is systematically characterized and investigated. $\tau_{CD}$ is shown to be correlated with contact adhesive force and the mechanical properties of the contact materials; $\tau_{CD}$ can also be reduced by ultra-thin-oxide coating and contact area scaling.

## 5.1 Motivation

Ideally, the operating speed of a relay-based integrated circuit is limited by the mechanical switching time rather than the electrical delay (charging/discharging time) [9]. Previous studies of mechanical switching time have focused on turn-on delay, specifically pull-in dynamics [69] and methods for reducing the pull-in voltage ($V_{PI}$) and pull-in delay ($\tau_{PI}$) [28]. Since very large contact resistance ($R_{ON}$ > 10 kΩ) can significantly reduce computational throughput, $R_{ON}$ stability has also been investigated extensively for various contact materials and relay operating conditions [70].

In contrast, the turn-off delay of micro-relays was reported but has yet been studied in detail [71]. This is because it is generally assumed that a relay turns off more quickly than it turns on, since a relatively small separation (~1 nm) between the contacting electrodes is sufficient to prevent current flow, *i.e.* the mechanical displacement required to turn off a relay is smaller than that required to turn on a relay. However, the time required to break physical contact (before the contacting electrodes can move apart) can be significant due to surface adhesion [72]. If the contact detachment delay ($\tau_{CD}$) is greater than the pull-in delay $\tau_{PI}$, then a direct current path (“short circuit”) between the power supply and ground can be temporarily formed in a conventional complementary logic circuit comprising at least one “pull-up” device connected between the output node

and power supply and at least one “pull-down” device connected between the output node and ground; the resultant “crowbar current” gives rise to undesirable dynamic power dissipation [73]. In this chapter, the impact of contacting electrode material, micro-relay operating conditions and device structural dimensions on $\tau_{CD}$ is systematically characterized. The impact of dimensional scaling is also investigated to provide insight for device miniaturization.

## 5.2 Contact Theory

The source/drain electrode surface roughness was measured by atomic force microscopy (AFM) to be approximately 0.7 nm (rms) for each of the different metals. On the other hand, the channel (top electrode) surface should be much smoother, due to conformal deposition of the relatively thick sacrificial LTO layers. A contact model between two nominally flat surfaces (with one smooth and the other rough) was developed by Greenwood and Williamson [74], which links the load to the summit level distribution of multiple asperities. However, actual asperity height distribution is not easily obtained and modeled, and it could vary from device to device. For simplicity, the contacting asperities are assumed to be of the same height and equally loaded, as in Tas *et al.* [75].

Furthermore, due to the nature of small loading, contacts in microsystems are typically made only between a few contacting asperities, and the number of contact points $N$ is in the low single-digit range which can be close to zero [75]. For the purpose of providing insight into the dependences of the contact adhesive force and $\tau_{CD}$ on the contacting electrode material, $N$ is approximated to be 1 and the contact geometry is approximated as a single hemispherical asperity compressed against a flat surface, reducing the case to “sphere on flat”.

Based on the analytical adhesion model summarized in Maugis and Pollock [31], the adherence force (or the “pull-off” force) that is required to separate the contacting surfaces (sphere on flat) is described by

$$F_{adh} = \alpha \pi R \Delta\gamma \tag{5.1}$$

In Eq. (1), $\Delta\gamma$ ($\equiv \gamma_1 + \gamma_2 - \gamma_{12}$) is the Dupré energy of adhesion, $R$ is the spherical radius of the contacting asperity, and the coefficient $\alpha$ varies from 3/2 to 2 depending on the model of elastic contact.

It is assumed that the contact is elastic but the contact interface is maintained in a state of initial plastic deformation; such deformation determines the contact area and the adhesion force. After removal of the external load and during contact detachment, the deformed spherical surface recovers, with an effective radius of curvature $R_f$ (considering the originally flat surface now exhibits a spherically deformed morphology), which can

be derived by approximating the pressure distribution to a Hertzian contact as in Maugis and Pollock [31] and Du *et al.* [76]:

$$R_{\mathrm{f}} = \frac{4}{3}\frac{a_{\mathrm{f}}E^{*}}{\pi p_{\mathrm{m}}} \tag{5.2}$$

Here $a_f$ denotes the radius of contact during unloading and $E^*$ is the biaxial Young's modulus given by $E/(1-\nu^2)$ in which $E$ is the Young's modulus and $\nu$ is the Poisson ratio. The mean pressure $p_{\mathrm{m}}$ equals to the hardness $H$ of the material when the entire contact undergoes plastic deformation. The contact junction itself can be approximated to have a hemispherical shape with radius $a_{\mathrm{f}}$ which is related to the contact force:

$$a_{\mathrm{f}} = \sqrt{\frac{F_{\mathrm{load}}}{\pi p_{\mathrm{m}}}} \tag{5.3}$$

Combining Eq. (2) and (3), Eq. (1) reduces to

$$F_{\mathrm{adh}} = \alpha\pi R_{\mathrm{f}}\Delta\gamma = \frac{4\alpha\Delta\gamma E^{*}F_{\mathrm{load}}{}^{1/2}}{3(\pi p_{\mathrm{m}}^{3})^{1/2}} \tag{5.4}$$

as given by [31] and [76].

The switching delays of the micro-relays are compared herein for the same operating voltage conditions and hence the same $F_{\mathrm{load}}$. Since the adhesion energy $\Delta\gamma$ is the sum of the surface energies $\gamma_1$ and $\gamma_2$ minus the interfacial energy $\gamma_{12}$ (which equals to 0 when the two contacting surfaces are composed of identical material), the term reduces to $2\gamma_1$ (= $2\gamma_2$). As a result, any difference in adherence force is due to differences in the contact material mechanical properties:

$$F_{\mathrm{adh}} \propto \frac{\gamma E^{*}}{H^{3/2}} \tag{5.5}$$

Therefore, the ratio of surface energy times the effective Young's modulus to hardness should be positively correlated to adhesion, *i.e.* higher $\gamma E^*/H^{3/2}$ should correspond to higher $F_{\mathrm{adh}}$.

## 5.3 Test Setup

The fabricated micro-relays are transferred to a Lakeshore TTPX vacuum probe station for characterizations soon after HF vapor release, to minimize contact surface contamination. In this sealed vacuum chamber, the temperature, pressure, and relative humidity are kept at 300 K, ~5 μTorr, and ~0%, respectively. Generally the devices exhibit relatively high $R_{ON}$ (~10 kΩ) for the first switching cycle, and hence are subjected to a high-voltage ($V_{DS}$ ~ 6 V along with current compliance) "burn-in" process [77] using the HP 4155B semiconductor parameter analyzer to reduce $R_{ON}$ to below 0.9 kΩ, depending on the contact material. The contact detachment delay measurements are performed after the burn-in procedure. Without such a process, the residual contamination layer such as hydrocarbons [78] and some metal-oxides [79] (which have lower surface energy compared to the metal counterparts) could reduce the adhesion force and subsequently $\tau_{CD}$ [78]. It should be noted that minute amounts of oxygen and contaminants such as hydrocarbons can cause thin insulating films to form at the contacting asperities over time, especially during the course of many hot-switching cycles [79], [80].

Relay switching delays are monitored using a resistive-load inverter setup as depicted in Fig. 5−1; the relay serves as the "pull-down" device and a resistor serves as the "pull-up" device. The cyclic evolution of ON-state resistance ($R_{ON}$) [79], as well as $\tau_{PI}$ and $\tau_{CD}$, are monitored as shown in Fig. 5−2. When the relay is ON, a direct current path exists between the power supply ($V_{DD}$) and ground, and the output voltage is given by the voltage divider formula shown in Fig. 5−2 (a). $\tau_{PI}$ is defined as the difference between the time that $|V_{GB}|$ increases above $0.5\times|V_{DRIVE}|$ and the time that the output voltage begins to fall toward ground as shown in Fig. 5−2 (b). $\tau_{CD}$ is defined as the difference

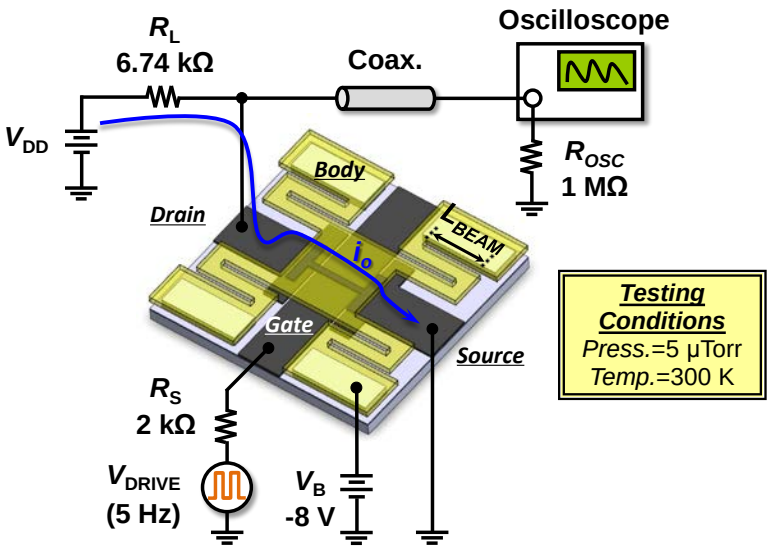



Figure 5-1. Schematic of the resistive-load inverter test setup.

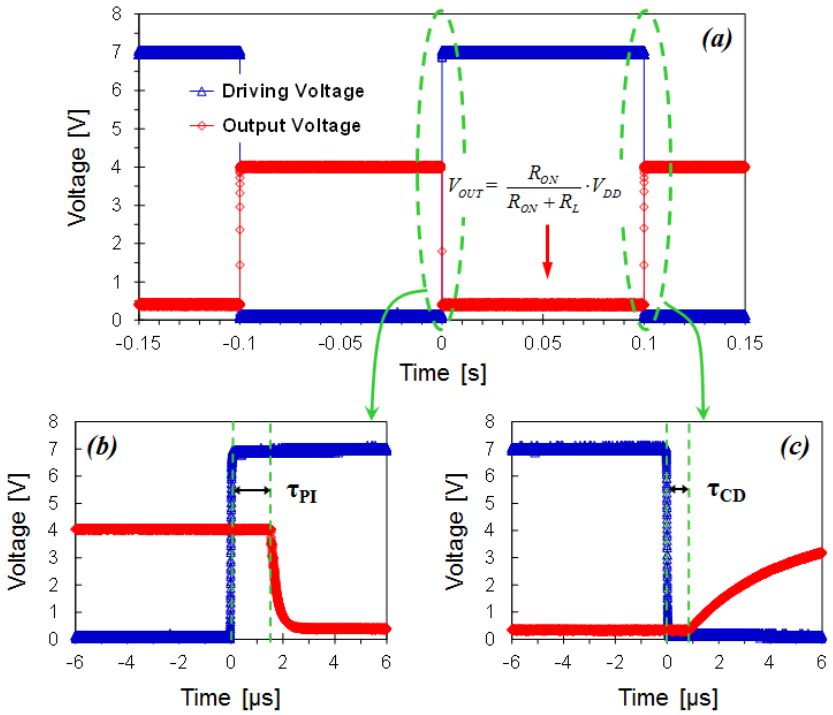



Figure 5-2. (a) Measured input and output voltage waveforms for the setup in Fig. 5-1 (with $V_D$ = 4 V, $V_{DRIVE}$ = 7 V, and $V_B$ = −8 V), with zoomed-in views of the regions of (b) relay turn-on and (c) relay turn-off.

between the time that $|V_{GB}|$ falls below $0.5\times|V_{DRIVE}|$ and the time that the output voltage begins to rise toward $V_{DD}$ as depicted in Fig. 5-2 (c). This is essentially the time it takes for the contact dimples to be fully detached from the bottom source/drain electrodes after the relay driving voltage is removed.

The body (structure) is biased at −8 V in order to lower the gate voltage required to switch the relay, to < 3 V. The hysteresis voltage $V_H$ sets the lower limit for relay $V_{PI}$ and restricts the maximum body bias that can be applied; this allows $V_{DRIVE}$ to be scaled down to 3 V (further increase in $|V_B|$ will cause the device to stick down when $V_{RL}$ drops below 0 V). The maximum value of $V_{DD}$ used in this work is 7 V, because contact welding becomes an issue for $V_{DD}$ > 7 V.

Herein $\tau_{PI}$ and $\tau_{CD}$ are characterized for micro-relays with Ni, Ru, W and $TiO_2$-coated W contacting electrodes. W was patterned with dry etching whereas Ru and Ni were patterned with the lift-off process described in Chapter 4. Ru-contact electrodes patterned with dry-etching [55] were also characterized and yielded very similar results as the ones fabricated with a lift-off process. The mechanical properties of these materials are summarized in Table 5−1. The relative values of adhesion force listed in Table 5−1 for the contact materials studied in this work are normalized to the value for W, using Eq. 5−5. For $TiO_2$-coated W electrode, the Young's modulus and the hardness are assumed to be the same as for W, since the volume of the ultra-thin ALD coating is very small relative to that of the W electrode; it mainly alters the surface energy. The

Table 5-1. Mechanical properties of contact materials.

| | **$TiO_2$** | **W** | **Ru** | **Ni** |
|---|---|---|---|---|
| Surface energy, $\gamma$ (J/m$^2$) | 0.89 [81] | 3.675 [82] | 3.050 [82] | 2.450 [82] |
| Young's modulus, $E$ (GPa) [38] | -- | 360 | 430 | 216 |
| Poisson ratio, $v$ [38] | -- | 0.28 | 0.3 | 0.31 |
| Estimated hardness, $H$ (GPa) | -- | 21.3 [83] | 15.28 [84] | 6 [85] |
| Normalized adherence force | 0.24 | 1 | 1.65 | 2.73 |

surface energies of the contact metals after the burn-in process are assumed to be the same as those reported by Vitos *et al.* [82] listed in Table 5−1. It should be noted that the hardness of a thin-film material usually is higher than that of a bulk material due to grain-boundary strengthening; this is known as the Hall-Petch effect. In [83]-[85], the micro-hardness of sputtered thin films (comparable in thickness to the electrode layer in this work) was determined directly by nanoindentation tests. The values in Table 5−1 are extracted from [83]-[85] at an indentation depth of 70 nm.

## 5.4 Results and Discussions

Fig. 5−3 compares the average measured values of $\tau_{CD}$ for micro-relays employing different contact materials, as a function of the driving voltage $V_{DRIVE}$ and supply voltage $V_{DD}$. (Ten devices were measured for each of contact type; the standard deviation σ for $\tau_{PI}$ is 0.1 μs, and σ for $\tau_{CD}$ is 0.03 μs.) These devices have very similar values of $\tau_{PI}$, since their poly-$Si_{0.35}Ge_{0.65}$ structures are identical in design. The measured trend of $\tau_{CD}$ for different contact materials is as expected, since $F_{adh,Ni} > F_{adh,Ru} > F_{adh,W} > F_{adh,TiO2/W}$ (cf. Table I).

From Fig. 5−3 (a) it can be seen that $\tau_{CD}$ increases with the amplitude of the driving voltage. An increase in gate actuation voltage enhances the contact force due to quadratic growth in electrostatic attraction. As the external load rises, $a_f$ (which can be interpreted as an equivalent contact radius as if only one spot were in contact) widens according to Eq. 5−3. In any case, the real contact area increases with increasing contact force, leading to larger adhesive force and hence longer $\tau_{CD}$. The rate of change in $F_{adh}$ to $F_{load}$ is also proportional to the factor $\gamma E^*/H^{3/2}$, which can be shown by differentiating Eq. 5−4 with respect to $F_{load}$. Thus, contact electrodes exhibiting higher initial values of $\tau_{CD}$ would respond to the change in $F_{load}$ more rapidly, as seen in the Ni electrodes.

Fig. 5−3 (b) shows that $\tau_{CD}$ increases with the supply voltage $V_{DD}$. A possible explanation for this trend is an increase in real contact area with increasing $V_{DD}$ due to increased power dissipation (Joule heating). The steady-state temperature $T_m$ at a contact

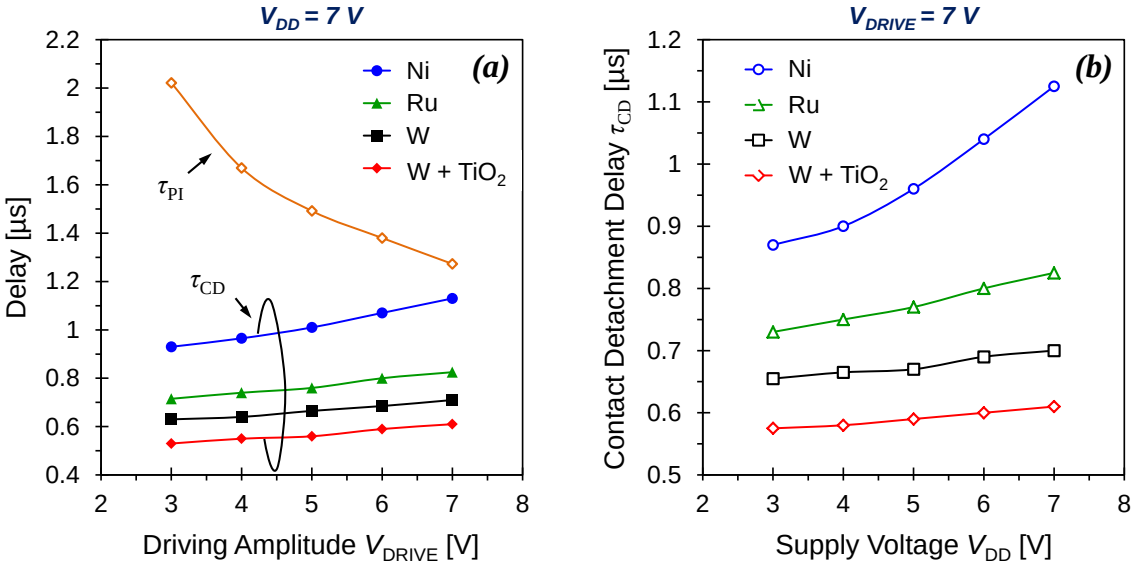



Figure 5-3. Contact detachment delay ($\tau_{CD}$) and pull-in delay ($\tau_{PI}$) of micro-relays with different contact electrode materials (a) vs. actuation voltage ($V_{DD}$ = 7 V) and (b) vs. supply voltage ($V_{DRIVE}$ = 7 V). $L_{BEAM}$ = 15 µm.

spot, given a contact voltage $V_C$ across the junction, can be estimated using the Kohlrausch-relation as in [86]:

$$T_m = T_0 + \frac{V_C^2}{8\lambda\rho} \tag{5.6}$$

where $T_0$ is the temperature far away from the contact spot (assumed to be 20˚C), $\lambda$ is the thermal conductivity [38] and $\rho$ is the electrical resistivity (calculated by multiplying the measured sheet resistance by the film thickness) of the material. Note that in order to estimate the de-embedded $V_C$ (across a single contact) one must take into account the trace resistance $R_{trace}$ (comprising ~28 squares) from the source/drain signal paths. The true contact resistance $R_C$ for each single contact is given by ($R_{ON}$ - $R_{trace}$)/2 and $V_C$ can be calculated as

$$V_C = \frac{R_C}{2R_C + R_{trace} + R_L} V_{DD} \tag{5.7}$$

Calculations predict that the temperature exceeds 80˚C for high $V_{DD}$ but is still well below the softening temperature (cf. Table 5−2), for each of the contact materials.

Table 5-2. Thermal/electrical properties of the contact metals.

| | W | Ru | Ni |
|---|---|---|---|
| Thermal coductivity @ 20˚C, $\lambda$ ($W \cdot m^{-1} \cdot k^{-1}$) | 167 | 105 | 92 |
| Electrical resistivity @ 20˚C, $\rho$ ($\mu\Omega \cdot cm$) [38] | ~24 | ~22 | ~18 |
| $R_{ON}$ @ $V_{DD}$ = 7 V ($\Omega$) | ~700 | ~480 | ~250 |
| $V_C$ @ $V_{DD}$ = 7 V (V) | ~0.284 | ~0.190 | ~0.089 |
| Estimated temperaure at contact spot @ $V_{DD}$ = 7 V, $T_m$ (˚C) | 272 | 215 | 80 |
| Softening temperature (˚C) [38] | 1000 | 430 | 520 |

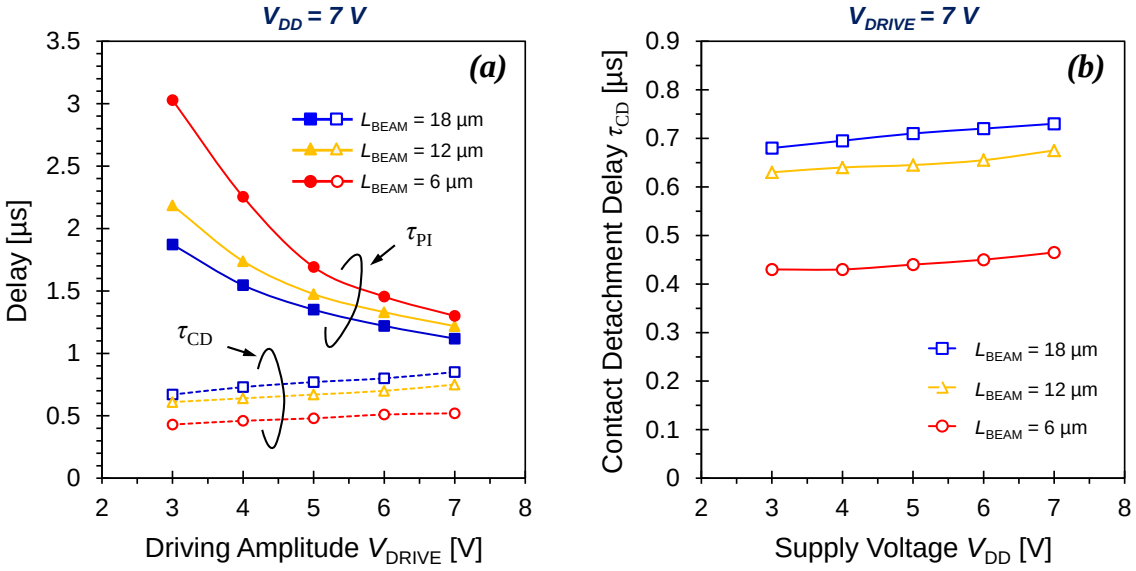



Figure 5-4. Contact detachment delay ($\tau_{CD}$) and pull-in delay ($\tau_{PI}$) of W micro-relays with different suspension beam length ($L_{BEAM}$) (a) vs. actuation voltage ($V_{DD}$ = 7 V) and (b) vs. supply voltage ($V_{DRIVE}$ = 7 V).

However, it has been experimentally shown that the melting temperature of small particles can be lower than that of bulk material [87]. Therefore, softening might occur locally at some smaller contacting asperities, leading to increased contact area and $\tau_{CD}$.

Another possible explanation for the increase of $\tau_{CD}$ with increasing $V_{DD}$ is the removal or electrical breakdown of insulating material (native oxide, or surface contaminants) to temporarily reestablish interfacial metal-to-metal bonds at the contacting asperities [77]. Since metal-to-metal bonds having higher binding energies, the adhesion force rises consequently. We believe this is more likely to be the dominant factor to cause $\tau_{CD}$ to increase.

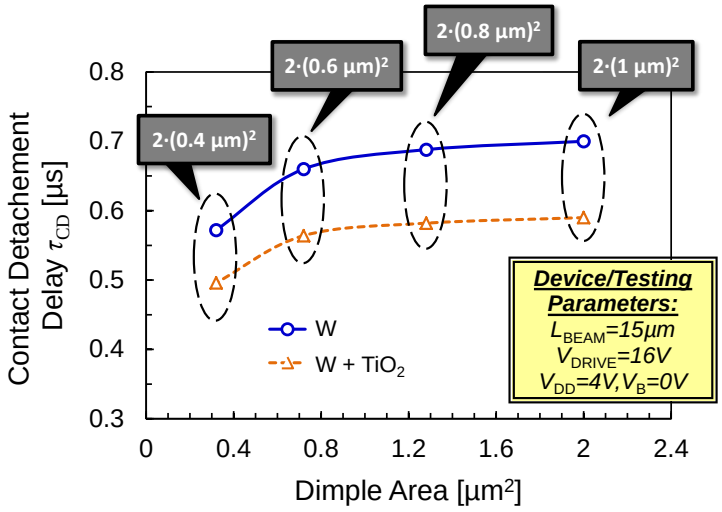



Figure 5-5. Measured $\tau_{CD}$ of W micro-relays as a function of total contact dimple area (2 square dimples for each relay).

In addition to the contact material properties and relay operating conditions, relay design parameters also affect $\tau_{CD}$. The stored elastic energy in the flexure beams and the spring restoring force (which pulls the relay out of contact, to turn it OFF) is proportional to the effective spring constant ($k_{eff}$) of the folded-flexure suspension beams. A shorter flexure beam length introduces larger spring restoring force so that the electrodes can be separated more quickly upon removal of the hold-down force, with a tradeoff of increased $V_{PI}$ and hence increased $\tau_{PI}$ for the same operating voltage conditions (Fig. 5−4). Furthermore, smaller contact dimple area is also beneficial for reducing contact adhesive force [72]. By reducing the contact dimple width from 1 µm to 0.4 µm, $\tau_{CD}$ is reduced from 0.7 µs to 0.57 µs, as presented in Fig. 5−5. It is observed that $\tau_{CD}$ does not scale linearly with the apparent contact area; a result reminiscent of the findings on non-linear reduction in surface adhesive force by Li *et al.* [88].

In summary, the contact detachment delay ($\tau_{CD}$) of a micro-relay can vary significantly with the contact electrode material, as well as relay design parameters and operating conditions. Low $\gamma E^*/H^{3/2}$ ratio is a favorable electrode property for reducing contact adhesive force, which also can be reduced by thin dielectric coating and scaling down the area of the contacting regions. Structural design optimization involves a trade-off between improving turn-on delay ($\tau_{PI}$) and degrading turn-off delay; fortunately, a large design window exists for ensuring that ($\tau_{PI} > \tau_{CD}$) to avoid crowbar current in a relay-based complementary logic circuit. Selection of the operating voltage ($V_{DD}$) involves the same trade-off.

# Chapter 6

# Summary and Future Research Directions

Electrostatic relay technology presents a pathway for enhancing the energy efficiency of electronic devices because it provides for zero leakage current, abrupt ON/OFF switching behavior, and compatibility with CMOS technology. These properties make scaled relays attractive for efficient power-gating of CMOS circuitry, as well as for ultra-low-power digital computation. To fully realize their promise, however, relays must operate with sufficiently stable characteristics to ensure reliable circuit operation. This chapter summarizes the contributions of this work and offers suggestions for future research directions.

## 6.1 Summary

This thesis presents the design, fabrication, and reliability studies of electrostatic microrelays aimed for digital logic applications. Various device failure mechanisms were investigated. Excellent stability in switching voltage ($V_{PI}$) was seen over 10 billion ON/OFF switching cycles, indicative of immunity against fatigue (of the poly-SiGe/$Al_2O_3$ structural film stack) and against dielectric charging. Contact resistance ($R_{ON}$) degradation was identified to be the primary issue which practically limits the operating lifetime of micro-relays. For tungsten (W) contacting electrodes, $R_{ON}$ inevitably increases with time and the number of switching cycles, due to surface oxidation. The rate of $R_{ON}$ degradation depends on micro-relay switching frequency, ON time, and OFF time; stable operation was observed through $3.5\times10^8$ ON/OFF cycles at switching frequency of 60 kHz. Contact resistance stability is also found to be positively correlated to the contact force, which can help to break down ultra-thin dielectric surface layers.

Ruthenium (Ru) was investigated as an alternative contacting electrode material because it forms a conductive oxide, in contrast to W. A lift-off process was developed to form the Ru electrodes, to fabricate Ru-contact logic micro-relays. The sputtered 70-nm-thick Ru film has a low electrical resistivity of 22 μΩ·cm (very close to that of a W

film) with a residual tensile stress below 200 MPa. $R_{ON}$ was found to increase under hot-switching conditions, but did not exceed 10 kΩ before stiction-like failure occurred after ~$5\times10^6$ cycles. Failure analysis via scanning electron microscopy and Auger spectroscopy indicated two main causes of contact degradation: material transfer and friction-polymer accumulation. Cold-switching eliminates arcing during contact opening/closure and was found to result in stable contact performance up to ~$5\times10^7$ cycles, limited by carbonaceous deposits. Both process-induced contamination and adventitious hydrocarbons contribute to the formation of non-volatile friction polymer.

A low-cost, low-thermal budget inkjet-printed microshell encapsulation technique based on nanoparticles are proposed and demonstrated to improve stability of W-contact microrelays. Silver nanoparticles (~50 nm in diameter) are used to construct the porous microshell, which is sealed by gold nanoparticles (~5 nm in diameter) after HF vapor device release. The encapsulation process not only retains mechanical characteristics of the logic microrelays (such as $R_{ON}$, $V_{PI}$ and $V_{RL}$), but also extends their lifetime by two orders of magnitude.

Lastly, the contact detachment delay ($\tau_{CD}$) of logic micro-relays was experimentally investigated, for various contacting electrode materials. $\tau_{CD}$ was found to be positively correlated to surface adhesive force, which depends on the contacting material's mechanical properties including hardness, Young's modulus and surface energy. Relay design parameters also affect $\tau_{CD}$; stiffer suspension beams provide for stronger restoring force hence smaller $\tau_{CD}$ (at a trade-off of larger pull-in delay, $\tau_{PI}$), while a reduction in apparent/real contact area helps to reduce $\tau_{CD}$.

## 6.2 Suggestions of Future Work

This research work has presented the fundamental reliability analysis for the electrostatic logic microrelays. Further work is suggested for improving their performance and lifetime, to expand the range of applications.

### 6.2.1 Alternative Contact Materials

As described in Chapter 4, Ru electrodes degrade with the number of relay (hot-) switching cycles due material transfer and hydrocarbon contamination. Its electrically conductive oxide ($RuO_2$) is capable of catalyzing large carbon-based molecules into smaller molecules ($CH_4$ into CO and $H_2$, for example); $RuO_2$ can oxidize smaller alcohols as well [52]. Though some native oxide $RuO_2$ is formed on the Ru electrode surface during the course of cycling, actual coverage of $RuO_2$ over Ru is unknown. Therefore it would be worthwhile to investigate the use of $RuO_2$, formed directly by sputter deposition, as a contacting electrode material.

Alternatively, metal alloys could be investigated as the contacting electrode material. In particular, it would be interesting to investigate alloys of Ru or $RuO_2$ with other

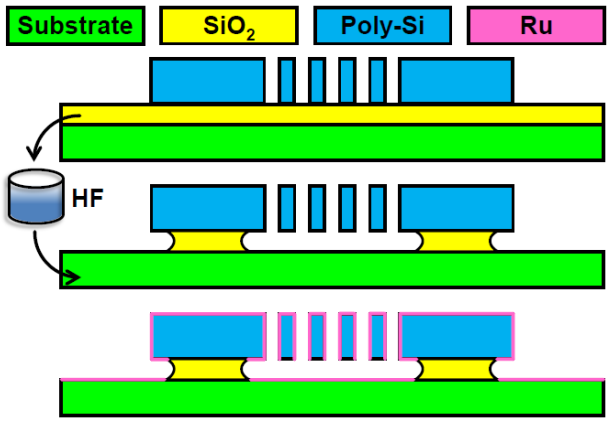



Figure 6-1. Cross-sectional illustration of the one-mask process used to fabricate comb-drive resoswitch [50].

metals, which leverage favorable properties of those materials. For example, adding W to $Ru/RuO_2$ could potentially make the contacts less susceptible to material transfer since W is more resistant to arcing.

On the other hand, it has been shown that surface treatment such as high-temperature oxygen annealing (under high vacuum) and oxygen plasma cleaning can effectively reduce absorption and inhibit the accumulation of organic deposits [89], [90]. Such "deactivation" treatments could be employed for improved $Ru/RuO_2$ contact stability.

### 6.2.2 Metal-Last Process for Contact Material Characterization

The integration of alternative contact materials is not trivial for the vertically actuated relay design [55]. A laterally actuated relay design can be fabricated using one-mask process [50], and hence could be used to more quickly identify promising candidates for the contact material. As depicted in Fig. 6−1, this "metal-last" one-mask approach eliminates the need for going through the complete 5-mask logic relay process as well as customizing new processes for each individual material (such as etching).

### 6.2.3 Circuit Design for Arc-Free Operation

Circuit design techniques could be used to ameliorate voltage/current surges during contact opening/closure (which causes material transfer). For example, by placing diodes or resistor/capacitor (RC) networks in parallel with the relay, transient voltages can be reduced and consequently damage to the relay contacts should be suppressed.

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