Germanium-Source Tunnel Field Effect Transistors for Ultra-Low Power Digital Logic

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By

Sung Hwan Kim

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Abstract

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Driven by a strong demand for mobile and portable electronics, the chip market will undoubtedly impose "low power" as the key metric for microprocessor design. Although circuit and system level methods can be employed to reduce power, the fundamental limit in the overall energy efficiency of a system is still rooted in the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) operating principle and its immutable physics: an injection of thermally distributed carriers will not allow for switching characteristics better than 60 mV/dec at room temperature. This constraint ultimately defines the lowest energy consumed per digital operation attainable with current Complementary-Metal-Oxide-Semiconductor (CMOS) technology.

In this work, Tunnel Field Effect Transistor (TFET) based on Band-to-Band Tunneling (BTBT) will be proposed and investigated as an alternative logic switch which can achieve steeper switching characteristics than the MOSFET to permit for lower threshold (V_{TH}) and supply voltage (V_{DD}) operation. It will be experimentally demonstrated that by employing Germanium (Ge) only in the source region of the device, a record high *on* to *off* current ratio (I_{ON}/I_{OFF}) can be obtained for 0.5 V operation. Technology Computer Aided Design (TCAD) calibrated to the measured data will be used to perform design optimization study. The performance of the optimized Ge-source TFET will be benchmarked against CMOS technology to show greater than 10x improvement in the overall energy efficiency for frequency range up to 500 MHz. The fundamental challenges associated with TFET-based digital logic design will be addressed. In order to mitigate these constraints, a circuit-level solution based on n-channel TFET Pass-Transistor Logic (PTL) will be proposed and demonstrated through mixed-mode simulations. The accompanying design modifications required at the device level will be discussed.

To my family

For our steps toward love and justice

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Chapter 1

The Need for a New Switch

1.1 CMOS Power Crisis

The advent of integrated circuit (IC) technology has triggered an era of electronics with previously unimaginable capabilities and computing power. Decades of progress were driven by the continued miniaturization of transistor dimensions to yield greater circuit density and functionality at lower cost per function.

But the chip industry is facing a crisis. Although transistor scaling has provided for enhanced performance, it has also resulted in increased in power per unit area of a chip. This is manifested in today's typical Complementary-Metal-Oxide-Semiconductor (CMOS) microprocessor, which operates at around the power density of a nuclear reactor (Fig. 1.1) [1].

The fundamental reason for the rapid rise in the power density is that the supply voltage (V_{DD}) used to drive the transistors has not scaled proportionately with transistor density. Simply put, transistor dimensions have continued to shrink to minute scales, but the voltage used to operate these transistors has plateaued. As Fig. 1.2(a) indicates the supply voltage reduction has leveled off at approximately 1 V for 90 nm node and beyond [2].

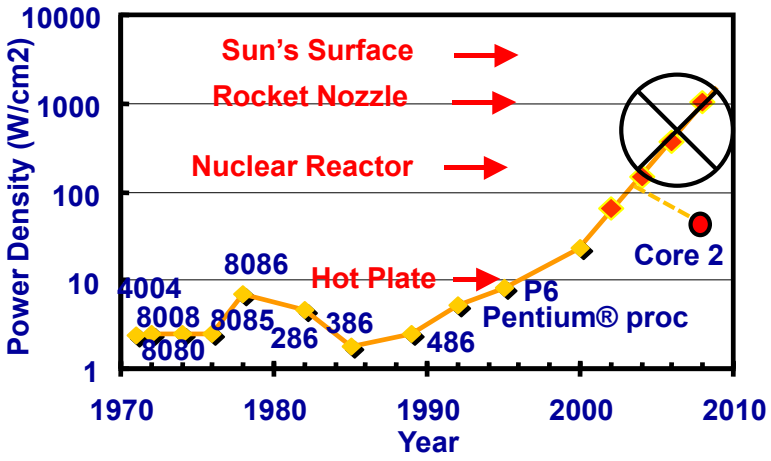

Figure 1.1 Today, typical CMOS microprocessors operate at around the power density of a nuclear reactor, *e.g.* 65 W and 130 W for Intel® CoreTM2 Duo E6320 (die size of 143 mm^2) and Intel® CoreTM i7-990X (die size of 239 mm^2), respectively. Courtesy of Shekhar Y. Borkar, Intel Corp. [1].

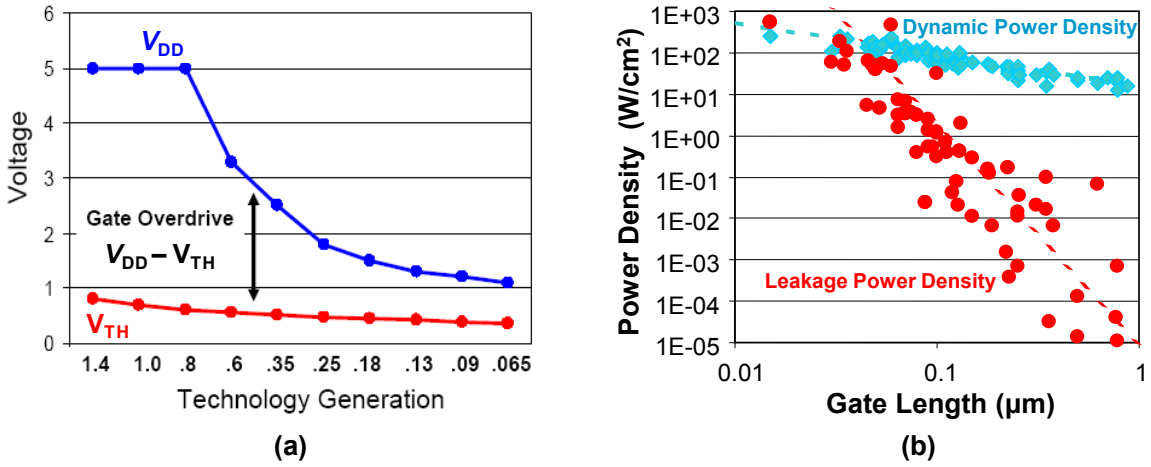

Figure 1.2 (a) Scaling trend of the supply (V_{DD}) and threshold voltage (V_{TH}) with CMOS technology generation (adapted from [2]). (b) Scaling trend of the power density with gate length (L_G); leakage power density has exponentially increased with L_G scaling (adapted from [3]).

The root cause for the slowdown in V_{DD} scaling is attributed to the non-scalability of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) threshold voltage (V_{TH}, voltage defined as the gate voltage at which a transistor turns *on* and *off*). Since the MOSFET is not an ideal switch, the *off*-state leakage current (I_{OFF}) is non-zero (Fig. 1.3) and hence dissipates power even when it is supposed to be *off* (Fig. 1.2(b)) [3]. Furthermore, the non-ideal switching characteristics imply that there is a finite steepness at which a MOSFET can switch from *on* to *off*-state. This factor is defined as subthreshold swing (S) which measures the amount of voltage

is required to modulate the current by one-order of magnitude (Fig. 1.3). This can be formulated as [4]:

$$S = \left(\frac{\partial \log I_D}{\partial \log V_G} \right)^{-1} = \frac{\partial V_G}{\partial \varphi_S} \frac{\partial \varphi_S}{\partial \log I_D} = \left(1 + \frac{C_{DEP}}{C_{OX}} \right) \left(\frac{kT}{q} \ln 10 \right) \geq \left(\frac{kT}{q} \ln 10 \right)$$

The first term in the right-hand side defines the coupling efficiency of the gate voltage to the channel potential, and is greater than 1 for a typical MOSFET operation. The second term defines a factor associated with the thermal (Boltzmann) distribution of mobile charge carriers and is fundamentally limited to 60 mV/dec at room temperature. This means that even if the gate voltage could couple perfectly to the surface potential (so that $1+C_{DEP}/C_{OX} = 1$, or $C_{OX} >> C_{DEP}$), at least 60 mV of gate voltage is required to change the current by one order of magnitude.

This fundamental limit in S describes why V_{TH} cannot be scaled aggressively in a MOSFET. As V_{TH} is decreased, I_{OFF} increases exponentially, resulting in exponentially larger leakage power dissipation (Fig. 1.4) [5]. On the other hand, if V_{TH} were too high, then there would not be sufficient gate overdrive voltage to operate chips at high speed (Fig. 1.4) [5]. The resultingtradeoff between power (energy) dissipation and speed (delay) sets a fundamental energy efficiency limit for CMOS technology.

To achieve improvements in system performance without increasing transistor operating speed, parallel computing has been employed in microprocessor design (Fig. 1.5) [6]. Parallelism allows for reduced energy per operation by running at reduced clock speed while maintaining system performance by operating multiple cores in parallel. However, the power savings offered by parallel computing will eventually reach a limit when each core operates at the minimum energy defined by device-level constraints [7].

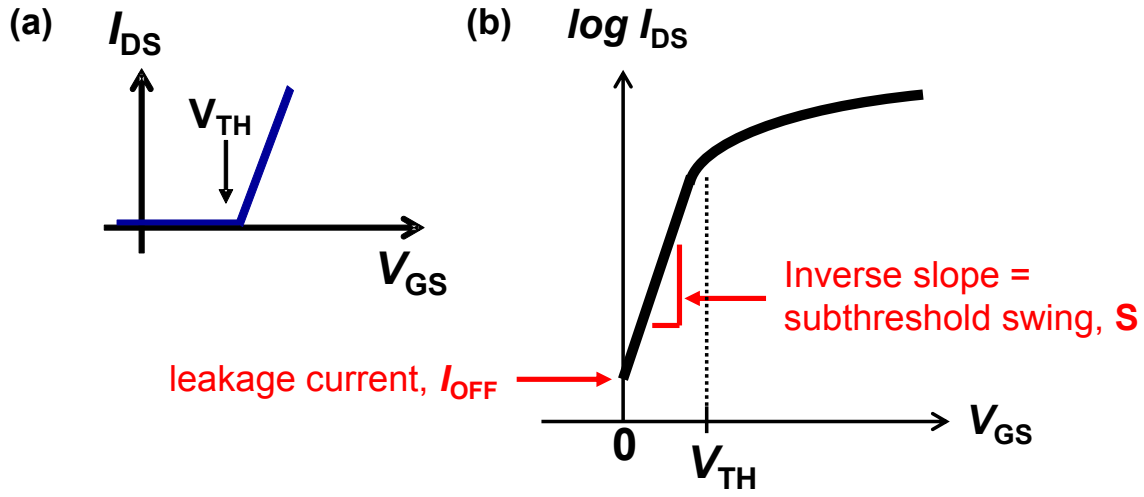

Figure 1.3 An example of a MOSFET transfer (I_{DS} *vs.* V_{GS}) characteristics in (a) linear current scale and (b) log current scale. Since MOSFET is not an ideal switch, off-state current (I_{OFF}) is non-zero and results in large leakage power. The inverse slope of the I_{DS}-V_{GS} characteristics is the subthreshold swing (S).

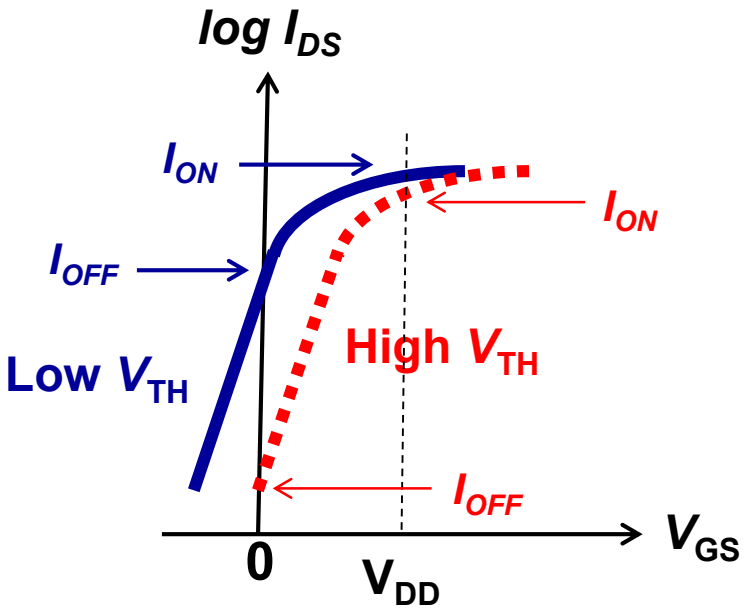

Figure 1.4 A schematic demonstrating the impact of V_{TH} scaling. If V_{TH} were too low, then I_{OFF} would increase exponentially resulting in a large leakage power; if V_{TH} were too high, then I_{ON} would be too small resulting in slower circuit operating speed.

1.2 Design Requirements for a New Switch

It has been highlighted that increasing power density is a challenge for continued MOSFET scaling, due to non-scalability of subthreshold swing which limits the extent to which the MOSFET threshold voltage and hence the supply voltage can be reduced for a given performance target and optimal energy efficiency. In order to address this issue, alternative transistor designs which can achieve steeper switching behavior ($S < 60$ mV/dec at room temperature) than the MOSFET is required.

A new device with steeper switching characteristics would allow for a significant reduction in V_{TH} and hence V_{DD}. This means that for a given I_{OFF} specification, a new device can achieve the required I_{ON} at a significantly lower voltage, resulting in reduced dynamic energy as compared to a MOSFET. Furthermore, for a given delay specification, a steeper switching device will achieve much lower I_{OFF}, yielding reduced leakage energy. These translate to an overall improvement in the energy efficiency.

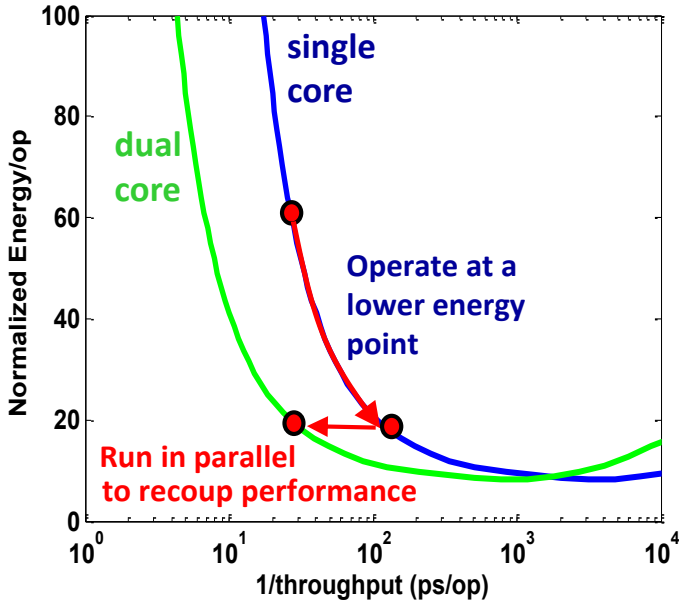

Figure 1.5 A single-core processor can operate at lower energy per operation by running at reduced clock speed. The system performance can be recovered by operating two single-core processors in parallel [6].

The improvement in energy efficiency should also be accompanied by sustainable device speed. A new device which offers significant improvement in energy efficiency, but only at extremely slow speeds may not be attractive for practical application. Hence a large *on* to *off*-state current ratio with large I_{ON} is a necessary requirement to be competitive with CMOS.

A new switch should also be cost effective. Hence it is preferable that the fabrication of the new switch utilizes the well-established CMOS infrastructure and be compatible with the existing CMOS process flow. The layout area required should also be comparable to CMOS designs.

1.3 The Proposed Solution

Previous sections have highlighted that the switching behavior of a MOSFET was fundamentally limited to 60 mV/dec due to carrier injection that obey Boltzmann statistics. As a result, a new switch with dramatically different carrier injection mechanism needs to be explored. This thesis explores the tunnel field effect transistor (TFET) as an alternative switching device to overcome the fundamental limit in subthreshold swing and hence the energy efficiency of CMOS. TFETs rely on carrier injection via band-to-band tunneling (BTBT) and the absence of thermal (kT) dependence allows for the subthreshold swing to be steeper than 60 mV/dec [8]. It will be shown that by employing Germanium (Ge) only in the source region of the TFET, I_{ON}/I_{OFF} ratio can be greatly enhanced to provide for significant energy savings compared to CMOS [9].

1.4 Thesis Outline

This dissertation aims to address the promise and challenges associated with Ge-source TFET technology in achieving "greener" electronic devices. Experimental results based on CMOS compatible process flow will demonstrate steeper than 60 mV/dec switching characteristics. The calibrated BTBT model will be employed in Technology Computer Aided Design (TCAD) to gain deeper understanding of the device physics and provide for advanced design optimization at the device level. The applicability of Ge-source TFETs for digital logic and the necessary design changes will also be examined.

Chapter 2 introduces the fundamentals of a TFET. The differences in the device structure and the accompanying carrier injection mechanism with respect to a MOSFET will be discussed. The physics of BTBT based on Kane's formulation is summarized, followed by discussion on point *vs*. line tunneling. An overview of the BTBT model used in TCAD analysis is provided.

Chapter 3 presents a new TFET design - planar Germanium-source TFET - which employs a small bandgap material (Ge) in the source region of the device to achieve steep switching behavior and enhance the tunneling current. It will be experimentally demonstrated that the planar Ge-source TFET can achieve a record high I_{ON}/I_{OFF} ratio ($> 10^6$) for low supply voltage ($V_{DD} = 0.5$ V) operation. The BTBT model parameters used by the device simulation package (Sentaurus Device) are calibrated to the experimental data and then used for a design optimization study.

Chapter 4 addresses the limitations associated with the planar design and proposes an improved Ge-source TFET structure. The raised Ge-source TFET is demonstrated to suppress "parasitic" lateral tunneling and achieve steeper switching behavior and higher I_{ON} for an even lower supply voltage operation ($V_{DD} < 0.5$ V). The performance of this new TFET design is benchmarked against that of CMOS technology and other Ge-source TFET designs, and is shown to offer lower energy per operation for frequency range up to 1 GHz for sub-0.5 V operation. Device fabrication and measurement results are presented and discussed.

Chapter 5 examines the application of the optimized Ge-source TFET design for digital logic. Challenges for TFET technology in logic design are addressed. In order to mitigate design constraints, a circuit-level solution based on n-TFET pass transistor logic is proposed and demonstrated through mixed-mode simulations. The accompanying design modifications required at the device level are discussed.

Chapter 6 summarizes the key results and contributions to this work. Suggestions for future research directions are offered.

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Chapter 2

Tunnel Field Effect Transistor Design and Operation

2.1 Introduction

The previous chapter motivated the need for a new switch in order to address the rapid rise in power consumption associated with today's Complementary Metal-Oxide-Semiconductor (CMOS) technology and proposed that a Tunnel Field Effect Transistor (TFET) can offer a promising solution for reduced operating voltage (V_{DD}). This chapter is devoted to the discussion of the TFET operating principle and understanding the physics behind the steep switching characteristics. It will begin with a comparative analysis of TFET *vs*. Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET); the fundamental differences in terms of device structure and current injection mechanism will be presented. Then the physics of Band-to-Band Tunneling (BTBT) phenomena based on Wentzel-Kramers-Brillouin (WKB) approximation will be derived, after which the incorporation of the BTBT model in Technology Computer Aided Design (TCAD) will be investigated. Subsequent sections will present two BTBT modes (lateral *vs*. vertical tunneling) that can be employed in a TFET. It will be proposed that the vertical tunneling in the direction perpendicular to the semiconductor/gate-dielectric interface offers multiple advantages which make it attractive over the original TFET design.

2.2 MOSFET vs. TFET

Fig. 2.1(a) and (b) show the cross-sectional schematics of an n-channel MOSFET and TFET, respectively. The only structural difference associated with a TFET is in the asymmetrically doped source and drain regions (p^+-i-n^+) *vs*. symmetrically doped source and drain regions (n^+-p-n^+) of a MOSFET [1,2].

The nomenclatures for the voltage terminals (source, drain, and gate) and the corresponding biasing scheme to define *on* ($V_{GS} = V_{DS} = V_{DD}$) and *off*-state ($V_{GS} = 0$ V, $V_{DS} = V_{DD}$) remain identical for both devices. This seemingly trivial difference in terms of the device structure, however, results in a profound difference in terms of the carrier injection mechanism and its accompanying physics.

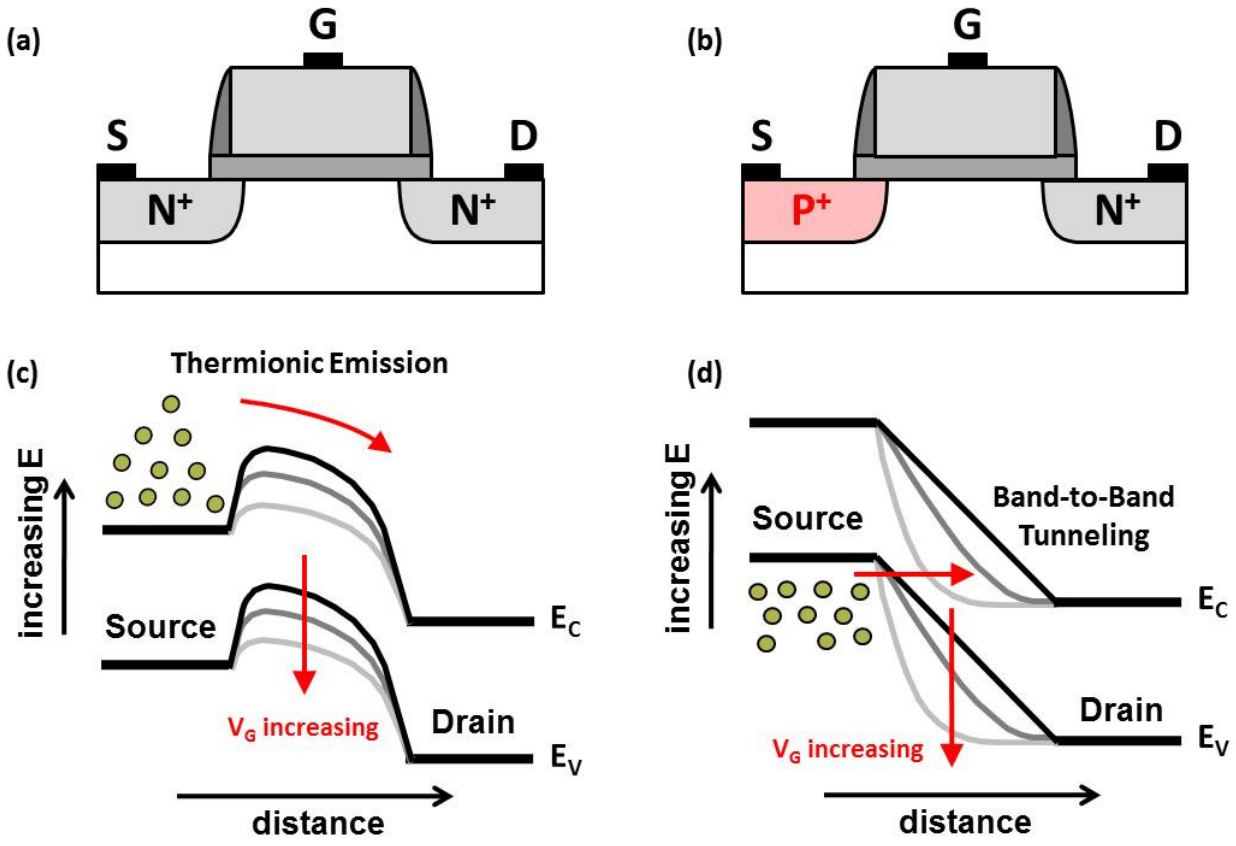

Fig. 2.1 Schematic cross-sections for n-channel (a) MOSFET and (b) TFET. (c) The operation of a MOSFET is based on gate-voltage (V_G) modulation of the channel potential for the injection of carriers *over* the barrier height from the source into the channel region through a process called thermionic emission. (d) The operation of a TFET is also based on gate-voltage modulation of the channel potential, but the carriers are injected into the channel *through* the potential barrier via band-to-band tunneling.

The operation of a MOSFET relies on gate-voltage modulation of the channel potential for the injection of carriers from the source into the channel region through a process called thermionic emission (Fig. 2.1(c)) [3]. These carriers (electrons for an n-channel and holes for a p-channel MOSFET) are thermally distributed in the source region of the device according to the Boltzmann distribution, and the resulting current can be expressed as [3]:

$$I_{Thermionic} \simeq \exp\left[\frac{V_{GS}}{nV_T}\right] \qquad (1)$$

In the *off*-state, the potential barrier seen by the carriers from the source region is large, and the resulting current (*off*-state leakage, I_{OFF}) is small (Fig. 2.1(c)). Note that this current is not zero (in contrast to an ideal switch), since the thermal (exponential) distribution of carriers still permit a finite number of carriers to be injected over the large potential barrier.

In the *on*-state, the gate voltage lowers channel potential barrier, and results in an exponential carrier injection from the source region into the channel (hence exponential current modulation) (Fig. 2.1(c)). Note that as described in Section 1.1, the thermal (Boltzmann) distribution of mobile charge carriers in the source region ultimately defines how steeply a MOSFET can switch from *on* to *off*-state. The steepness, defined by the amount of voltage required to modulate the current by one-order of magnitude, is called the subthreshold swing (S) and is limited to 60 mV/dec at room temperature [4]:

$$S = \left(\frac{\partial \log I_D}{\partial \log V_G}\right)^{-1} = \frac{\partial V_G}{\partial \varphi_S}\frac{\partial \varphi_S}{\partial \log I_D} = \left(1+\frac{C_{DEP}}{C_{OX}}\right)\left(\frac{kT}{q}\ln 10\right) \geq \left(\frac{kT}{q}\ln 10\right) \qquad (2)$$

The subthreshold swing observed for the state-of-the-art MOSFET technology is approximately 90 to 100 mV/dec [5-7]. This number is expected to degrade with advancing technology nodes due to problems (*i.e.* short channel effect) associated with scaling down the transistors to extremely small dimensions. This will further prevent the reduction of the threshold and supply voltages.

The operation of a TFET also relies on gate-voltage modulation of the channel potential for the injection of carriers (electrons for an n-channel and holes for a p-channel MOSFET) from the source into the channel region. However, in contrast to an injection *over* the potential barrier (*i.e.* thermionic emission) in a MOSFET, the carriers are injected into the channel *through* the potential barrier via a process called band-to-band tunneing (BTBT) (Fig. 2.1(d)) [8-10]. Although a detailed discussion on the tunneling phenomena will be presented in Section 2.3, the main advantage associated with BTBT is that the energy band gap (of magnitude E_G) cuts off the Boltzmann "tail" of the electrons in the p-type source region (holes for the n-type source region) (Fig. 2.1(d)) [11-12]. This lack of thermal ('kT') dependence permits sharper than 60 mV/dec turn-on characteristics at room temperature, when the conduction band of the channel overlaps with the valence band of the source region. The resulting tunneling current can be expressed as (details shown in Section 2.3) [10]:

$$I_{BTBT} \simeq A\varepsilon^2 \exp\left[-\frac{B}{\varepsilon}\right] \qquad (3)$$

where A and B are material dependent parameters. When a TFET is in the *off*-state, the p-i-n structure of a TFET is reverse-biased and hence the diode leakage current comprises the dominant source of I_{OFF}, which is significantly smaller than the MOSFET I_{OFF} [13].

2.3 Physics of Band-to-Band Tunneling

BTBT is a quantum mechanical phenomenon in which the electrons "tunnel" across the energy gap of a semiconductor. From a physical perspective, BTBT is the plucking of electrons from covalent bonds formed between the semiconductor atoms. In order to understand how the BTBT process can achieve a steep subthreshold swing, this section is devoted to the derivation of the BTBT generation rate (G_{BTBT}). It will begin by elaborating the general tunneling framework and the underlying assumptions to be used for the derivation. Then the tunneling probability (T), current (J), and generation rate will be derived based on WKB approximation. The end result will present important physical parameters that must be optimized for large BTBT rate.

2.3.1 Underlying Assumptions for Derivation

The original expression for the tunneling probability was derived by Kane using time-dependent perturbation theory and Fermi's Golden Rule [8-9]. This section will instead employ a simplified and more intuitive approach to perform the same task based on the Wentzel-Kramers-Brillouin (WKB) approximation [14]. The calculation will be based on tunneling across a reverse-biased p-n junction as shown in Fig. 2.2.

In order to obtain a closed form solution of the BTBT generation rate, the following assumptions are necessary:

A) Assume a direct band-gap semiconductor so that the momentum contribution from the phonon scattering can be ignored and that a closed form solution for BTBT generation rate can be obtained [10].
B) Assume high doping levels in the semiconductor such that the Fermi levels align perfectly with the valence band of the p-type semiconductor ($E_V = F_P$) and the conduction band of the n-type semiconductor ($E_C = F_N$). Also assume that the valence band states are completely occupied by electrons and conduction band states completely empty so that the carrier statistics (Fermi distribution) are simplified (*i.e.* $f_V - f_C = 1$).
C) Assume a constant electric field across the p-n junction, as shown by the constant-slope energy lines in Fig. 2.2.
D) Assume symmetric 2-band relation to model the imaginary wave vector dispersion relation within the band gap [15]. This form shows correct behavior at the band edges and also allows for closed form solution of G_{BTBT}.

2.3.2 Calculation of the Imaginary Dispersion Relation

From WKB theory, the tunneling probability (T) is expressed as [14]:

$$T \simeq \exp\left[-2\int_{x_1}^{x_2} k(x)dx\right] \qquad (4)$$

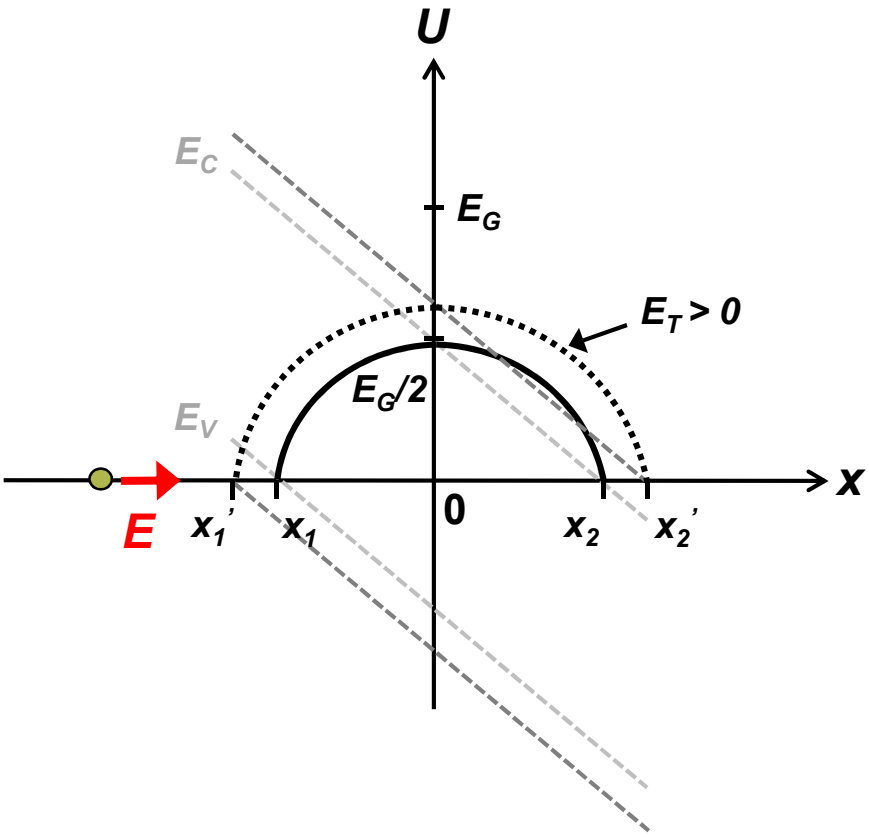

Fig. 2.2 A schematic of the energy-band diagram within the depletion region of a p-n junction, showing the constant-slope lines (grey) representing uniform electric field. The imaginary dispersion relation can be approximated by symmetric 2-band relation. E is the energy of the incident electron and U the potential barrier height. Introduction of the energy (E_T) associated with the transverse momentum modifies the classical turning points to x_1' and x_2'.

where x_1 and x_2 are the classical turning points. In order to evaluate Eq. (4), the imaginary wave vector dispersion relation, $k(x)$, needs to be defined. From the general E-k relationship [14]:

$$k(E_X) = \sqrt{\frac{2m^*}{\hbar^2}(E_X - U)} \qquad (5)$$

where E_X is the energy of the incident carrier and U is the potential barrier height seen by the carriers within the band gap (Fig. 2.2). U can be calculated using the symmetric 2-band relation [15] assuming uniform electric field across the p-n junction (Fig. 2.2).

$$E_X - U = c\left(x - \frac{E_G}{2q\varepsilon}\right)\left(x + \frac{E_G}{2q\varepsilon}\right) \qquad (6)$$

From the boundary condition ($U = E_G/2$ at $x = 0$) associated with uniform electric field, the constant prefactor c can calculated, after which the final expression for U can be determined:

$$E_X - U = -2\left[\frac{\left(\frac{E_G}{2}\right)^2 - (q\varepsilon x)^2}{E_G}\right] \qquad (7)$$

For tunneling in a 3-D semiconductor, the total momentum of the incident electrons consists of the momentum in the tunneling direction and transverse to the tunneling direction. The energy associated with transverse momentum is accounted for by the introduction of the term E_T to Eq. (7) [10].

$$E_X - U = -\left[2\frac{\left(\frac{E_G}{2}\right)^2 - (q\varepsilon x)^2}{E_G} + E_T\right] \qquad (8)$$

Hence, the expression for tunneling probability becomes:

$$T(E_X, E_T) \simeq \exp\left[-2\int_{x_1'}^{x_2'}\sqrt{\frac{2m^*}{\hbar^2}\left[2\frac{\left(\frac{E_G}{2}\right)^2 - (q\varepsilon x)^2}{E_G} + E_T\right]}dx\right] \qquad (9)$$

Note that the integration limit changes from x_1 and x_2 to x_1' and x_2' with the introduction of E_T since transverse momentum leads to an additional damping factor of the wave function and modifies the classical turning points resulting in increased effective tunnel barrier thickness (x_1' and x_2' in Fig. 2.2) [15]. The new turning points can be evaluated by:

$$2\frac{\left(\frac{E_G}{2}\right)^2-(q\varepsilon x)^2}{E_G}+E_T=0 \qquad (10)$$

$$\therefore x'_{1,2}=\pm\frac{1}{q\varepsilon}\left[\left(\frac{E_G}{2}\right)^2+\left(\frac{E_G E_T}{2}\right)\right]^{\frac{1}{2}} \qquad (11)$$

In order to evaluate the integral in eq. (9), the following coordinate transformation is performed [15]:

$$y=\frac{q\varepsilon}{\left[\left(\frac{E_G}{2}\right)^2+\left(\frac{E_G E_T}{2}\right)\right]^{\frac{1}{2}}}x \qquad (12)$$

Using eq. (12) in (9), tunneling probability is simplified to [15]:

$$T(E_X,E_T)\simeq\exp\left[-2\int_{-1}^{1}\sqrt{\frac{2m^*}{\hbar^2}}\frac{\left(\frac{E_G}{2}\right)^2+\left(\frac{E_G E_T}{2}\right)}{q\varepsilon E_G^{\frac{1}{2}}}(1-y^2)^{\frac{1}{2}}dy\right] \qquad (13)$$

Evaluating the integral and rearranging:

$$T(E_X,E_T)\simeq\exp\left[-\frac{\pi m^{*\frac{1}{2}}E_G^{\frac{3}{2}}}{2\sqrt{2}q\varepsilon\hbar}\right]\exp\left[-\frac{\sqrt{2}\pi m^{*\frac{1}{2}}E_G^{\frac{1}{2}}}{2q\varepsilon\hbar}E_T\right]=T_O\exp\left[-\frac{E_T}{E_O}\right] \qquad (14)$$

where $E_O=\dfrac{\sqrt{2}q\varepsilon\hbar}{\pi m^{*\frac{1}{2}}E_G^{\frac{1}{2}}}$

2.3.3 Calculation of the BTBT Current and Generation Rate

Using the expression for tunneling probability (Eq. 14), the differential tunneling current density (*dJ*) can be calculated as [15]:

dJ = (charge) × (velocity in k-space) × (number of states per unit volume in k-space) × (probability of tunneling) × (occupancy of the states)

$$\therefore dJ=q\cdot\left(\frac{1}{\hbar}\frac{\partial E_X}{\partial k_X}\right)\cdot\left(\frac{2}{(2\pi)^3}dk_X dk_Y dk_Z\right)\cdot T(E_X,E_T)\cdot(f_V-f_C) \qquad (15)$$

The velocity of the incident electrons has been expressed as the group velocity of the valence band electron wave packet [14]. Eq. (15) can be further simplified by assuming that the valence band is completely occupied by electrons and conduction band is empty, so that $f_V - f_C = 1$. The transverse momentum (k_Y, k_Z) can also be expressed in terms of transverse wave vector, k_t [10]:

$$k_T^{\,2} = k_Y^{\,2} + k_Z^{\,2} \qquad (16)$$

$$dk_Y dk_Z = 2\pi k_T dk_T \qquad (17)$$

Then transverse dispersion relationship is used to change the coordinates from momentum to energy space [10]:

$$E_T = \frac{\hbar^2 k_T^{\,2}}{2m^*} \qquad (18)$$

$$2\pi k_T dk_T = \frac{2\pi m^*}{\hbar^2} dE_T \qquad (19)$$

Substituting Eq. (19) into Eq. (15), the expression for the differential tunneling current reduces to:

$$dJ = \frac{qm^*}{2\pi^2\hbar^3} T(E_X, E_T) dE_X dE_T \qquad (20)$$

The tunneling current (J) can be evaluated by integrating both the normal and transverse energies:

$$J = \frac{qm^*}{2\pi^2\hbar^3} \int_{F_P=0}^{F_N} \int_0^E T(E_X, E_T) dE_T dE_X \qquad (21)$$

Note that the integration limit for the energy along the tunneling direction is from the Fermi level of the n-type semiconductor to the Fermi level of the p-type semiconductor (entire overlap between p-type valence band and n-type conduction band), since it has been assumed that the Fermi levels align with the band edges. The upper limit for the integration of the transverse energy extends to E ($E_{MAX} = E_G/2$) since $E_T > E$ results in tunneling into forbidden states [10]. However, since the tunneling probability decays exponentially with E_T, it is reasonable to extend this upper limit to ∞ without losing generality [10] and for computational simplicity.

The BTBT generation rate (G_{BTBT}) can be calculated from (21) by changing the coordinates from energy to position, and is expressed as:

$$G_{BTBT} = \frac{qm^*}{2\pi^2\hbar^3} \left(\frac{1}{q} \frac{\partial E_X}{\partial x} \right) \int_0^\infty T(E_X, E_T) dE_T \qquad (22)$$

Since a constant electric field ε was assumed, the energy is linearly proportional to the position by the following relationship [16]:

$$E_X = q\varepsilon x, \quad \frac{dE_X}{dx} = q\varepsilon \qquad (23)$$

Substituting Eq. (23) into (22), the generation rate reduces to:

$$G_{BTBT} = \frac{qm^*\varepsilon}{2\pi^2\hbar^3}\int_0^\infty T_O \exp\left[-\frac{E_T}{E_O}\right] dE_T \qquad (24)$$

Evaluating Eq. (24), a closed form expression for the BTBT generation rate can be obtained:

$$G_{BTBT} = \frac{qm^*\varepsilon}{2\pi^2\hbar^3} T_O \int_0^\infty \exp\left[-\frac{E_T}{E_O}\right] dE_T = \frac{qm^*\varepsilon}{2\pi^2\hbar^3} T_O E_O \qquad (25)$$

$$\therefore G_{BTBT} = \frac{\sqrt{2}q^2 m^{*\frac{1}{2}}}{2\pi^3\hbar^2 E_G^{\frac{1}{2}}}\varepsilon^2 \exp\left[-\frac{\pi m^{*\frac{1}{2}} E_G^{\frac{3}{2}}}{2\sqrt{2}q\varepsilon\hbar}\right] = A\varepsilon^2 \exp\left[-\frac{B}{\varepsilon}\right] \qquad (26)$$

where $A = \frac{\sqrt{2}q^2 m^{*\frac{1}{2}}}{2\pi^3\hbar^2 E_G^{\frac{1}{2}}}$, $B = \frac{\pi m^{*\frac{1}{2}} E_G^{\frac{3}{2}}}{2\sqrt{2}q\hbar}$

Although aforementioned assumptions were necessary to derive the BTBT generation rate in a closed form, Eq. (26) still provides for valuable information regarding the tunneling phenomena. The observation of the tunneling coefficients A and B indicates that they are inherently material dependent parameters, and that smaller E_G and m^* will result in exponentially larger BTBT current (since pre-exponential factor B has greater sensitivity to the generation rate). Hence, TFETs employing Germanium (Ge, E_G = 0.66 eV) [17] or Indium Arsenide (InAs, E_G = 0.36 eV) [18] are expected to show significantly larger I_{ON} as compared to a Si TFET. Furthermore, Eq. (26) suggests that a large electric field (ε) is a key factor to enhance BTBT. Optimized electrostatics accompanied by the use of smaller band gap materials are the two most significant factors in TFET performance, which are the motivation for the study of Ge-source TFET (to be discussed in Chapter 3) [19].

2.4 TCAD Overview and BTBT Model Calibration

Throughout the rest of the chapters, TCAD will be heavily used to design and analyze the performance of the TFET. Hence, it is imperative to understand the underlying models and physics used by the device simulators.

In the analysis of a TFET, the BTBT model that can accurately capture the tunneling phenomena is of particular interest. In this regard, Synopsys Sentaurus Device (S-Device) was adopted for this purpose. The previous versions of S-Device required a manual definition of the tunneling paths and angles, and the resulting BTBT current altered drastically with various changes [20]. However, with its recent release of the dynamic non-local BTBT model, S-Device can dynamically determine the tunneling paths according to the gradient of the energy bands, and is applicable to arbitrary tunneling barriers with non-uniform electric field and abrupt or graded heterojunctions [21]. This model accounts for direct and phonon-assisted tunneling processes, and reduces to Kane's [8] and Keldysh's model [22] in the uniform electric field limit (Eq. (26). It is the basis for all of the BTBT models used in the commercial device simulators.

The use of the dynamic non-local BTBT model requires user definition of the pre-exponential and exponential terms (A and B coefficients in Eq. (26), respectively) of the BTBT generation rate. While Sentaurus offers experimentally calibrated A and B factors for Silicon, they are not defined for low band gap materials such as Ge. Hence, for the analysis of the Ge-source TFET (details of which will be discussed in Chapter 3), the BTBT model needs to be calibrated to obtain simulation results that are physically plausible. This has been performed based on the experimental results of the fabricated Ge-source TFET (Fig. 2.3(a)) by simulating the actual structure and tuning the A and B coefficients for the best fit with the measured transfer characteristics (Fig. 2.3(b)) [23]. (Discussion on the device structure and the measurement results will be provided in Chapter 3.) The fitted coefficients are $A = 10^{17}$ $cm^{-3}s^{-1}$ and $B = 2.5 \times 10^{6}$ Vcm^{-1}. (Latest calibration including the trap energy states associated with poly-crystalline Ge yielded $A = 1.46 \times 10^{17}$ $cm^{-3}s^{-1}$ and $B = 3.59 \times 10^{6}$ Vcm^{-1} which are subsequently used for the analysis of Ge-source TFETs.)

2.5 Lateral *vs.* Vertical Tunneling

In designing a TFET based on BTBT, there are two different tunneling modes that can be employed depending on the device structure. The first is lateral tunneling in which the electrons are injected from the source to the channel region largely in a direction parallel to the semiconductor/gate-dielectric interface (referred to as "point" tunneling in [24]). This is the basic mode of operation for a conventional TFET (Fig. 2.4(a) and (c)). In order to achieve high tunneling rate, the source region should be heavily doped so that the energy band bending of the source to channel junction is steep (Fig. 2.4(c)) [25-27]. The source region should also align with the gate edge; if the gate partially overlaps the source, then the depletion at the edge of the source region would result in degraded BTBT due to reduction in the abruptness of the energy band profile; gate to source underlap would also result in a degraded tunneling rate [28-29].

A TFET based on lateral BTBT offers an advantage in terms of the ease of device fabrication. In comparison to a standard CMOS process flow, the only additional step required is a separate and opposite-dopant ion implantation for source and drain regions. However, the design window reduces significantly when the impact of physical parameters on the electrical characteristics is considered. In order to achieve steep switching characteristics, the edge of the source region should be perfectly aligned to the gate edge [29-30]. Furthermore, the doping gradient from the

source to the channel should essentially be eliminated to attain large energy band bending. The simulations have demonstrated that the sensitivity of the subthreshold swing to the doping gradient is large, and S degrades rapidly with increasing doping gradient [30]. Another fundamental limitation in the lateral BTBT is that the tunneling area is fundamentally small. Since it relies on BTBT from source to channel, the tunneling area is localized by the inversion layer thickness which is typically 2~3 nm in the *on*-state.

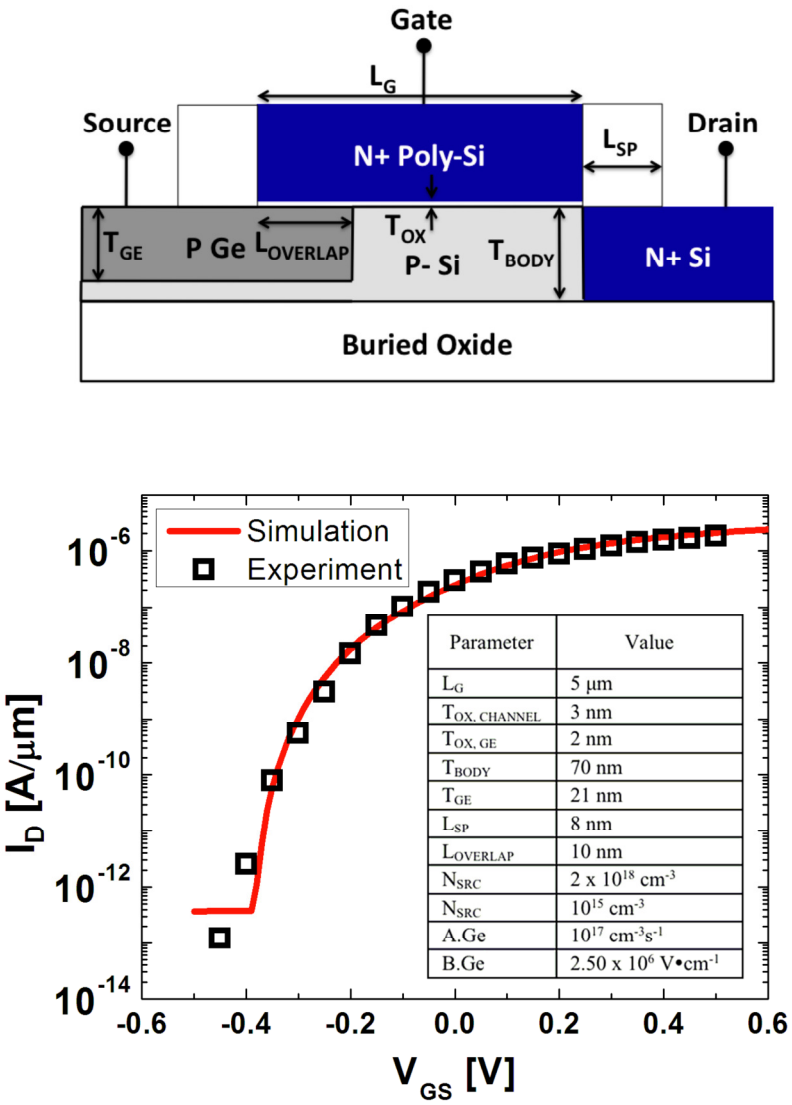

Fig. 2.3 (a) Schematic cross-section of the fabricated Ge-source TFET structure which was used to calibrate the A and B coefficients of the BTBT model used in Sentaurus Device. (b) Simulated and measured I_D-V_{GS} characteristics of a Ge-source TFET for V_{DS} = 0.5 V. The device design parameter values used for the simulation, based on [19], are shown in the inset.

Another type of BTBT mode that can be employed for a TFET design is vertical tunneling in which the electrons tunnel within the source region largely in the direction perpendicular to the semiconductor/gate-dielectric interface (Fig. 2.4(b) and (d)) (referred to as "line" tunneling in [24]). Similar to Gate-Induced Drain Leakage (GIDL), the existence of a sufficient gate to source overlap region (L_{OV}) allows for the electrons to be injected from within the source to the inverted surface region of the source (Fig. 2.4(d)) [31]. In addition to the requirement for a gate to source overlap area, the doping of the source must be moderate to allow for significant energy band bending within the source, and the depth of the source region must be thicker than the depletion width (*i.e.* ~15 nm for moderately doped Ge) [13, 32].

A TFET based on vertical BTBT can provide for improved I_{ON}. Since the gate-to-source overlap region determines the tunneling area, I_{ON} can be modulated by changing L_{OV} [23]. Furthermore, since BTBT takes place within the source region, subthreshold swing is significantly less sensitive to the doping gradient across the source to channel junction [13].

Since the introduction of the gate to source overlap region requires isotropic and selective Si etch process, the fabrication challenge is inherent. However, as exemplified by the Intel's embedded Silicon-Germanium (SiGe) source and drain process for p-channel MOSFETs [5], the source recess etch has become a standard fabrication process and can be achieved with relative ease. The recessed source profile then allows for a selective deposition of low-band-gap materials (*i.e.* Ge) in the source region which can enhance I_{ON} to a greater extent.

2.6 Summary

This chapter reviewed the fundamental differences between a TFET and a MOSFET. The asymmetrically doped source and drain regions of a TFET result in a current injection mechanism that is drastically different from thermionic emission in a MOSFET; the absence of thermal ('kT') dependence in BTBT permits for steeper than 60 mV/dec switching characteristics.

In order to gain an in-depth understanding of the tunneling phenomena, the physics of BTBT was presented. Based on WKB approximation and aforementioned assumptions, the equation for BTBT generation rate was derived. The end result demonstrates that materials with small band gap and carrier effective mass can greatly enhance the tunneling current.

Two BTBT modes can be used in a TFET design. The conventional TFET structure, which is based on lateral tunneling (in the direction parallel to the semiconductor/gate-dielectric interface), is fundamentally limited to small I_{ON} due to reduced tunneling area and degraded BTBT generation rate associated with doping gradient from source to channel region. On the other hand, a TFET structure with gate-to-source overlap area to achieve vertical tunneling in the direction perpendicular to the semiconductor/gate-dielectric interface offers improved robustness to process-induced variations and higher I_{ON}. This is the motivation for the study of the Ge-source TFET which will be presented in next chapter.

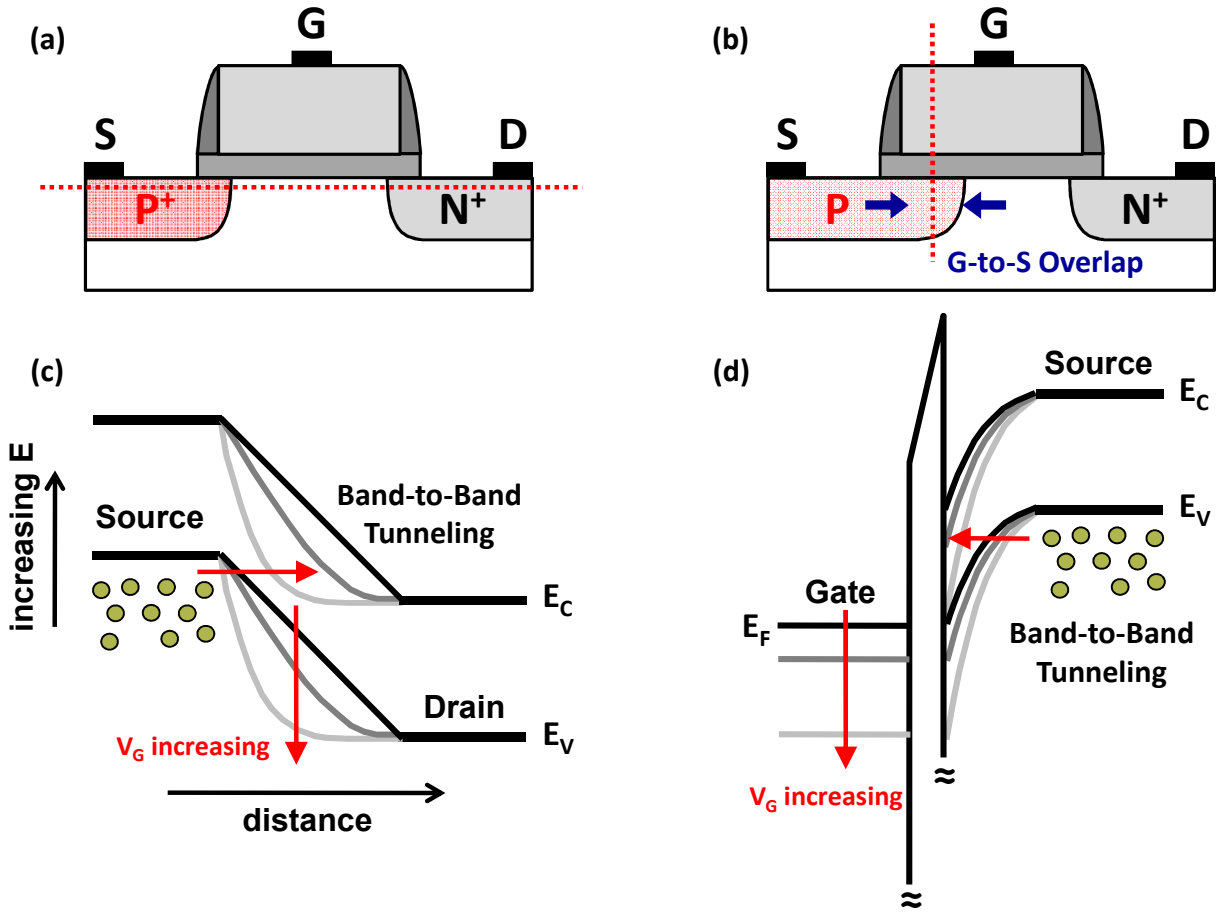

Fig. 2.4 Schematics for n-channel TFET based on (a) lateral tunneling and (b) vertical tunneling. (c) Energy band diagram showing lateral electron injection from the source to the channel region in direction parallel to the semiconductor/gate-dielectric interface. (d) Energy band diagram showing vertical electron injection from within the source region to the inverted surface of the source region in the direction perpendicular to the semiconductor/gate-dielectric interface.

2.7 References

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Chapter 3

Planar Germanium-Source TFET

3.1 Introduction

As discussed in the previous chapter, a TFET based on line tunneling offers multiple advantages over the conventional point tunneling TFET design [1-2]. This chapter presents a new TFET design – the planar Germanium-source TFET - which extends the benefits of line tunneling further by employing a small bandgap material (*i.e.* Ge) in the source region of the device to enhance the tunneling current. It will be experimentally demonstrated that the planar Ge-source TFET can achieve a record high on-state to off-state current ratio ($I_{ON}/I_{OFF} > 10^6$) for low supply voltage (V_{DD} = 0.5 V) operation. The experimental results are used to calibrate the device simulation package (Sentaurus Device) which will then be used for design optimization study.

3.2 The Fundamentals of Ge-Source TFET

3.2.1 Impact of Ge-Source on I_{ON}/I_{OFF}

The schematic cross section of the planar Ge-source n-channel TFET is shown in Fig. 3.1(a) [1]. Structurally, the differences between the Ge-source TFET and conventional source-to-channel tunneling TFET (Fig. 2.8(b)) are the selective use of non-degenerately doped Ge only in the source region of the device and the introduction of gate-to-source overlap area.

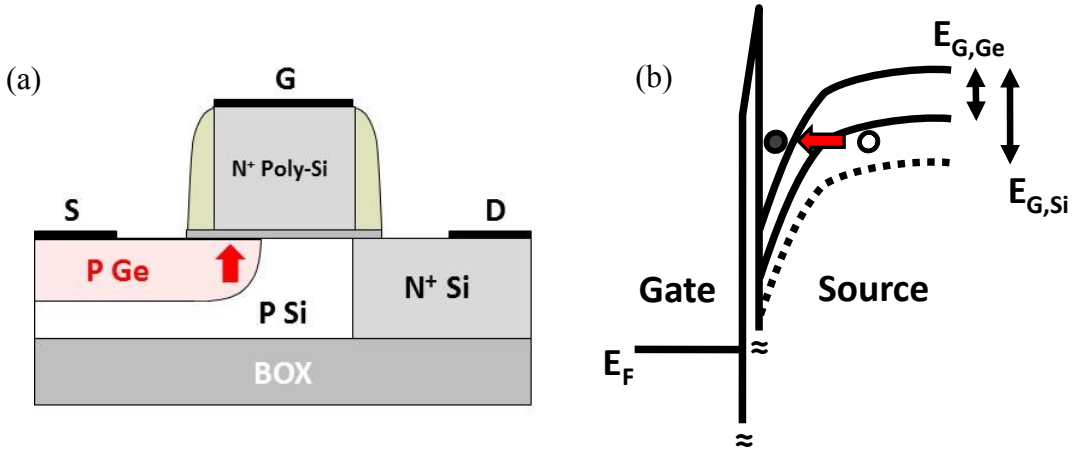

Fig. 3.1 (a) Schematic cross section of the planar Ge-source n-channel TFET. (b) The corresponding energy band diagram along the perpendicular direction of the gate-to-source overlap area showing the band bending of Ge *vs*. Si.

The selective use of Ge only in the source region of the device enhances the on-state drive current of the TFET as compared to a Si device [3-5]. From the band-to-band tunneling (BTBT) theory [6-8], the tunneling current can be formulated as:

$$I_D = AE_S \exp(-\frac{B}{E_S}) \qquad (1)$$

where A and B factors are material-dependent terms and E_S the electric field. The B factor within the exponential term has power dependence to the bandgap (E_G) and the effective mass (m^*) of the tunneling material and is expressed as [8]:

$$B = \frac{\pi m^{*\frac{1}{2}} E_G^{\frac{3}{2}}}{2\sqrt{2}q\hbar} \sim m^{*\frac{1}{2}} E_G^{\frac{3}{2}} \qquad (2)$$

Ge has approximately half the bandgap as compared to Si (0.66 eV *vs*. 1.2 eV) and smaller effective mass ($0.06m_o$ vs. $0.2m_o$) [9], whichprovide for smaller B factor and hence exponentially larger I_{ON} [3-5]. In other words, for the same gate-overdrive, Ge allows for more energy band overlap and smaller tunneling distance *vs*. Si (Fig. 3.1(b)).

In addition to the I_{ON} benefit arising from the use of Ge-source, I_{OFF} can be effectively suppressed due to the presence of Ge-Si heterojunction (Ge source to Si channel) which improves the overall I_{ON}/I_{OFF} ratio of the Ge-source TFET as compared to an all-Si or all-Ge

device. In the off state (V_{GS} = 0V and V_{DS} = V_{DD}), the n-channel TFET is reverse biased and the dominant source of I_{OFF} comprise of the reverse-bias p-i-n diode leakage [2]. In order to gain physical insight into how bandgap of a material affects the reverse-bias current, the Ideal Diode (Shockley Equation) formulation is adopted (assuming non-degenerate doping and low-level injection). The total reverse bias current (J_R) can then be approximated by the sum of the diffusion component (J_O) in the quasi-neutral region and the generation current (J_{ge}) in the depletion region [10]:

$$J_R = J_O + J_{ge} \tag{3}$$

From [10], J_O can be expressed as:

$$J_O = \frac{qD_P p_{no}}{L_P} + \frac{qD_N n_{po}}{L_N} = \frac{qD_P n_i^2}{L_P N_D} + \frac{qD_N n_i^2}{L_N N_A} \tag{4}$$

where D_P and D_N are the diffusion coefficients, L_P and L_N diffusion lengths, p_{no} and n_{po} minority carrier densities, and N_D and N_A doping densities in N-type and P-type regions, respectively. n_i is the intrinsic carrier concentration associated with a given material. Replacing the following relations for the L_P, L_N and n_i into Eq. (4) [10],

$$L_P = \sqrt{D_P \tau_P}$$
$$n_i^2 = N_C N_V \exp(-\frac{E_G}{kT})$$

the diffusion component of the diode leakage can be expressed in terms of the bandgap of the material:

$$J_O = q[\sqrt{\frac{D_P}{\tau_P}}\frac{1}{N_D} + \sqrt{\frac{D_N}{\tau_N}}\frac{1}{N_A}]N_C N_V \exp(-\frac{E_G}{kT}) \propto \exp(-\frac{E_G}{kT}) \tag{5}$$

where τ_P and τ_N are the hole and electron lifetimes, respectively, and N_C and N_V effective density of states for conduction and valence band, respectively.

In addition to the diffusion current in the quasi-neutral region, the generation current in the depletion region must be taken into account especially for large reverse biases. This can be found by integrating the electron-hole pair generation rate (U) over the depletion region (W_{DEP}):

$$J_{ge} = \int_0^{W_{DEP}} q\,|U|\,dx \approx q\,|U|\,W_{DEP} \approx \frac{qn_i W_{DEP}}{\tau_g} = \frac{qW_{DEP}}{\tau_g}\sqrt{N_C N_V}\exp(-\frac{E_G}{2kT}) \propto \exp(-\frac{E_G}{2kT}) \tag{6}$$

where τ_g is the generation lifetime.

From Eqs. (5) and (6), it can be seen that the total reverse-bias current (J_O) is exponentially dependent on -E_G. Hence, an all-Ge TFET would always exhibit orders of magnitude larger I_{OFF} as compared to an all-Si TFET. In a Ge-source TFET, however, the presence of a Ge-Si heterojunction with larger effective bandgap results in a reduced thermal leakage current [2], which enhances I_{ON}/I_{OFF}.

3.2.2 Device Operating Principle

The basic device operating principle of the Ge-source TFET is analogous to a line tunneling device [11] and is illustrated by the energy band diagram in Fig. 3.2 [2]. In the on-state, an inversion layer of electrons (channel) exists at the surface of the Si body region, and a large vertical electric field within the Ge-source induces tunneling of electrons within the Ge to the inverted surface of the Ge to provide electrons to flow through the channel. This is possible because the gate overlaps the source, and the source is not degenerately doped so that it can be inverted at reasonable gate voltages [2]. Proper device operation further requires the channel-inversion threshold voltage (*i.e.* MOS threshold voltage) to be smaller than that of the onset of BTBT, so that the drain voltage (V_{DS}) can couple to the surface potential at the Ge-source, separating the quasi-fermi levels to initiate BTBT (similar to deep depletion) [12].

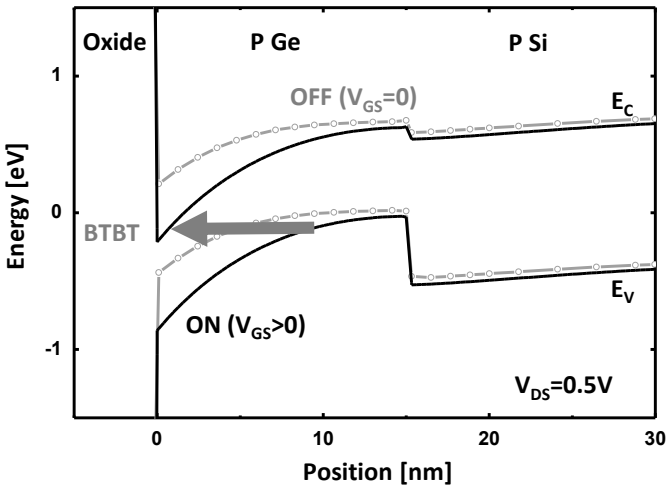

Fig. 3.2 Vertical energy band diagram along the gate-to-source overlap region for the TFET in the ON and OFF-state for the planar Ge-source TFET shown in Fig. 3.1.

3.3 Device Fabrication

N-channel TFETs (parameters listed in Table 3.1) were fabricated on (100) oriented lightly doped p-type silicon-on-insulator (SOI) wafers as follows. After thermal oxidation to thin the SOI layer down to 70 nm thickness, active areas were patterned using optical lithography and dry etching (Fig. 3.3(a)). The gate-stack consist of thermally grown SiO_2 (3 nm), N^+ poly-Si gate (150 nm), low-temperature-deposited oxide (LTO) gate-hard-mask layers (150 nm) (Fig. 3.3(b)). Si_3N_4 were deposited and anisotropically etched to form ultra-narrow gate-sidewall spacers (Fig. 3.3(b)).

After the spacer formation, masked ion implantation (1×10^{15} As^+/cm^2 at 70keV, 0^o tilt) followed by rapid thermal annealing (10 sec at 1000^oC in N_2 ambient) was used to dope the drain regions heavily n-type (Fig. 3.3(c)). Fig. 3.4 shows a plan-view scanning electron micrograph (SEM) of a TFET after the drain doping process was completed. Next, an LTO layer was deposited and patterned to selectively expose the source side of the TFET, before a highly selective and isotropic dry etching process (HBr and SF_6 based) was used to recess the Si in the source regions by ~20nm, undercutting the gate electrode to introduce the gate-to-source overlap region (Fig. 3.3(c)). Fig. 3.5 shows a cross sectional SEM image of a dummy wafer used to characterize the source recess etch process.

Native oxide was then removed in dilute HF (10 sec in 100:1 H_2O:HF) and boron-doped polycrystalline Ge (poly-Ge) was selectively deposited at 425^oC and 400mT in a hot-wall low-pressure chemical vapor deposition source gases, respectively ((LPCVD) reactor, using GeH_4 (15 sccm) and 1%BCl_3 /99%He (35 sccm) as the Ge and boron dopant Fig. 3.3(d)). The sheet resistance of the as-deposited poly-Ge layer was measured to be ~150 kΩ/□, which suggests only moderate active dopant concentration ($<10^{18}$ cm^{-3}). Another LTO (passivation) layer then was deposited (at 400^oC) and openings were patterned and etched in the LTO to allow for direct probing of the gate, source, and drain pads (Fig. 3.3(d)). Device fabrication was completed with a forming-gas anneal (30 min at 400^oC in H_2/N_2 ambient) to improve SiO_2 interface properties.

Parameter	Value
L_G	0.25-5μm
W	0.25-0.35μm
T_{ox}	3nm
T_{box}	200nm
T_{Si}	70nm
T_{Ge}	21nm
T_{sp}	8nm

Table 3.1 Device parameters for the fabricated Ge-source TFET.

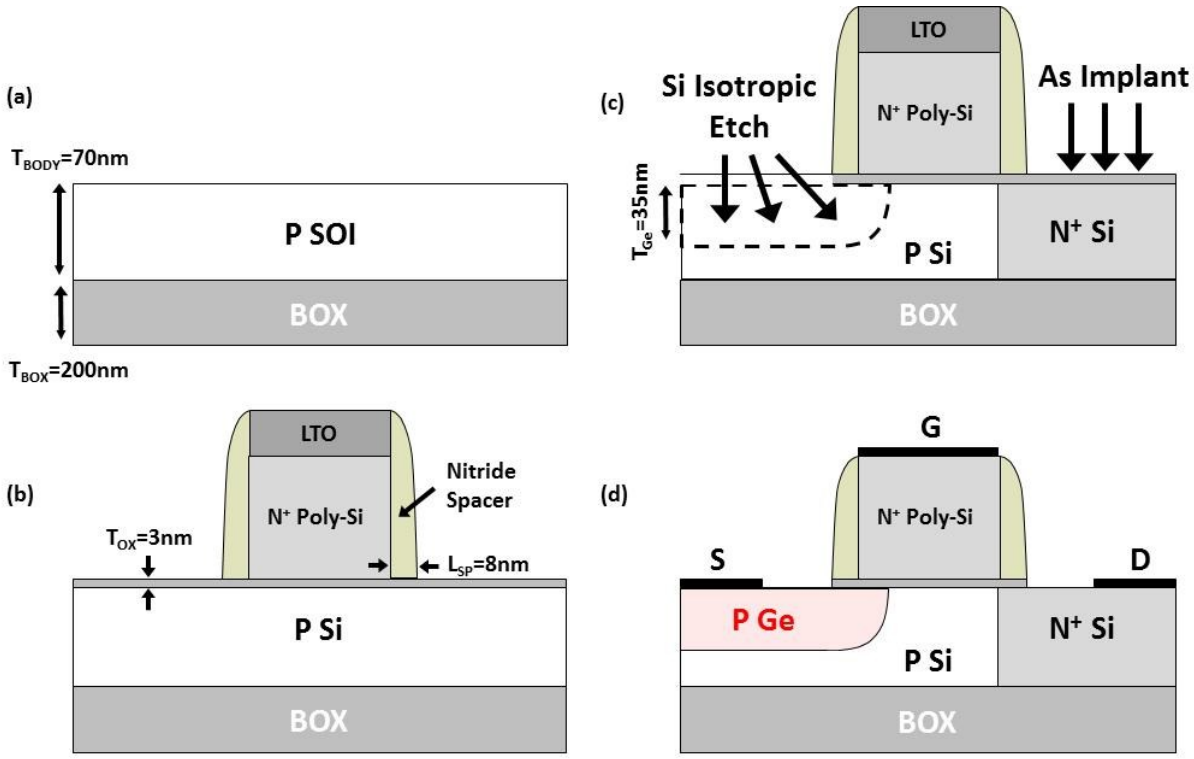

Fig. 3.3 Process flow of the planar Ge-source TFET. After (a) thinning down the SOI wafer, (b) gate stack consisting of thermal oxide, N^+ poly-Si, LTO gate-hardmask, and Si_3N_4 gate-sidewall spacers were deposited and patterned. Then (c) the drain region is implanted with As^+ and the source region etched isotropically to formthe gate-to-source overlap area. (d) Poly-Ge is selectively deposited only on Si.

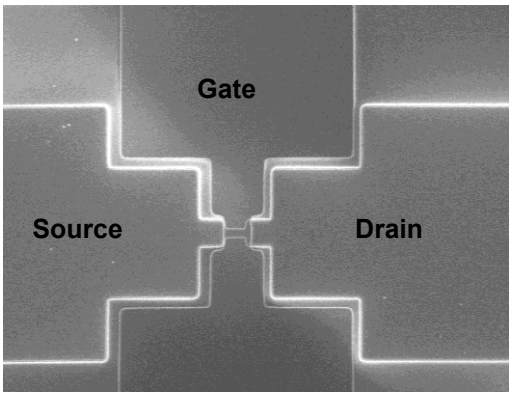

Fig. 3.4 Plan view scanning electron micrograph of the Ge-source TFET before Ge-source deposition.

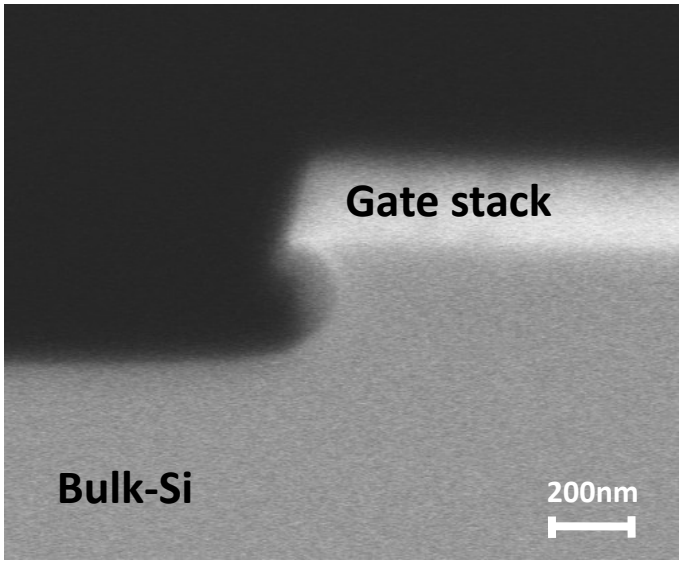

Fig. 3.5 Cross sectional SEM of a dummy wafer showing the recessed profile undercutting the gate.

3.4 Device Measurements

The measured I_{DS} *vs*. V_{GS} characteristics and the corresponding subthreshold swing (S) *vs*. I_{DS} are plotted in Fig. 3.6 for a long-channel (5 μm) TFET [1]. The minimum current ("leakage floor," I_{OFF}) is 0.1 pA/μm and the drive current for a 0.5 V gate-voltage swing is 0.4 μA/μm, for V_{DS} = 0.5 V (Fig. 3.6(a)). The low threshold voltage (V_T < 0 V) is likely due to a relatively large fixed charge density at the oxide/Ge interface [13]. The source recess-etch also partially etched away some of the SiO_2 gate-dielectric above the gate-to-source overlap region, which reduced the effective oxide thickness (EOT) and resulted in lower V_T. The measured data can be well-matched to the theoretical BTBT current model, the details of which will be explained in the next section.

Fig. 3.6(b) shows the sub-60mV/dec switching characteristics of the Ge-source TFET (3 orders of sub-60mV/dec current modulation) [1]. The TFET's representative exponential dependence of S on I_{DS} (V_{GS}) is also observed which confirms the BTBT carrier injection mechanism of the Ge-source TFET. In contrast, a MOSFET S *vs.* I_{DS} exhibits a constant slope in the subthreshold region followed by a rapid degradation in the saturation regime [14].

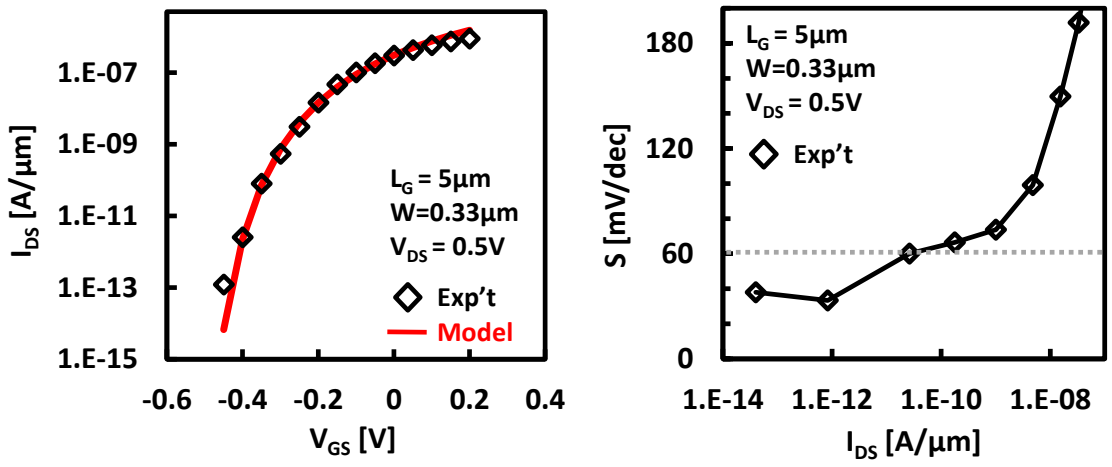

Fig. 3.6 (a) Measured I_{DS}-V_{GS} and (b) S-I_{DS} characteristics for a long-channel (5 µm) TFET. The measured data show good agreement with the BTBT analytical model.

The drive current shows minimal dependence on gate length and I_{ON}/I_{OFF} current ratios greater than 6 orders of magnitude are observed for gate lengths down to 0.4 µm below which the leakage floor increases due to short-channel effects (Fig. 3.7). The nearly L_G-independent I_{ON} is expected since the I_{ON} of a TFET is BTBT limited [15]. The source-side limited tunneling current translates to a different current pinchoff mechanism as compared to a MOSFET, which defines different short channel effects and scalability issues associated with TFETs (to be discussed in next chapter).

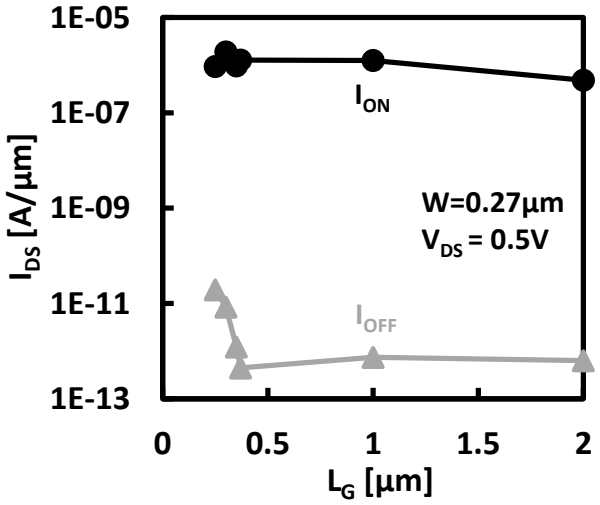

Fig. 3.7 Measured TFET I_{ON} and I_{OFF} vs. L_G. I_{OFF} corresponds to the minimum I_{DS}; I_{ON} corresponds to I_{DS} for 0.5 V gate voltage swing.

The measured I_{DS}-V_{DS} characteristics are shown in Fig. 3.8. Unlike the conventional TFET, in which the output characteristics show non-linear and non-saturating behavior, the Ge-source TFET exhibits almost MOSFET-like output characteristics (good linearity and saturation region with high output resistance) [16]. Note that the origin of the "slow" turn-on characteristics associated with a conventional TFET is due to the proximity of channel pinch off towards the source region. In other words, the drain bias not only collects carriers from the source region via drift, but also couples with the surface potential near the source region to modulate the tunneling barrier, which leads to an exponential behavior in the output current [16].

The experimental results of the Ge-source TFET (Fig. 3.8), however, deviates from the above theory for the following two reasons. First, due to its gate-to-source overlap area with non-degenerately doped source, the gate bias alone can effectively create a large energy band bending within the overlapped source region. Hence, the functionality of V_{DS} is to induce a separation of electron and hole quasi-Fermi levels (with respect to the bulk of P^+ Ge to the surface) to an existing large energy band bending, rather than to modulate the tunnel barrier thickness [15]. This results in a tunneling pinchoff ("$V_{D,SAT}$") at lower V_{DS} and higher output resistance, as compared to a conventional lateral tunneling device. Note that for a point tunneling device (BTBT across the source to the channel), the doping gradient inherently present across the source to channel junction degrades the gate modulation of the energy band bending [17-18] which then allows for a direct modulation by V_{DS}, resulting in degraded linearity and output resistance.

Secondly, the drain bias is further decoupled from the BTBT in the Ge-source region due to the highly resistive, amorphous interfacial layer present in the Ge to Si interface. Fig. 3.9 shows a cross sectional transmission electron microscope (TEM) image of poly-crystalline Ge deposited on Si following identical process conditions as the device fabrication (poly-Ge deposition condition: LPCVD, GeH_4 15 sccm, 1%BCl_3 /99%He 35 sccm) [1]. It can be seen that there exists an amorphous interfacial layer between poly-Ge and Si, which can be electrostatically considered as a larger resistor in series with the channel. Hence, the coupling of V_{DS} to the source region and its impact in modulating the tunnel barrier thickness becomes significantly weaker, resulting in a more MOSFET-like output characteristics.

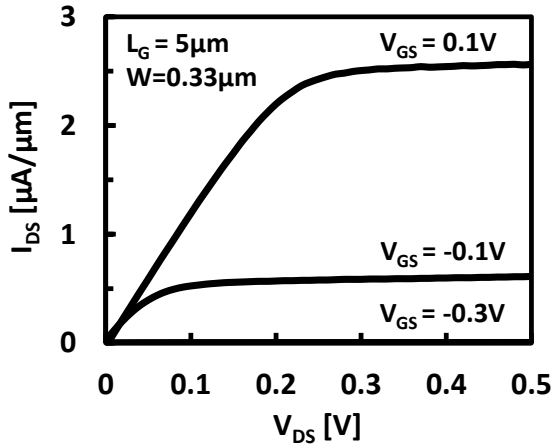

Fig. 3.8 Measured I_{DS}-V_{DS} characteristics for a long-channel (5 µm) TFET showing good linearity and high output resistance.

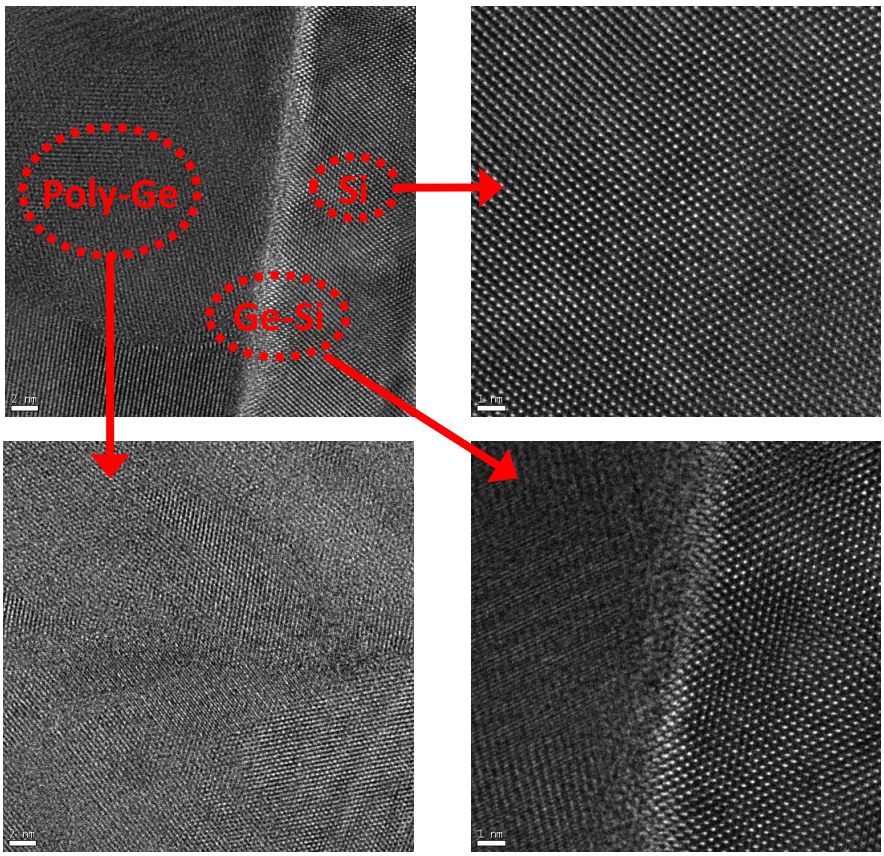

Fig. 3.9 Cross-sectional transmission electron microscopy (TEM) image of the poly-crystalline Ge to Si junction [1]. Identical process conditions as in the device fabrication were used to fabricate this poly-Ge and Si heterojunction.

Table 3.2 shows the performance comparison of Ge-source TFET *vs.* other TFET designs based on Si, Ge, and SiGe. It can be seen that by employing Ge only in the source of an n-channel TFET, a record high I_{ON}/I_{OFF} ratio ($>10^6$) is achieved for low-voltage (0.5 V) operation. It has also been demonstrated that the Ge-source TFET can be fabricated using established planar processing techniques, in a CMOS-compatible process flow.

3.5 BTBT Model Calibration and Energy-Delay Performance Assessment

The previous section presented the experimental results of the Ge-source n-channel TFET and highlighted its outstanding DC performance. This section will assess the energy-delay performance of the TFET and benchmark against a MOSFET to accurately assess the potential energy savings offered by the TFET. This will be accomplished by beginning with the BTBT model calibration to the experimental results, and then utilizing the analytical framework to perform energy-delay assessment.

3.5.1 BTBT Model Calibration

From the measured transfer characteristics of the Ge-source TFET, it was shown that the experimental results can be well-matched to a calibrated BTBT model (Fig. 3.6(a)). The following will present the analytical framework for the calibration process.

From Eqs. (1) and (2), the BTBT theory predicts [6-8]:

	Ref. [3]	**Ref. [19]**	**Ref. [20]**	**This Work**
Structure	**Si TFET**	**SiGe TFET**	**s-Ge TFET**	**Ge TFET**
T_{ox}(nm)	2(SiO_2)	3(HfO_2)	20(LTO)	3(SiO_2)
L_G(nm)	70	100	1000	5000
@ V_D (V)	1	1.2	0.5	0.5
I_{ON}(μA/μm)	12.1	0.009	0.001	0.42
I_{OFF}(pA/μm)	5400	8	0.3	0.12
I_{ON}/I_{OFF} for V_{DD}=0.5V	6E3	3E3	4E4	3E6

Table 3.2 Performance comparison among TFET designs based on Si, Ge, and SiGe. Ge-source TFET achieves the highest I_{ON}/I_{OFF} ratio for small supply voltage operation (0.5 V).

$$I_D = AE_S \exp(-\frac{B}{E_S}) \text{ where } A = \frac{\sqrt{2}q^3 m^{*\frac{1}{2}} V_a}{4\pi^3 \hbar} \text{ and } B = \frac{\pi m^{*\frac{1}{2}} E_G^{\frac{3}{2}}}{2\sqrt{2}q\hbar} \qquad (7)$$

where *E*s is the vertical electric field at the semiconductor (Ge) surface in the gate-to-source overlap region of the tunneling, and can be expressed as:

$$E_S = \frac{\varepsilon_{OX} | V_{GS} + V_{FB} + V_{TUNNEL} |}{\varepsilon_{Ge} T_{OX}} \simeq \frac{| V_{GS} + V_{FB} + V_{TUNNEL} |}{4T_{OX}} \qquad (8)$$

where qV_{TUNNEL} is the minimum energy-band bending needed for band-to-band tunneling to occur, 4 is the ratio of Ge to SiO_2 permittivity, and *Tox* is the gate-oxide thickness over the gate-to-source overlap region [1].

Substituting Eq. (8) into (7) and rearranging, BTBT current can be expressed as:

$$\therefore I_D = A \frac{| V_{GS} + V_{FB} + V_{TUNNEL} |}{4T_{OX}} \exp\left(- \frac{B}{\frac{| V_{GS} + V_{FB} + V_{TUNNEL} |}{4T_{OX}}} \right) = A' | V_{GS} + V_{FB} + V_{TUNNEL} | \exp\left(- \frac{B'}{| V_{GS} + V_{FB} + V_{TUNNEL} |} \right) \qquad (9)$$

where $A' = \frac{A}{4T_{OX}}$ and $B' = 4T_{OX} B$ (10).

Linearizing the above expression to $y = -B'x + \ln A'$ format:

$$\ln(\frac{I_D}{| V_{GS} + V_{FB} + V_{TUNNEL} |}) = -B'(\frac{1}{| V_{GS} + V_{FB} + V_{TUNNEL} |}) + \ln A'$$

The best linear fit for *ln* $I_D/|V_{GS}+V_{TUNNEL}|$ *vs.* $1/|V_{GS}+V_{TUNNEL}|$ was found for a V_{TUNNEL} value of 0.595 V ($V_{TUNNEL} = \frac{E_{G,Poly-Ge}}{q} = 0.595V$, Fig. 3.10), indicating that the effective tunnel bandgap ($E_{G,Poly-Ge}$) is somewhat smaller than the bandgap of monocrystalline Ge (0.66 eV) [21]. This is reasonable, considering poly-Ge has a high density of defects with associated trap state energy level located ~0.1eV away from the valence-band edge [22], which would effectively lower the tunnel bandgap. Using $E_{G,Poly-Ge}$ = 0.56 eV and *m** = 0.06 m0 [21], *B* factor can be calculated using eqn. (1). Then using *B* and eqn. (10), T_{OX} is determined to be 1.9nm from the experimentally measured value of *B* (2.59 MV/cm, ref. Fig.3.10). Note that a thinner oxide thickness expected, since source recess etch process partially etched away SiO_2 from the gate-to-source overlap region.

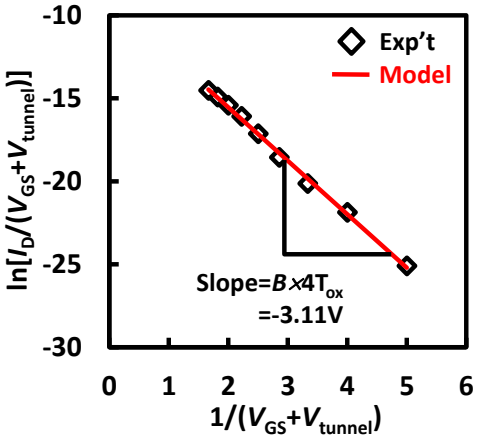

Fig. 3.10 Linear fit of $ln|I_D/(V_{GS}+V_{TUNNEL})|$ *vs.* $1/(V_{GS}+V_{TUNNEL})$ with V_{TUNNEL}=0.595V, for the TFET of Fig. 3.6.(a). The tunneling model exponential factor B is extracted to be 2.59 MV/cm.

3.5.2 Energy-Performance Assessment

Utilizing the calibrated BTBT model, the energy-performance of the TFET can be assessed using the methodology below.

The total energy dissipated can be expressed as follows [23]:

$$E_{TOTAL} = E_{DYN} + E_{LEAK} \qquad (11)$$

where $E_{DYN} = \alpha L_d F C V_{DD}^2$ (12), $E_{LEAK} = L_d F I_{off} V_{DD} t_{delay}$ (13), and $t_{delay} = \frac{L_d F C V_{DD}}{2 I_{on}}$.

α is the activity factor, L_d logic depth, F fanout, and C capacitance per stage of the logic chain. Each performance specification (f in Hz) defines the total delay of the logic network defined by $f = \frac{1}{t_{delay}}$. From t_{delay}, delay-per-stage ($t_{delay/stage}$) can be calculated from $t_{delay/stage} = \frac{t_{delay}}{L_d}$. Then, each $t_{delay/stage}$ specification defines corresponding V_{DD} and I_{ON}.

For each (V_{DD}, I_{ON}) pair that satisfies $t_{delay/stage}$, $V_{G,ON}$ can be determined from the experimental/simulation data, and $V_{G,OFF}$ is correspondingly defined as $V_{G,ON}$ - V_{DD}; current that corresponds to $V_{G,OFF}$ is defined to be I_{OFF}. Fig. 3.11 shows the schematic description of this extraction process.

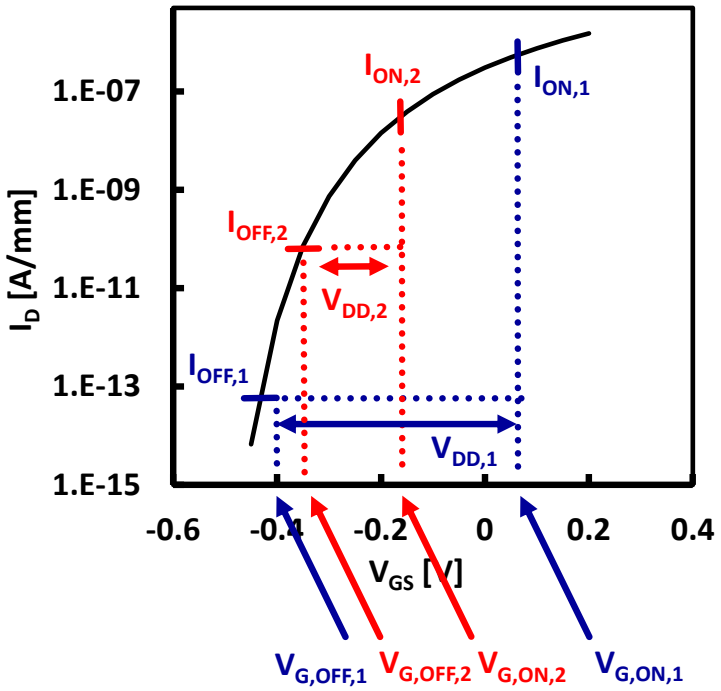

Fig. 3.11 Pictorial demonstration of the extraction method used to determine $V_{G,ON}$, $V_{G,OFF}$, and I_{OFF} from I_{ON} that satisfies a certain delay constraint, $t_{delay/stage}$.

For each extracted (V_{DD}, I_{ON}-I_{OFF}) pair, E_{DYN} and E_{LEAK} *vs.* V_{DD} (from (12) and (13), respectively) can be calculated and the plot of energy/cycle *vs.* V_{DD} can be generated as in Fig. 3.12(a). Note that t_{delay} is used in the E_{LEAK} calculation (rather than $t_{delay/stage}$) since off-transistors leak over the entire duration of a signal propagating from input to the output of the logic network. From the plot (Fig. 3.12(a)), the minimum switching energy is determined by two-times the crossover point between E_{DYN} and E_{LEAK}, with the corresponding $V_{DD,MIN}$ defining the optimal supply voltage. The above analysis can be performed for various frequency specifications. In the end, E_{MIN} *vs.* f or E_{MIN} vs. t_{delay} plots can be generated as in Fig. 3.12(b), with each data points corresponding to $V_{DD,MIN}$.

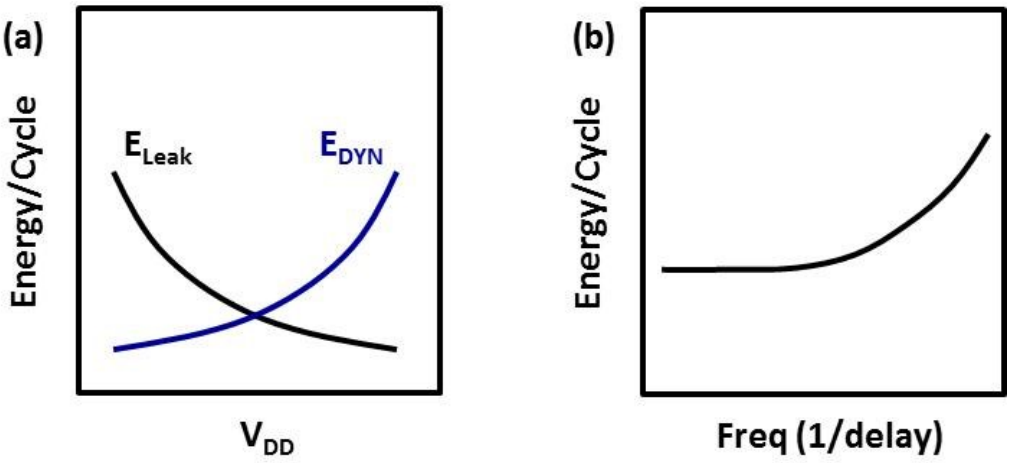

Fig. 3.12 (a) Schematic of the E_{LEAK} and E_{DYN} for various V_{DD} values. The cross over point multiplied by 2 ($E_{LEAK} + E_{DYN}$) corresponds to the minimum switching energy (E_{MIN}) for a given delay (frequency) constraint. (b) Plotting E_{MIN} for various frequencies generates energy-performance plot.

The energy-delay performance of the Ge-source TFET has been benchmarked against that of CMOS technology using the methodology described above. Using the calibrated analytical model for I_D, with T_{OX} scaled down to 1nm, a comparison is made for the 65nm technology node MOSFET (Fig. 3.13) [24]. The results indicate that this TFET technology offers substantial improvements in energy efficiency, so that it is attractive for low-power applications up to ~0.5GHz.

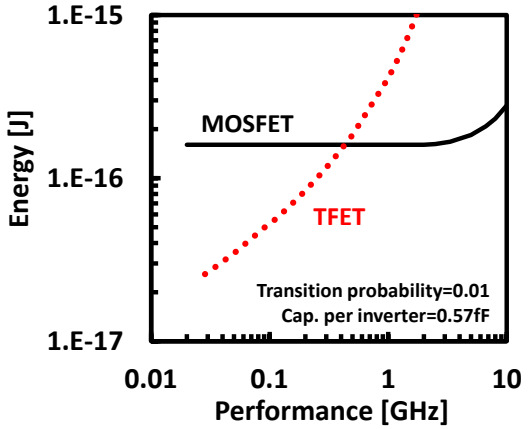

Fig. 3.13 Simulated Energy-Performance comparison of the Ge-source TFET *vs.* MOSFET, for a 30-stage FO4 inverter chain. Device parameters are taken from the ITRS, for the 65nm LSTP technology node.

3.6 Device Design Optimization via Simulation

Based on the experimental results and energy-performance assessment, the feasibility and the potential energy savings of the Ge-source TFET was presented. In order to gain better understanding of the device and perform further design optimization study, TCAD (Sentaurus Device) was used to investigate the impact of various physical parameters of the device. This section will highlight the optimization methodology and propose a nominal planar Ge-source n-channel TFET.

The cross-sectional schematic of the L_G = 30 nm Ge-source n-channel TFET structure used to perform the design optimization study is shown in Fig. 3.14 [2]. The embedded-Ge source region is heavily doped (10^{19} cm^{-3}) p-type, the Si body region is doped p-type, and the Si drain region is heavily doped (10^{19} cm^{-3}) n-type. The underlying buried oxide layer is 200 nm thick. The physical gate length (L_G) is 30 nm and the gate dielectric equivalent SiO_2 thickness (EOT) is 1 nm, relevant for state-of-the-art CMOS technology. N^+ poly-Si gate (4.0 eV work function), 8 nm-wide silicon-nitride gate-sidewall spacers, and 5 nm gate-to-source overlap (L_{Ge}) are used, following [1]. Fixed charge at the gate-dielectric/Ge interface, ~10^{11} q/cm^2 is assumed [13].

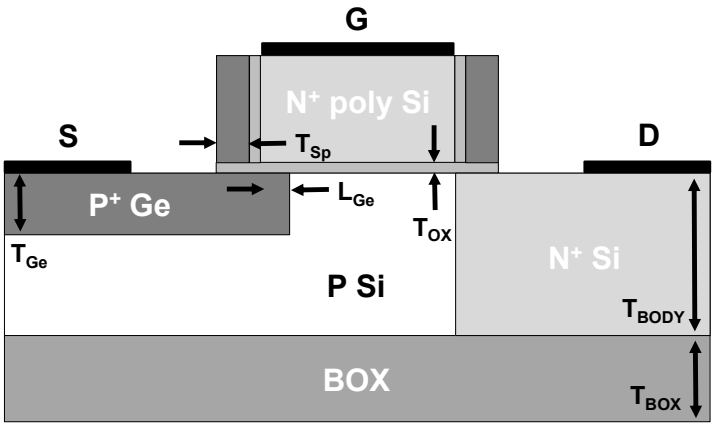

Fig. 3.14 Cross sectional schematic of the planar Ge-source n-channel TFET used to perform design optimization study in Sentaurus Device. L_G is 30 nm and other physical parameters are varied to investigate their impact.

3.6.1. Impact of Source Region Design

It should be noted that the first step in this study was to obtain a realistic *A* and *B* coefficients to be used in the dynamic non-local BTBT model of Sentaurus Device. Utilizing the experimental results (Fig. 3.6(a)), Jacobson *et al.* has performed a rigorous BTBT model calibration and obtained a good fit (Fig. 3.15(a)) [25]. The derived *A* and *B* coefficients ($A = 1.46 \times 10^{17}\ cm^{-3} \cdot s^{-1}$ and $B = 3.59 \times 10^{6}\ V \cdot cm^{-1}$, respectively) were then incorporated into Sentaurus Device for device optimization.

As expected from a line tunneling device, the most crucial design parameters are the source doping and the gate-to-source overlap area, both of which determine the on-state drive current and the steepness of the turn-on characteristics. The analysis was undertaken by Jacobson *et al*. the results of which are summarized in the following [25].

Since the source doping (N_{SOURCE}) defines the depletion region thickness which is directly correlated to the tunneling distance, it is of crucial importance to determine the optimal N_{SOURCE} that results in the steepest swing and highest I_{ON}. For low source doping (*i.e.* $10^{18}\ cm^{-3}$), the width of the depletion region is large, and hence the tunneling distance (tunneling probability) is low (Fig. 3.15(b)). If Ge-source is heavily doped (*i.e.* $10^{20} cm^{-3}$), then Ge is not significantly depleted so tunneling occurs laterally from the Ge-source region into the Si-channel inversion layer, near to the gate-oxide interface. Note that the S is relatively poor for this case since the applied gate voltage depletes the surface of the Ge source as it forms the inversion layer in the Si channel, so that the tunneling distance increases counterproductively (Fig. 3.15(b)). The optimal N_{SOURCE} for maximum I_{ON} and steepest S occurs for $10^{19} cm^{-3}$ since significant energy-band bending (*i.e.* potential drop) can exist within the Ge-source region so that tunneling can occur entirely within the Ge (Fig. 3.1) [2]. Note that the physical thickness of Ge (T_{Ge}) must be larger than the depletion width (~15 nm) in order to confine the electrostatics within the source region and induce vertical tunneling. If tunneling occurs entirely in the vertical direction, then larger overlap area directly translates to larger tunneling area, and hence I_{ON}.

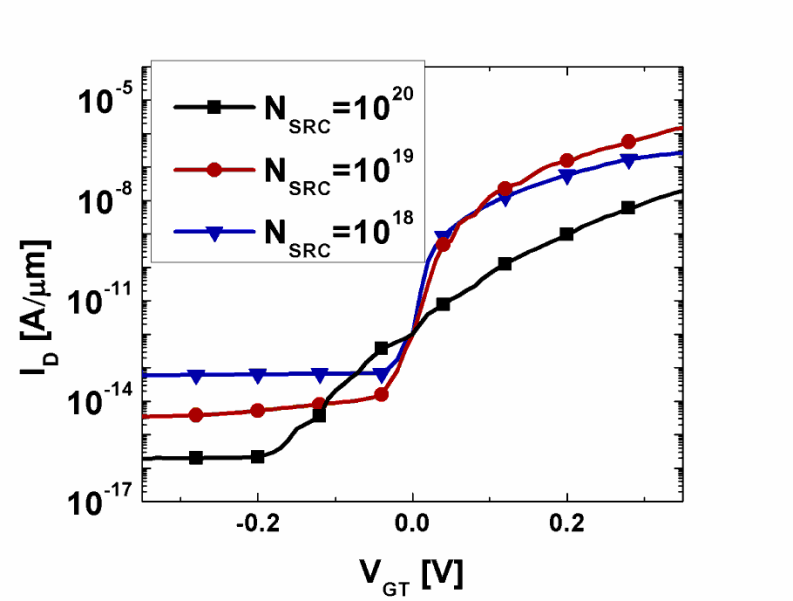

Fig. 3.15 Simulated transfer characteristics of a planar Ge-source TFET [1] for various source doping levels. $N_{SRC} = 1\times10^{19}$ cm^{-3} provides for the largest I_{ON}/I_{OFF}.

3.6.2 Impact of Body Doping and Thickness

In order to maximize the I_{ON}/I_{OFF} ratio for the largest energy savings, it is not only important to maximize I_{ON}, but also crucial to suppress I_{OFF} as much as possible. The following sections will investigate the physical origin of the TFET leakage currents and present design methods to co-optimize I_{ON} and I_{OFF} by changing the body doping and thickness.

3.6.2.1. Off-State Leakage Current

Figs. 3.16(a) and (b) show the simulated transfer characteristics for various body thicknesses (T_{BODY}), for light body doping (N_{BODY} = 10^{15} cm^{-3}) and moderate body doping (10^{18} cm^{-3}), respectively [2]. Generally, the leakage floor (I_{OFF}) is reduced with moderate body doping. The I_{OFF} dependence on T_{BODY} changes with N_{BODY}, which suggests that the dominant leakage mechanism also changes with body doping.

In the off state (with $V_{GS} = 0$ V and $V_{DS} = 0.5$ V), an inversion layer of electrons can exist at the surface of the Si body region if the MOS threshold voltage is less than 0 V. In that case, at the surface, V_{DS} is dropped almost entirely across the n-channel/P$^+$-source junction and leakage current flows primarily due to minority-carrier collection from the Ge. Away from the surface (towards the bottom of the body region), V_{DS} is dropped largely within the body region so that minority-carrier collection from the Si body also contributes to the leakage current. Depending on the values of T_{BODY} and N_{BODY}, either of these leakage components can be dominant.

Fig. 3.17 shows simulated off-state current contour plots for various combinations of T_{BODY} and N_{BODY}. Since lower body doping corresponds to larger vertical and lateral depletion widths and larger minority carrier concentration, the TFET off-state leakage is dominated by the reverse diode current of the body-drain junction for $N_{BODY} = 10^{15}$ cm^{-3} (Fig. 3.17(a)). As T_{BODY} is scaled down (Fig. 3.17(b)), the body-drain junction area is reduced and the leakage floor correspondingly decreases (Fig. 3.16(a)).

For $N_{BODY} = 10^{18}$ cm^{-3} and $T_{BODY} = 100$ nm, the body is only partially depleted and its minority carrier concentration is lower, so that the reverse diode current of the body-drain junction is negligible (Fig. 3.17(c)). The TFET off-state leakage is dominated by the surface component. If T_{BODY} is reduced such that it becomes fully depleted, however, the situation becomes similar to that for the lightly doped body: body-drain reverse diode current becomes significant (Fig. 3.17(d)) and the leakage floor correspondingly increases (Fig. 3.16(b)).

These results indicate that if moderate body doping (10^{18} cm^{-3}) is used, then it is not necessary to scale down the body thickness for optimal performance; rather, it is preferable to avoid a fully depleted body region because it results in larger sub-surface reverse-diode leakage current.

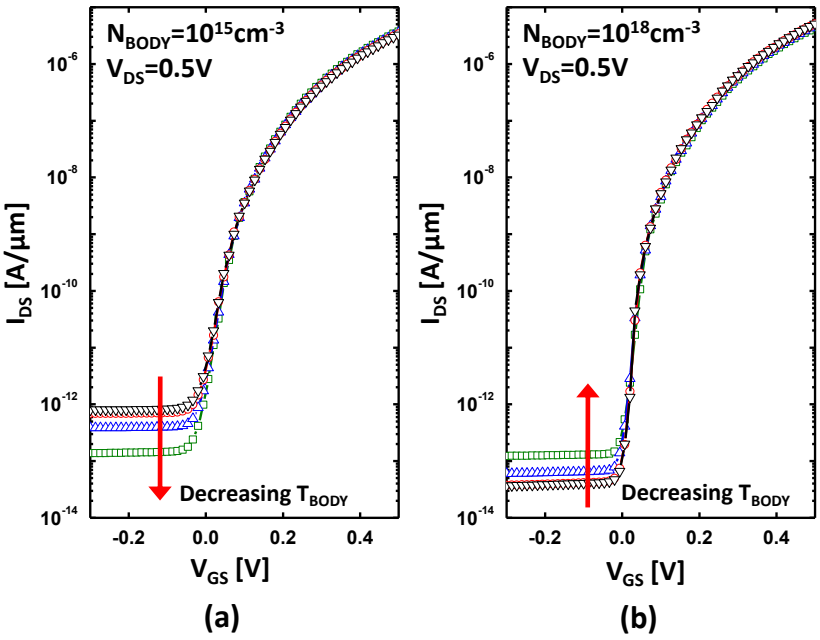

Fig. 3.16 Comparison of simulated transfer characteristics for various body thickness values (T_{BODY} = 20, 30, 50, and 100 nm). (a) N_{BODY} =10^{15} cm^{-3}. (b) N_{BODY} = 10^{18} cm^{-3}.

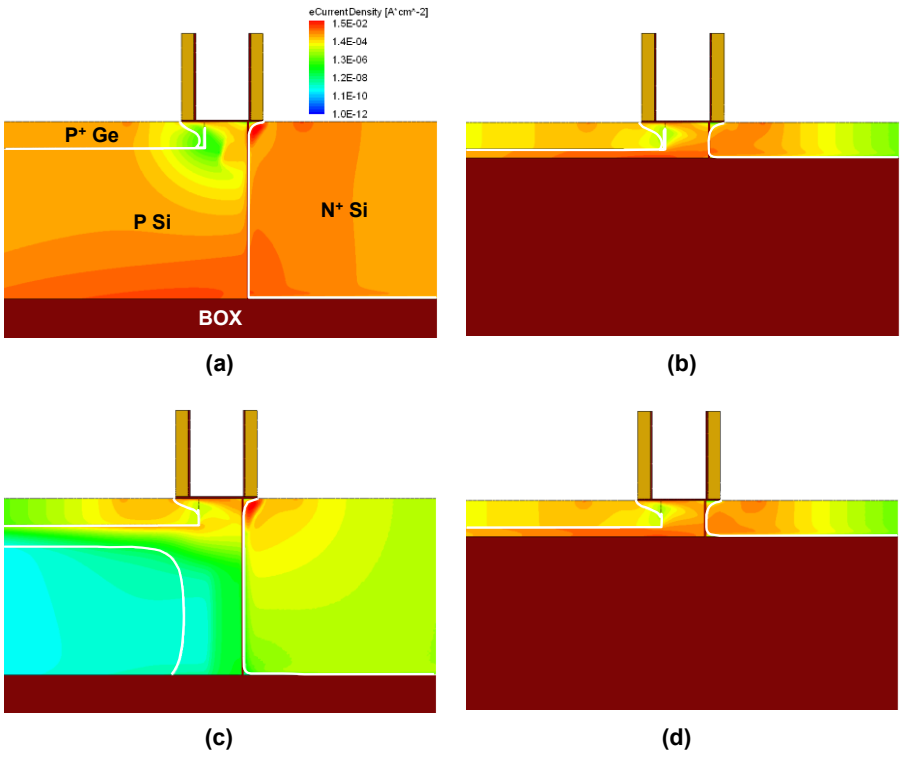

Fig. 3.17 Contour plot of electron current density in the OFF-state for (a) $N_{BODY} = 10^{15}$ cm^{-3} and $T_{BODY} = 100$ nm, (b) $N_{BODY} = 10^{15}$ cm^{-3} and $T_{BODY} = 20$ nm, (c) $N_{BODY} = 10^{18}$ cm^{-3} and $T_{BODY} = 100$ nm, and (d) $N_{BODY} = 10^{18}$ cm^{-3} and $T_{BODY} = 20$ nm. The edges of the depletion regions are denoted by white lines. The dominant leakage path depends on the body doping concentration and body thickness.

3.6.2.2 On-State Drive Current

Figs. 3.18(a) and (b) show the simulated output characteristics for various body thicknesses, for light body doping (10^{15} cm^{-3}) and moderate body doping (10^{18} cm^{-3}), respectively [2]. Generally I_{ON} is higher for moderate body doping. Note, however, that the dependence of I_{ON} on T_{BODY} is relatively small in comparison to the dependence of I_{OFF} on T_{BODY} since the source design is the dominant factor in determining I_{ON}.

For light body doping I_{ON} improves as T_{BODY} is reduced, whereas for moderate body doping I_{ON} degrades as T_{BODY} is reduced. The fundamental reason for these differences is that the Ge along the source-body junction is depleted when the body is lightly doped, due to the very large difference in hole concentrations between the source and the body which drives the diffusion of holes from the Ge into the Si. Thus, the Ge source is partially depleted at its bottom interface with the P-Si body, for $N_{BODY} = 10^{15}$ cm^{-3}. As a result, the vertical band bending within the Ge is reduced, forcing tunneling within the Ge to occur more laterally (with a slightly longer tunneling

distance); hence I_{ON} is lower. The depletion of the Ge source is reduced and hence tunneling current is increased as T_{BODY} is scaled down.

Although not shown here, for $N_{BODY} = 10^{18}$ cm^{-3} and $T_{BODY} = 100$ nm, the Ge along the bottom of the source-body junction is accumulated when the body is moderately doped, due to the large valence-band discontinuity between Ge and Si which makes it energetically favorable for holes to move from the Si into the Ge, despite the concentration gradient. This counteracts the lateral depletion of the Ge (due to the lateral pn junction) at the bottom of the source-body junction, so that tunneling occurs more vertically (with a slightly shorter tunneling distance); hence I_{ON} is higher. As T_{BODY} is reduced such that the thickness of the P-Si underneath the Ge source becomes much less than the P^+-Ge/P-Si depletion width (~15nm), the Ge along the bottom of the source-body junction becomes less accumulated so that tunneling occurs less vertically, *i.e.* the tunneling current decreases.

These results indicate that heavier body doping is desirable for higher I_{ON}. The upper limit for N_{BODY} is set by the requirement that the surface of the body must be inverted when tunneling occurs within the Ge source, *i.e.* the MOS threshold voltage must be lower than the BTBT threshold voltage. (Otherwise, current would be limited by the formation of the inversion layer, and S would be no steeper than 60 mV/dec.) For the device design parameters used in this work, the MOS threshold voltage varies from -0.26 V to -0.079 V for N_{BODY} ranging from 10^{15} cm^{-3} to 10^{18} cm^{-3}. Considering that V_T should be close to 0 V (to allow for the most aggressive V_{DD} scaling) in the ideal case of a very steeply switching transistor, the MOS threshold voltage should not exceed 0 V. Thus, $N_{BODY} = 10^{19}$ cm^{-3} is close to the upper limit.

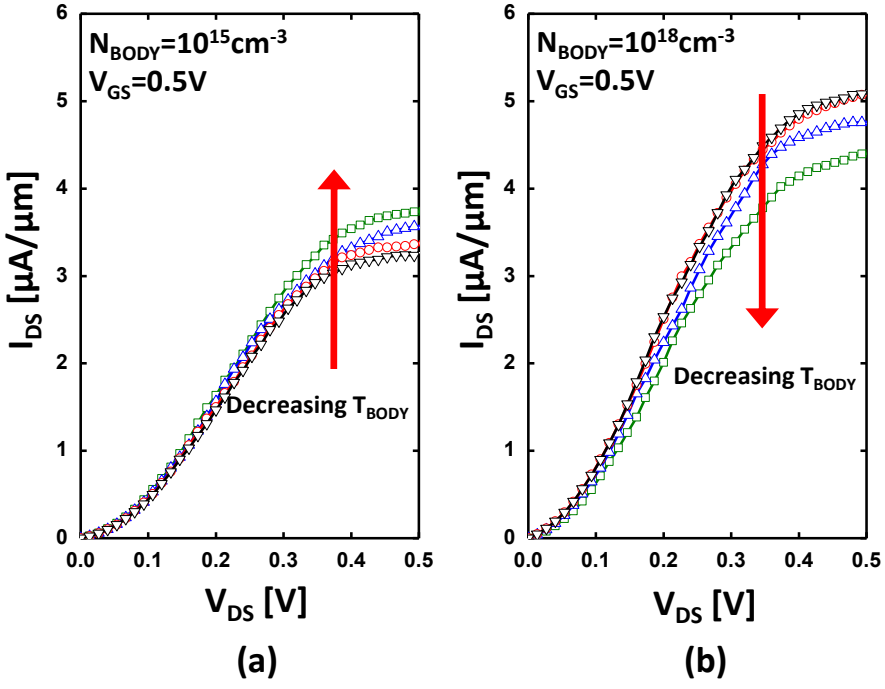

Fig. 3.18 Simulated output characteristics for N_{BODY} of (a) 10^{15} cm^{-3} and (b) 10^{18} cm^{-3} for T_{BODY} of 20, 30, 50, and 100 nm.

3.6.2.3. Output Characteristics

It should be noted that the linearity of the output characteristics is improved with higher body doping (Fig. 3.18). This is expected, since tunneling occurs more vertically with higher body doping, so that the lateral electric field (*i.e.* the drain voltage) has less impact. The current saturates when it becomes limited by tunneling (*vs.* drift). For the optimal body design, the small-signal output resistance in saturation (at V_{DS} = 0.5V) is 1.18 MΩ, which is notably better than the typical value (<50 kΩ) for a MOSFET of comparable dimensions [24]. The corresponding intrinsic gain ($g_m r_o$) of an optimized TFET is 50 for V_{DD}=0.5 V.

3.7 Summary

This chapter proposed and demonstrated a planar Germanium-source n-channel TFET which overcame the fundamental limits in poor swing and low drive current associated with the conventional source-to-channel lateral tunneling device design. It has been shown that employing Ge only in the source region and introducing gate-to-source overlap area are effective methods to improve I_{ON}/I_{OFF} ratio for low supply voltage operation.

Ge-source n-channel TFETs were experimentally demonstrated using a conventional CMOS process flow. The measured characteristics exhibited greater than 6 orders of I_{ON}/I_{OFF} ratio for V_{DD} of 0.5 V operation, a record which still holds to date for any Si/Ge/SiGe-based TFETs. Based on the experimental results, methods to calibrate the BTBT model and utilizing it to assess the energy-performance were demonstrated. It was projected that the Ge-source TFET, as compared to 65 nm CMOS technology, is expected to provide for lower energy per operation for throughput up to 500 MHz.

The experimental results were also used to calibrate the simulation package (Sentaurus evice) which was then used for a design optimization study. It was found that an optimal source doping exists which yields the steepest slope and largest drive current. In-depth analysis was performed to reduce I_{OFF} in order to improve the overall I_{ON}/I_{OFF} ratio. A careful design of the body doping and thickness was found to co-optimize I_{ON} and I_{OFF}.

3.8 References

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3.9 Appendix: Process Flow for Planar Ge-Source TFET

Step	Process Name	Process Specification	Equipment
0.01	Wafers	6 six inch prime SOI wafers and 22 test wafers	Soitec
0.02	Labeling	Label the wafers	
0.03	Si (SOI) Thickness Measurement	Recipe: 4. Polysilicon on Oxide, record in A	nanoduv

0.04	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
0.05	LTO Deposition	Recipe: 11SULTOA - 20min (dep. rate ~125A/min)	tystar11
0.06	SiN Deposition	Recipe: 9SNITA - 800C, 300mT, NH3 75sccm, DCS 25sccm, 30min (dep. rate ~40A/min)	tystar9
0.07	LTO Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
	SiN Thickness Measurement	Recipe: 2. Nitride on Silicon, record in A	nanoduv
***1.00**	**SOI Thinning**		
*1.01	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
*1.02	Oxidation (Dry)	Recipe: 2DRYOXA - 900C, dry O2 4000sccm, 300min Post N2 anneal 950C 20min, ramp to 950C 5min	tystar2
*1.03	Oxide Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
*1.04	Oxide Etch - Wet	piranha, 120C, 10min / 10:1 HF 4min	msink6
*1.05	SOI Thickness Measurement	Recipe: 4. Polysilicon on Oxide, record in A	nanoduv
2.00	**Alignment Mark(PM)**		
2.01	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
2.02	Alignment Mark (PM) Lithography *(lithography 1)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle: BA-COMBI-4X, Reticle ID: **45440204D176**, Layer ID: PM Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300

		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C, 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
2.03	Inspection	Microscope - PM mark inspection	uvscope
2.04	Hard Bake	UV bake: Program U, 140C, 1min	uvbake
2.05	Alignment Mark(PM) Etch	Recipe: shpkim_5003_OB_ME OB: 13mT, TCP RF 200W, bias RF 40W, CF4 100sccm, 5sec ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm, 32sec ME c-Si E.R. ~50A/sec	lam8
2.06	PR Ashing	Recipe: std - 3.75T, 400W, 250C, MFC1 40% O2, 2min 30sec	matrix
2.07	Post Cleaning	piranha, 120C, 10min	msink8
3.00	**Active S/D Area Etch**		
3.01	Preclean	piranha, 120C, 10min	msink8
3.02	Active S/D Area Lithography *(lithography 2)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEVGRPCLR**, Layer ID: Actv (Image ID #3) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
3.03	Inspection	Microscope - active S/D area lithography inspection	uvscope
3.04	Hard Bake	UV bake: Program U, 140C 1min	uvbake
3.05	Active S/D Etch (SOI Etch)	Recipe: shpkim_8003 OB: 13mT, TCP RF 200W, bias RF 40W, CF4 100sccm, 3sec	lam8

		ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm *Times:* ***L5W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)* OE: 80mT, TCP RF 200W, bias RF 150W, HBR 100sccm, O2 1sccm, He 100 sccm *Time:* ***L5W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	
3.06	BOX Thickness Measurement 1	Recipe: 1. Oxide on Silicon, record in A	nanoduv
3.07	PR Ashing	Recipe: std - 3.75T, 400W, 250C, MFC1 40% O2, 2min 30sec	matrix
3.08	Post Cleaning 1	piranha, 120C, 10min	msink8
	Post Cleaning 2	100:1 HF 20sec	msink7
4.00	**Gate Stack Deposition**		
4.01	Preclean	piranha, 120C, 10min / 25:1 HF 10sec	msink6
4.02	Sacrificial Oxidation (Dry)	Recipe: 1GATEOXA - 850C, dry O2 4000sccm, 1min Post N2 anneal 950C 20min, ramp to 950C 5min	tystar1
4.03	Preclean Sacrificial Oxide Etch	piranha, 120C, 10min / 25:1 HF 20sec	msink6
4.04	Gate Oxidation	Recipe: 1GATEOXA - 850C, dry O2 4000sccm, 1min Post N2 anneal 950C 20min, ramp to 950C 5min	tystar2
4.05	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
4.06	poly-Si Gate Deposition (N+ poly-Si)	Recipe: 10SDPLYA - 615C, 375mT, PH3 4sccm, SiH4 100sccm, 95min (dep. rate ~17A/min)	tystar10
4.07	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
4.08	LTO1 Deposition	Recipe: 11SULTOA - 12min (dep. rate ~125A/min)	tystar11
4.09	Dit Measurement	record Dit in cm-2	sca
4.10	Oxide Thickness Measurement	record in A	sopra

4.11	Poly-Si Thickness Measurement	Recipe: 4. Polysilicon on Silicon, record in A	nanoduv
	LTO1 Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
5.00	**Gate Stack Etch**		
5.01	Preclean	piranha, 120C, 10min	msink8
5.02	Gate Lithography *(lithography 3)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEVGRPCLR**, Layer ID: Poly (Image ID #1) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
5.03	Inspection	Microscope - gate lithography inspection	uvscope
5.04	Hard Bake	UV bake: Program U, 140C 1min	uvbake
5.05	LTO1 Etch	Recipe: MXP_OX_VAR - 200mT, 700W, Ar 150sccm, CF4 15sccm, CHF3 60sccm E.R. ~70A/sec (recipe identical to MXP_OXIDE_ETCH) *Time: **dm-LTO1** (sec), **L6W1** (sec), **2** (sec), **3** (sec), **4** (sec), **5** (sec), **6** (sec)*	centura-MxP
5.06	N+ poly-Si Gate Etch	Recipe: shpkim_8003 OB: 13mT, TCP RF 200W, bias RF 40W, CF4 100sccm, 3sec ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm Time: ***dm-LTOa*** (sec) ***L6W1** (sec), **2** (sec), **3** (sec), **4** (sec), **5** (sec), **6** (sec)*	lam8

		OE: 80mT, TCP RF 200W, bias RF 150W, HBR 100sccm, O2 1sccm, He/Ar 100 sccm *Time:* ***L6W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	
5.07	Si (SOI) Thickness Measurement	Recipe: 4. Polysilicon on Oxide, record in A	nanoduv
	BOX Thickness Measurement 2	Recipe: 1. Oxide on Silicon, record in A	nanoduv
	LTO Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
5.08	PR Ashing	Recipe: std - 3.75T, 400W, 250C, MFC1 40% O2, 2min 30sec	matrix
5.09	Post Cleaning 1	piranha, 120C, 10min	msink8
	Post Cleaning 2	100:1 HF 20sec	msink7
6.00	**Spacer Deposition/Etch**		
6.01	Preclean	piranha, 120C, 10min	msink6
6.02	Regrowth Oxidation (Dry)	Recipe: 2DRYOXA - 850C, dry O2 4000sccm, 1min Post N2 anneal 950C 20min, ramp to 950C 5min	tystar2
6.03	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
6.04	SiN Spacer Deposition	Recipe: 9SNITA - 800C, 300mT, NH3 75sccm, DCS 25sccm, 2min (dep. rate ~40A/min)	tystar9
6.05	SiN Thickness Measurement	record in A	sopra
6.06	SiN Spacer Etch	Recipe: MXP_NIT_VAR - 50mT, 450W, Ar 50sccm, CH3F 50sccm, O2 7sccm E.R. ~70A/sec (recipe identical to MXP_NIT_ETCH) *Time:* ***L6W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	centura-MxP
6.07	Post Cleaning	piranha, 120C, 10min	msink8
7.00	**Drain Implantation**		
7.01	Preclean	piranha, 120C, 10min	msink6
7.02	Implant-Barrier Oxidation (Dry)	Recipe: 2DRYOXA - 850C, dry O2 4000sccm, 1min	tystar2

		Post N2 anneal 950C 20min, ramp to 950C 5min	
7.03	Drain Implant Lithography *(lithography 4)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEV_GRP_TFET**, Layer ID: Actv (Image ID #3) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
7.04	Inspection	Microscope - drain implant lithography inspection	uvscope
7.05	Hard Bake	UV bake: Program U, 140C 1min	uvbake
7.06	N+ Drain Implant	As, 7E13cm-2, 15keV, 7 tilt	Core Systems
7.07	PR Ashing	Recipe: std - 3.75T, 400W, 250C, MFC1 40% O2, 2min 30sec	matrix
7.08	Post Cleaning	Piranha, 120C, 10min	msink8
7.09	Preclean	piranha, 120C, 10min / 25:1 HF 10sec	msink6
7.10	RTA, Drain Activation Anneal	Recipe: SHPKIM10 Delay: 10sec, 0C, 1 (steady intensity factor) Ramp: 20sec, 450C, 1 Steady: 30sec, 450C, 0.8 Ramp: 10sec, 950C, 1 Steady: **5sec, 950C**, 1	heatpulse4
7.11	Post Cleaning	piranha, 120C, 10min	msink8
8.00	**Source Recess Etch**		
8.01	Source Implant Lithography *(lithography 5)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6

		Exposure - Reticle ID: **DEV_GRP_TFET**, Layer ID: Metal (Image ID #4) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
8.02	Inspection	Microscope - source implant lithography inspection	uvscope
8.03	Hard Bake	UV bake: Program U, 140C 1min	uvbake
8.04	Source Recess Etch 1 (anisotropic)	Recipe: shpkim_8003_OB_ME OB: 13mT, TCP RF 200W, bias RF 40W, CF4 100sccm, 5sec ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm *Time:* ***dm-LTO2*** *(sec)* ***L6W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	lam8
8.05	Source Recess Etch 2 (isotropic)	Recipe: shpkim_8003_recess ME: 100mT, TCP RF 50W, bias RF 25W, SF6 80sccm, O2 5sccm, HBR 20sccm *Time:* ***dm-LTO2*** *(sec)* ***L6W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	lam8
8.06	PR Ashing	Recipe: std - 3.75T, 400W, 250C, MFC1 40% O2, 2min 30sec	matrix
8.07	Post Cleaning 1	Piranha, 120C, 10min	msink8
	Post Cleaning 2	100:1 HF 15sec	msink7
8.08	LTO Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
8.09	X-SEM	X-SEM - source-recess profile inspection	leo

9.00	**Ge + LTO2 Deposition**		
9.01	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
	Preclean	Acetone, 2min / DI rinse / 100:1 HF, 20sec / DI rinse	msink7
9.02	Ge Deposition (P+ poly-Ge)	Recipe: SGDEPF.019 - 400mT, 425C, GeH4 15sccm, BCl3 **25sccm**, 7min (dep. rate ~60A/min)	tystar19
9.03	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
9.04	LTO2 Deposition	Recipe: 11SULTOA - 8min (dep. rate ~125A/min)	tystar11
9.05	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
	Preclean	Acetone, 2min / DI rinse / 100:1 HF, 20sec / DI rinse	msink7
9.06	Ge Deposition (P+ poly-Ge)	Recipe: SGDEPF.019 - 400mT, 425C, GeH4 15sccm, BCl3 **35sccm**, 7min (dep. rate ~60A/min)	tystar19
9.07	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
9.08	LTO2 Deposition	Recipe: 11SULTOA - 8min (dep. rate ~125A/min)	tystar11
9.09	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
	Preclean	Acetone, 2min / DI rinse / 100:1 HF, 20sec / DI rinse	msink7
9.10	Ge Deposition (P+ poly-Ge)	Recipe: SGDEPF.019 - 400mT, 425C, GeH4 15sccm, BCl3 **45sccm**, 7min (dep. rate ~60A/min)	tystar19
9.11	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
9.12	LTO2 Deposition	Recipe: 11SULTOA - 8min (dep. rate ~125A/min)	tystar11

9.13	LTO2 Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
10.00	**Contact Via Etch**		
10.01	Preclean	piranha, 120C, 10min	msink8
10.02	Contact Lithography *(lithography 6)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEVGRPDRK**, Layer ID: Poly (Image ID #1) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
10.03	Inspection	Microscope - contact lithography inspection	uvscope
10.04	Hard Bake	UV bake: Program U, 140C 1min	uvbake
10.05	LTO2 Etch - Dry	Recipe: MXP_OX_VAR - 200mT, 500W, Ar 120sccm, CHF3 60sccm E.R. ~70A/sec (recipe identical to MXP_OXIDE_ETCH) *Time:* ***L6W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	centura-MxP
10.06	PR Removal	PRS 3000, 80C, 5min	msink16
10.07	LTO1 Etch from Gate - Wet	100:1 HF / DI rinse	msink7

10.08	BOX Thickness Measurement 3	Recipe: 1. Oxide on Silicon, record in A	nanoduv

***** PRELIMINARY TFET MEASUREMENTS (without metalization) *****

11.00	**Metalization**		
11.01	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
	Preclean	Acetone, 2min / DI rinse / 100:1 HF, 20sec / DI rinse	msink7
11.02	AlSi Deposition	Recipe: LWAL - 30sec => ~150nm of Al	novellus
11.03	Metal Lithography *(lithography 7)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEVGRPCLR**, Layer ID: Metal (Image ID #4) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
11.04	Inspection	Microscope - metal lithography inspection	uvscope
11.05	Hard Bake	UV bake: Program U, 140C 1min	uvbake
11.06	AlSi Etch	Recipe: MET_AL_VAR - 10mT, RF 1000W, Bias 100W, BCl3 45sccm, Cl2 90sccm E.R. ~ A/sec (recipe identical to MET_AL_ME) *Time: **L6W1** (sec), **2** (sec), **3** (sec), **4** (sec), **5** (sec), **6** (sec)*	centura-MET

11.07	PR Ashing	Recipe: std - 3.75T, 400W, 250C, MFC1 40% O2, 2min 30sec	matrix
11.08	X-SEM	SEM - Al thickness measurements	leo
11.09	Postclean	Acetone, 2min / DI rinse	msink7

***** ***SECONDARY TFET MEASUREMENTS*** *****

12.00	**Forming Gas Anneal**		
12.01	Preclean	Acetone, 2min / DI rinse	msink7
12.02	Forming Gas Anneal	Recipe: H2SINT4A.018, 400C, forming gas(10% H2, 90% N2, 3000sccm), 30min	tystar18

***** ***Final TFET MEASUREMENTS*** *****

Chapter 4

Raised Ge-Source TFET

4.1 Introduction

The previous chapter presented the planar Ge-source TFET in which the band-to-band tunneling (BTBT) occurred within the gate-to-source overlap region, in the direction vertical/perpendicular to the semiconductor/gate-dielectric interface [1-2]. Device fabrication and measurement results have demonstrated steep subthreshold swing (S), large on-state drive current (I_{ON}), and a potential for superior energy savings for low supply voltage (V_{DD}) operation, as compared with the conventional source-to-channel lateral tunneling device and CMOS technology [3]. The experimental results were used to calibrate the device simulation package (Sentaurus Device) which was employed to perform TFET design optimization [2, 4].

The planar design, however, inherently suffers from a few drawbacks. Due to the lateral potential drop induced by the drain voltage, lateral tunneling occurs first as the gate voltage is increased, resulting in a small "kink" in the transfer characteristics which effectively degrades S [5]. In other words, two BTBT processes (lateral *vs*. vertical) present within the gate-to-source overlap region compete for the given electrostatics, which results in the effective tunneling direction at an angle (as opposed to completely vertical or lateral) with degraded net performance. Furthermore, there exists a fundamental limit for which I_{ON} can be modulated by increasing the gate-to-source overlap area before the off-state leakage current (I_{OFF}) degrades due to direct source-to-drain tunneling induced by the drain field (V_{DS}) [6, 7]. This defines the scaling limit of the planar Ge-source TFET; once the channel length (defined to be from the edge of the gate-to-source overlap region to the drain region) becomes less than 25 nm, then the on-state to off-state current ratio (I_{ON}/I_{OFF}) degrades significantly [6, 7]. In terms of device fabrication, performing the source recess etch while minimizing the etch damage to the gate-dielectric is also a major challenge.

This chapter addresses the above limitations of the planar design and proposes an improved Ge-

source TFET structure. The raised Ge-source TFET will be shown to suppress lateral tunneling and achieve steeper switching behavior and higher I_{ON} for an even lower supply voltage operation ($V_{DD} < 0.5$ V). The performance of this new TFET design will be benchmarked against that of CMOS technology and other Ge-source TFET designs, and shown that it can offer lower energy per operation for throughput in the frequency range up to 1 GHz for sub-0.5 V operation. Device fabrication and measurement results will be presented and discussed.

4.2 Device Simulation

4.2.1. Device Structure

Fig. 4.1(a) shows the planar Ge-source TFET design reported in [1], which is fabricated by recessing the Si in the source region before selectively growing *in-situ*-doped p-type Ge. Fig. 4.1(b) shows the partially elevated Ge-source design, which can be fabricated by recessing the Si in the source region and then overgrowing the *in-situ*-doped Ge (by 10 nm). Fig. 4.1(c) shows the fully elevated Ge source design, which can be fabricated by selectively growing a thin Si vertical offset layer before growing *in-situ*-doped Ge in the source region.

For each of the TFET designs, the Ge source is heavily doped p-type ($N_{Ge} = 10^{19}$ cm^{-3}) and the Si drain is heavily doped n-type (10^{19} cm^{-3}). The Si channel region is moderately doped p-type (10^{18} cm^{-3}) and is 100 nm thick to minimize off-state leakage current [2]. The underlying buried oxide (SiO_2) layer is 200 nm thick. L_G is 30 nm and the gate dielectric equivalent SiO_2 thickness (EOT) is 1 nm. The gate material is assumed to be metallic, with work function = 4.0 eV. For the planar source design, the gate-sidewall spacers (L_{SP}) comprise silicon nitride and are 8 nm wide; for the elevated source designs, they comprise silicon dioxide and are 1 nm wide. For the planar and partially elevated source designs, the gate-to-source overlap (L_{OV}) is 5 nm. For the fully elevated source design, the Si vertical offset layer (T_{OFFSET}) is 5 nm thick and doped p-type (10^{18} cm^{-3}). Fixed charge (~10^{11} q/cm^2) at each dielectric/Ge interface is assumed [8].

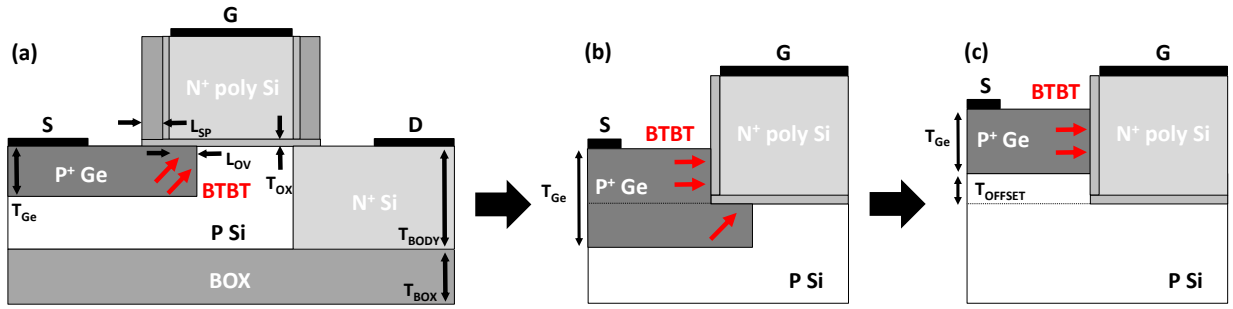


Fig. 4.1 Schematic cross section of the (a) planar, (b) partially elevated, and (c) fully elevated Ge-source TFETs, with (b) and (c) only showing the schematics near the source region. Dominant directions of electron tunneling are indicated by the arrows.

4.2.2. Device Operation Principle and DC Characteristics

The dominant tunneling mode (lateral *vs.* vertical) within a TFET is strongly dependent on its geometry. At high gate voltages, vertical tunneling is dominant as indicated by the arrows in Fig. 4.1 if (1) the source is non-degenerately doped ($N_{Ge} = 10^{19}$ cm^{-3}), (2) the source region thickness is greater than its depletion width ($W_{DEP} \approx 15$nm for $N_{Ge} = 10^{19}$ cm^{-3}) and (3) there is significant gate-to-source overlap [2]. With a thin gate-sidewall dielectric, vertical (perpendicular to the semiconductor/gate-dielectric interface) tunneling can be induced within the elevated Ge in the partially elevated source structure and fully elevated source structure, resulting in an increased tunneling area and hence increased I_{ON} (Fig. 4.2).

At low gate voltages, lateral tunneling can occur from the lower corner of the Ge source to the Si channel if the drain voltage induces a significant potential drop across the channel-source junction [5]. This is the case for the planar source structure and partially elevated source structure: the device first turns on with lateral tunneling and then transitions to predominantly vertical tunneling, so that the average S is degraded. For the fully elevated source structure, lateral tunneling is suppressed because the potential drop across the source-channel junction is relatively small. This is because the source region is non-degenerately doped and gated so that the depletion of the source region reduces the potential barrier height seen by the channel (Fig. 4.3(c)). As a result, the drain voltage is dropped laterally within the Ge source (in x-direction, Fig. 4.3(a)), rather than across the source-channel junction, thus electrostatically coupling with V_{GS} to maximize BTBT within the source. A vertical offset ($T_{OFFSET} > 0$ nm) is necessary to achieve this effect since placing the source to channel junction closer to the corner (where the gate field is weaker) would increase the lateral potential drop and degrade the turn on characteristics [5].

4.2.3 AC Characteristics and Energy-Performance

It can be seen from Fig. 4.2 that the fully elevated Ge-source TFET design offers the highest I_{ON}/I_{OFF} ratio, and that I_{ON} increases with Ge thickness. However, increasing T_{Ge} increases the total gate capacitance (C_{GG}) which compensates the effect of increasing I_{ON} with regard to switching speed ($t_{delay} = CV/I$) [9]. (This trade-off is favorable when the device drives a significant interconnect capacitance.) As a result, this section will address the capacitance components inherent to the TFETs and their impact on device switching speed and energy efficiency.

As expected from its structure, the raised Ge-source design inherently suffers from larger parasitic capacitances due to its source design that overlaps with the gate. In addition to a larger gate-to-source capacitance (C_{GS}), TFETs in general suffer from intrinsically larger gate-to-drain capacitance (C_{GD}) as compared to a MOSFET. This is fundamentally due to the differences in the inversion charge distribution [10, 11]; as addressed in previous chapter, V_{DS} pinchoff in a TFET occurs near the source region of the device due to the presence of a large tunnel resistance, which makes it electrically favorable for the inversion charges to be connected to the drain. As a result, C_{GD} constitutes a larger fraction of the total gate capacitance (C_{GG}) in both linear and

saturation region in a TFET [11]. Note that for a MOSFET in the linear region, both source and drain regions are connected to the inversion layer, and hence $C_{GD} \approx C_{GS} \approx 1/2C_{GG}$, and in saturation region $C_{GS} \approx 2/3C_{GG}$ and $C_{GD} \approx 0$ due to pinchoff occurring near the drain region [9, 11].

Fig. 4.4 shows the AC simulations results of C_{GS}, C_{GD}, and C_{GG} *vs*. V_{GS} for various V_{DS} values of a raised Ge-source TFET with T_{Ge} = 25 nm. It can be seen that the gate-to-(p^+)source capacitance is largest when the device is in the off state due to the accumulation of holes at the gate dielectric interface in the (p^+)source and (p)channel regions. C_{GS} decreases with an increase in V_{GS} since the Ge depletion region thickness increases with gate bias (Fig 4.4(a)). C_{GD} exhibits much stronger dependence on V_{GS} which confirms that the inversion charges are connected to the drain (Fig. 4.4(b)). The combined effect of the two capacitance components can be seen in Fig. 4.4(c); in the on-state, the total gate capacitance is dominated by gate-to-(n^+)drain capacitance, due to the inversion layer of electrons at the gate dielectric interface in the channel region which constitutes a larger capacitance. It is important, however, to note that the minimum capacitance is still established by C_{GS} rather than C_{GD}. This suggests that the thickness of the gate-to-source overlap area must be optimized to leverage the current gain *vs*. capacitance degradation. Fig. 4.5 shows the comparison of the simulated C_{GG} vs. V_{GS} characteristics for planar, partially elevated, and fully elevated Ge-source TFETs.

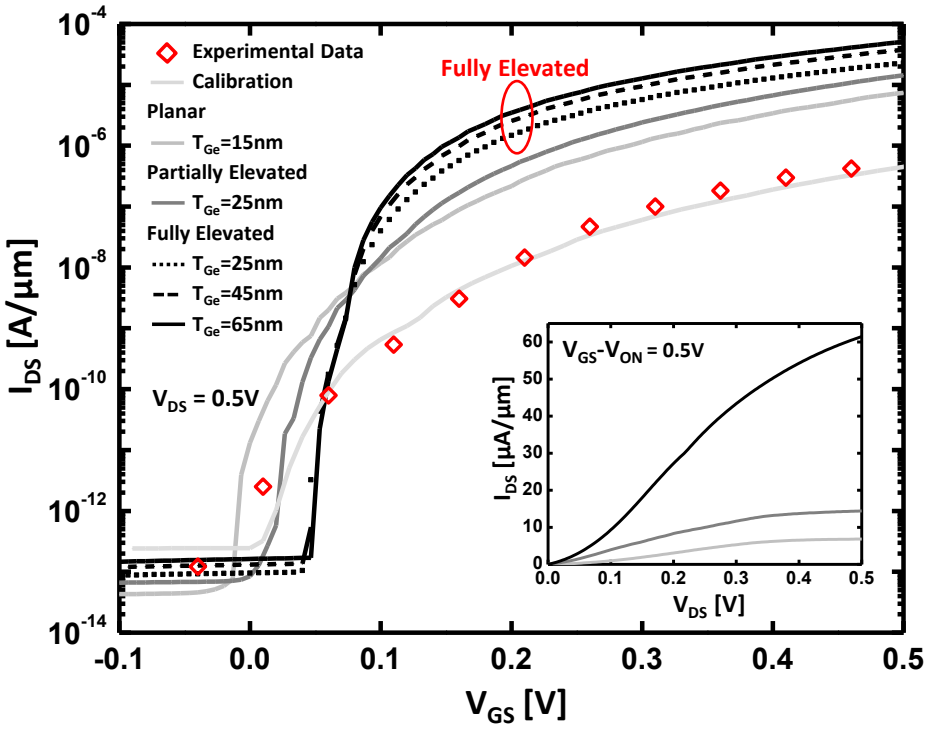


Fig. 4.2 Simulated transfer characteristics for planar, partially elevated, and fully elevated Ge-source TFETs. Experimental data from [1] and the corresponding simulated curve using the calibrated model are shown for reference. Inset: simulated output characteristics for planar (T_{Ge} = 15 nm), partially elevated (T_{Ge} = 25 nm), and fully elevated (T_{Ge} = 65 nm) Ge-source TFETs. V_{ON} is defined as the gate voltage at the onset of BTBT, which is extracted by determining the gate voltage at which the transconductance increases by more than an order of magnitude.

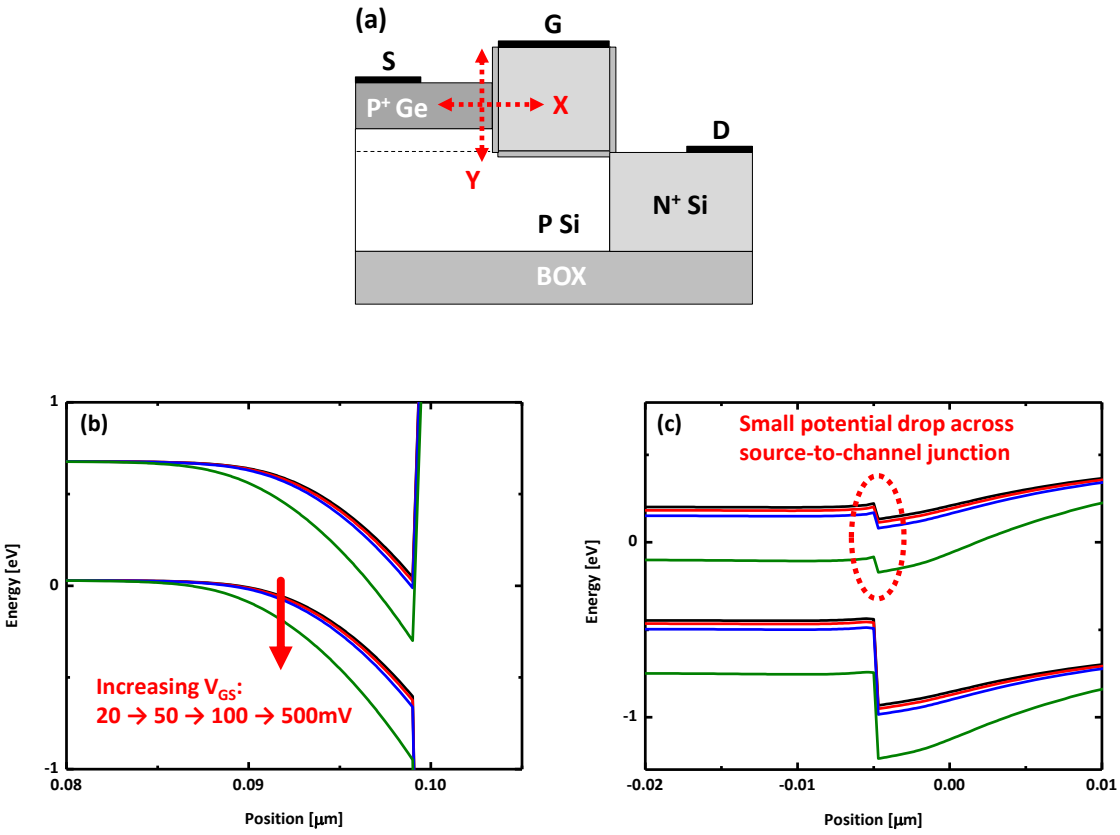


Fig. 4.3 (a) Schematic cross section of the raised Ge-source TFET. Energy band diagram for various gate voltages along the (b) x-direction (lateral direction within the source region) and (c) y-direction (vertical direction across the source to the channel junction). Because the source region is non-degenerately doped and gated, the lateral potential drop across the source-to-channel junction is small.

Using the DC and AC simulation results, the energy-delay performance of each TFET structure is evaluated using the methodology described in Chapter 4. The fully elevated Ge source design is projected to achieve the best delay because of its higher I_{ON} (Fig. 4.6(a)), saturating for $T_{Ge} >$ 45 nm. The best energy *vs*. delay (1/frequency) performance is achieved with $T_{Ge} = 25$ nm (Fig. 4.6(b)). The curves for 22 nm L_G MOSFET [3] are also shown in Fig. 4.6 for comparison. The TFET is not favorable for operation at high frequencies (>1 GHz) because it cannot achieve very high I_{ON}. At lower frequencies, however, the fully elevated Ge source TFET can achieve better energy efficiency than the MOSFET. This is because the TFET can operate at $V_{DD} < 0.3$ V (corresponding to the sub-threshold regime of operation of the MOSFET) with steeper swing. Reasonable performance (>100 MHz) is projected for the fully elevated Ge source TFET design, for V_{DD} down to 0.1 V.

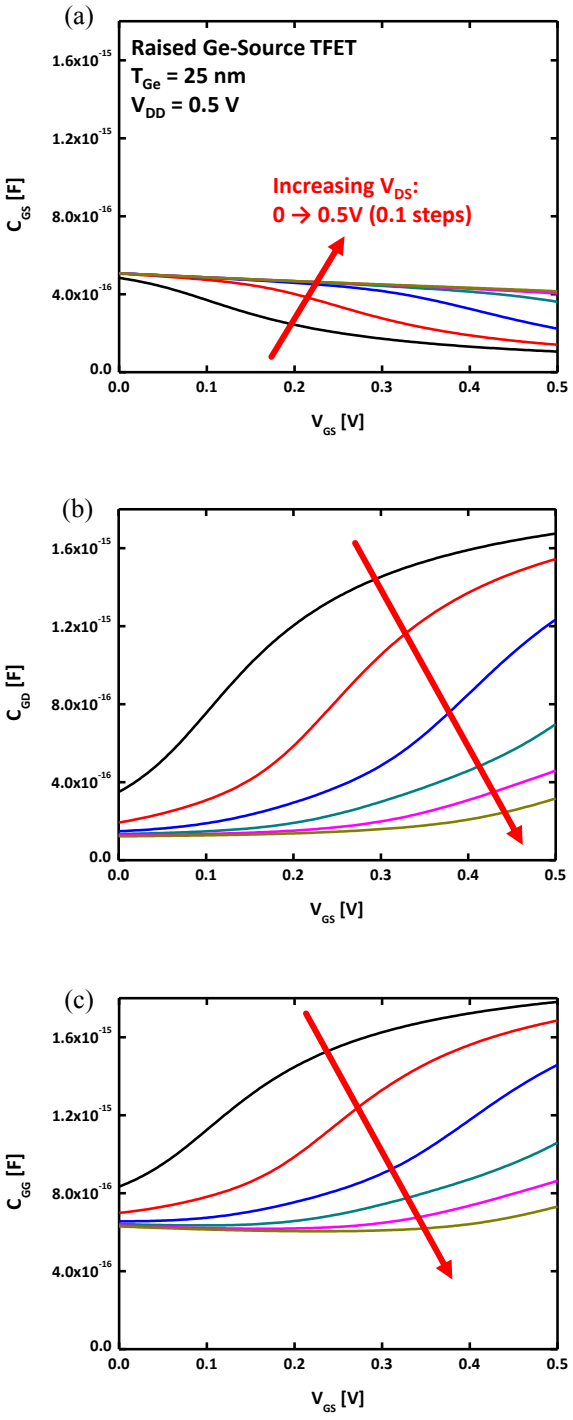


Fig. 4.4 AC simulation results of (a) C_{GS}, (b) C_{GD}, and (c) C_{GG} *vs*. V_{GS} for various values of V_{DS} of a raised Ge-source TFET with Ge thickness of 25 nm. The total capacitance is dominated by C_{GD}, but the minimum defined by C_{GS}.

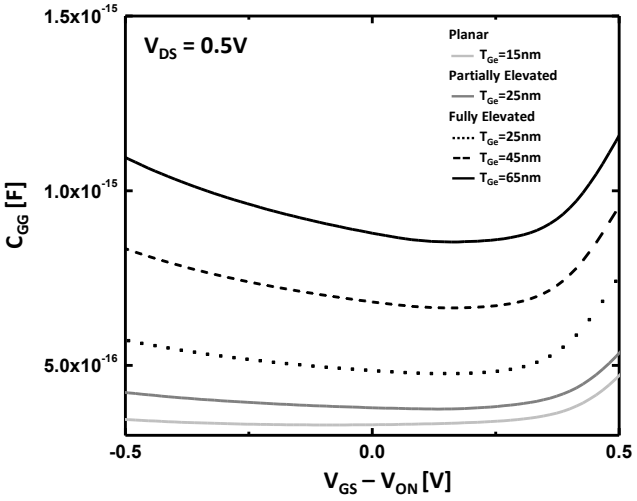


Fig. 4.5 Simulated gate capacitance versus gate voltage (C_{GG}–V_{GS}) characteristics for planar, partially elevated, and fully elevated Ge-source TFETs. C_{GG} is dominated by C_{GS} in the OFF state and by C_{GD} in the ON state. V_{ON} is defined as the gate voltage at the onset of BTBT.

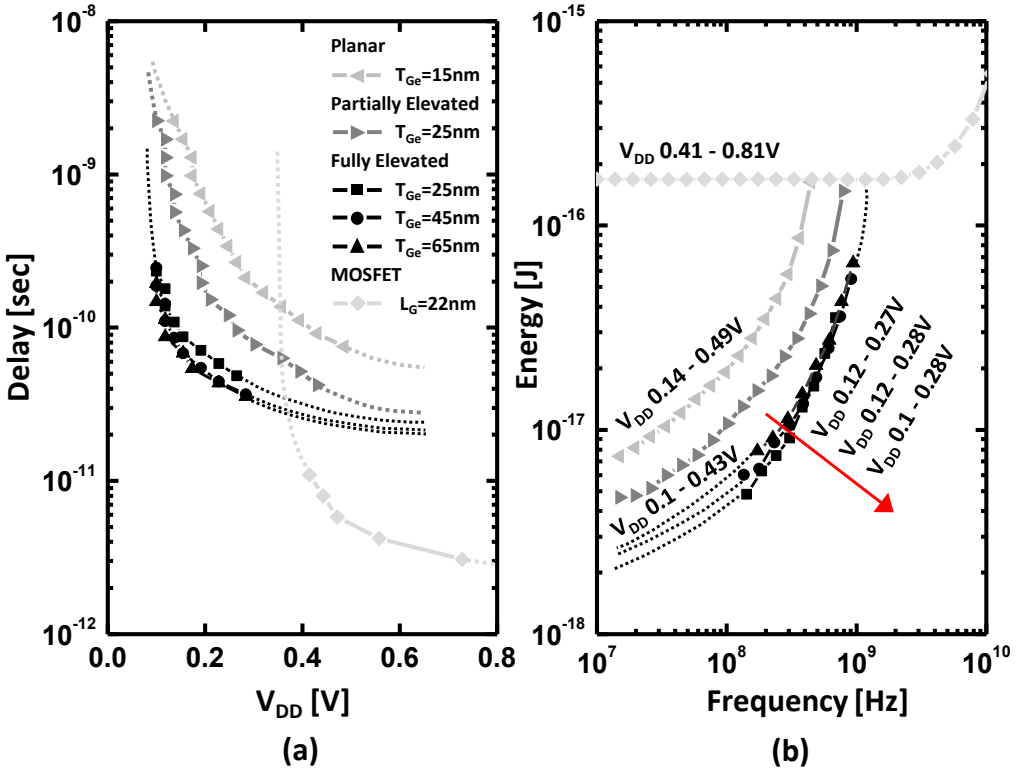


Fig. 4.6 Simulated (a) minimum-energy delay versus V_{DD} and (b) energy/cycle versus frequency of the TFETs versus MOSFET for a 30-stage FO1 inverter chain (activity factor = 0.01). Projections are indicated by the dotted lines.

4.2.4 Scalability of Raised Ge-Source TFET

A major disadvantage associated with the planar Ge-source TFET was that the scalability of the channel length (defined to be from the edge of the gate-to-source overlap region to the drain region) was fundamentally limited to 25 nm, below which direct source-drain tunneling degrades the off-state leakage current [6-7]. An obvious way to address this issue is to scale V_{DD} in conjunction with physical gate length, but this reduces I_{ON} significantly (although overall energy efficiency could still be better than that of a MOSFET technology, the frequency range for which a TFET is more advantageous could be too low to be of an interest). In contrast, the raised Ge-source design allows for much aggressive gate length and supply voltage scaling (L_G down to sub-10 nm and V_{DD} to 0.25 V, respectively) while maintaining superior performance.

The physical parameter in the raised Ge-source TFET that allows for such an aggressive scaling is the Si offset layer thickness (T_{OFFSET}, Fig. 4.1(c)). Note that the original purpose of T_{OFFSET} was to physically displace the Ge-source region away from the corner of the channel region (weaker field region) so that the lateral drain voltage drop across the source to channel junction could be minimized. However, by increasing T_{OFFSET}, the effective channel length (defined to be from the edge of the source region to the drain region along the channel) can be elongated for the same printed gate length.

Fig. 4.7 shows the simulated gate-length dependent transfer and output characteristics for the raised Ge-source TFET with T_{Ge} = 25 nm. Note that T_{OFFSET} was increased by 10 nm (from 5 nm) and V_{DD} reduced to 0.25 V (from 0.5 V) for devices with L_G = 10 and 25 nm. As a consequence, I_{OFF} is observed to be maintained at identical levels for gate lengths 100 nm down to 10 nm (Fig. 4.7(a)). The impact of supply voltage reduction on I_{ON} can be observed in Fig. 4.7(b). Due to steep switching behavior for an extremely low threshold voltage (V_T), the device operation at V_{DD} = 0.25 V (*vs*. operation at V_{DD} = 0.5 V) reduces I_{ON} only by 4x while maintaining same I_{OFF}. The results suggest that an even more aggressive L_G and V_{DD} scaling can be expected from the raised Ge-source structure with minimal penalty in performance.

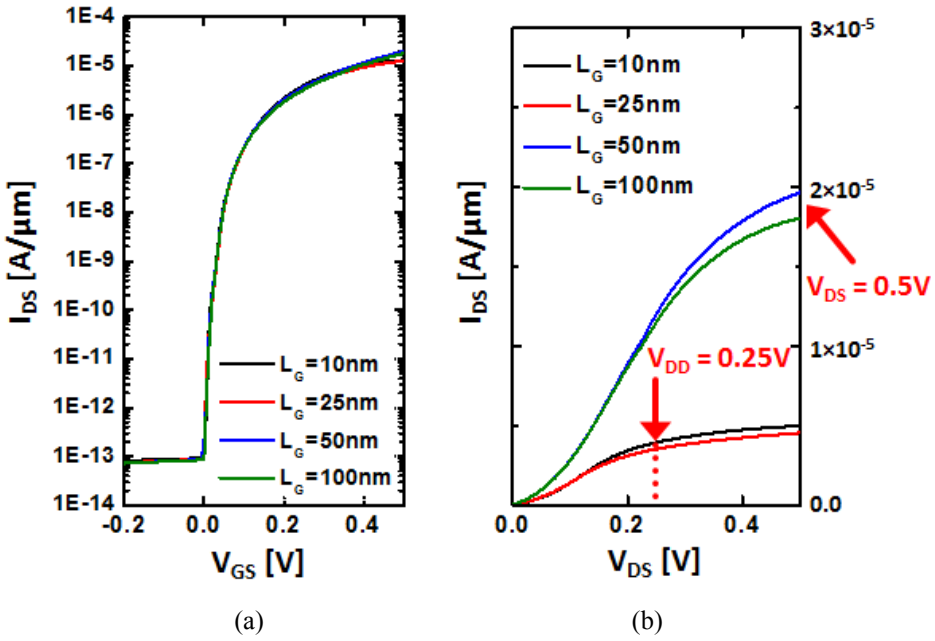


Fig. 4.7 Simulated (a) transfer and (b) output characteristics for fully elevated Ge-source TFET (T_{Ge} = 25 nm) for various gate lengths. In order to minimize I_{OFF} degradation, T_{OFFSET} was increased to 15 nm (from 5 nm) for devices with L_G = 10 nm and 25 nm.

4.3 Device Fabrication

4.3.1 Process Flow

N-channel TFETs (parameters listed in Table 4.1) were fabricated on lightly doped p-type silicon-on-insulator (SOI) wafers with 100 nm of Si (T_{BODY}) and 200 nm of buried-oxide layer (T_{BOX}) (Fig. 4.8(a)). After double-exposure of the gate and source regions, masked ion implantation (7×10^{13} As^+/cm^2 at 15keV, 7° tilt) followed by rapid thermal annealing (5 sec at 950°C in N_2) was used to dope the drain regions heavily n-type (Fig. 4.8(b)). Next, *in-situ* boron-doped polycrystalline Ge (poly-Ge) was selectively deposited at 425°C and 400 mT in a hot-wall low-pressure chemical vapor deposition (LPCVD) reactor, using GeH_4 (15 sccm) and 1%BCl_3 /99%He (35 sccm) as the Ge and dopant source gases, respectively (Fig. 4.8(c)). The active carrier concentration corresponding to this deposition condition is determined to be 3×10^{19} cm^{-3} (more details in section 4.3.2).

After immediately capping the Ge layer with low-temperature-deposited oxide (LTO) (deposited at 400°C), active areas were patterned using optical lithography and dry etching (Fig. 4.8(c)). Then the drain-implant half-gate mask was used to pattern the photoresist to cover only the source region, after which the LTO and Ge layers were removed from all other areas of the device via dry etching to form the L-shaped gate (Fig. 4.8(d)). The Si layer was also anisotropically etched by 5-10 nm to introduce the Si offset layer (T_{OFFSET}, Fig. 4.8(d)). Fig. 4.9 shows a plan-view scanning electron micrograph (SEM) of a TFET after the drain-implant half-gate-masked etch process. The wafers were subsequently cleaned in dilute HF (10s in 100:1 H_2O:HF) and placed in the atomic layer deposition (ALD) chamber for Al_2O_3 deposition (57 cycles at 300 °C, 5 nm thick) (Fig. 4.8(e)). P^+ poly-$Si_{0.4}Ge_{0.6}$ gate 300 nm thick was subsequently deposited and patterned (Fig. 4.8(e)). Another LTO (passivation) layer then was deposited (at 400°C) and patterned for contact openings (Fig. 4.8(e)). Metallization was performed by sputtering 5 nm of TiN followed by 95 nm of Al, and etched to form source, drain, and gate pads (Fig. 4.8(e)). Device fabrication was completed with a series of two-step forming-gas anneal (30 min at 400°C and 30 min at 300°C) to improve SiO_2 interface properties and contact resistance of Ge and Si.

The mask for the n-channel TFET also integrated n-channel MOSFET designs (Fig. 4.10), which permitted simultaneous fabrication of both devices. The major difference in terms of the process flow is that the n-MOSFET received both the source and drain implants during the n-TFET drain implant process (7×10^{13} As^+/cm^2 at 15keV, 7° tilt). Furthermore, LTO and Ge layers were completely etched away from all regions of the device (*vs*. LTO and Ge remaining on the source region of n-TFET) during n-TFET L-gate etch process. All of the subsequent processes remained identical for both devices.

Parameter	Value
L_G	0.25-5μm
W	0.25-50μm
T_{OX}	5nm
T_{BOX}	200nm
T_{BODY}	100nm
T_{Ge}	30, 60, 90nm
T_{OFFSET}	5-10nm

Table 4.1 Device parameters for the fabricated raised Ge-source n-channel TFET.

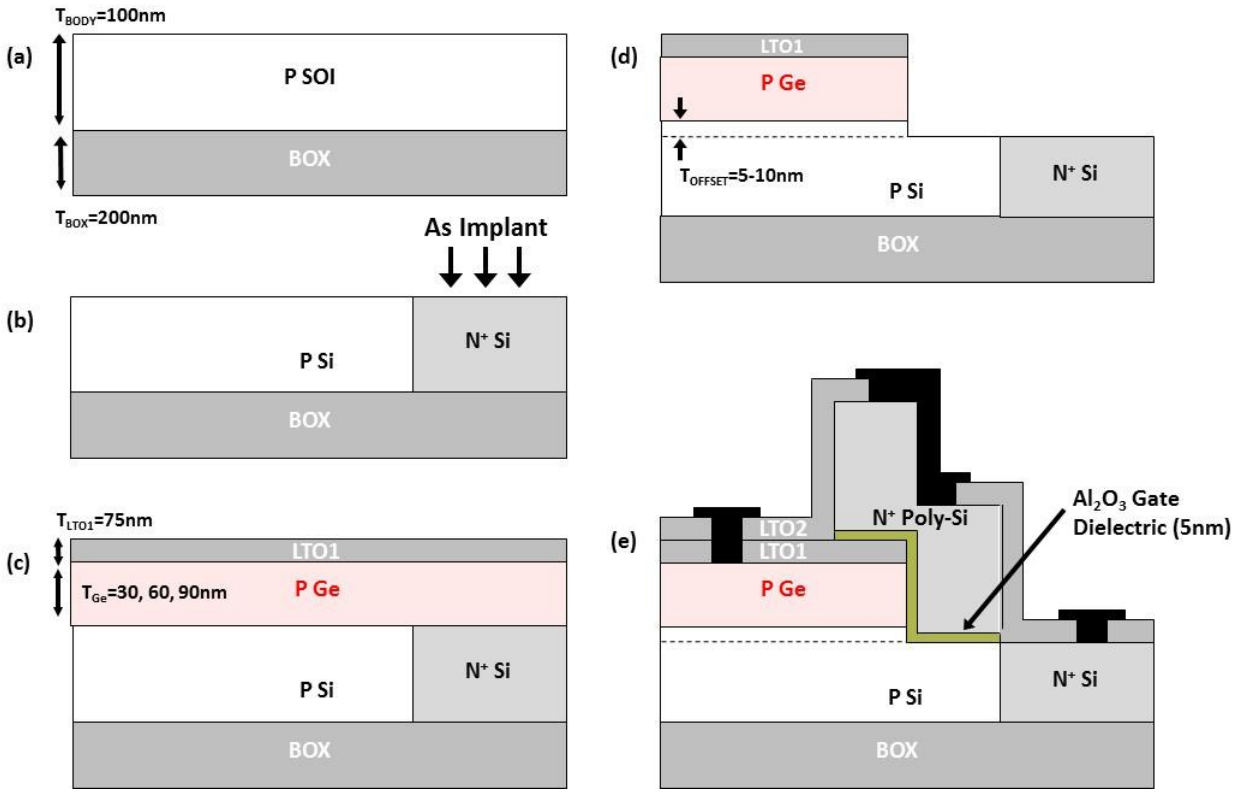


Fig. 4.8 Process flow for the raised Ge-source n-channel TFET. Starting with (a) SOI wafers, (b) drain region is implanted with As^+. Then (c) poly-Ge and LTO hardmask are deposited and (d) patterned anisotropically using drain-implant half-gate mask. (e) Gate stack consisting of Al_2O_3 gate-dielectric, P^+ poly-$Si_{0.4}Ge_{0.6}$ gate, and LTO gate-hardmask are deposited and patterned. After another LTO passivation, contact holes were patterned and deposited with TiN and Al for contact.

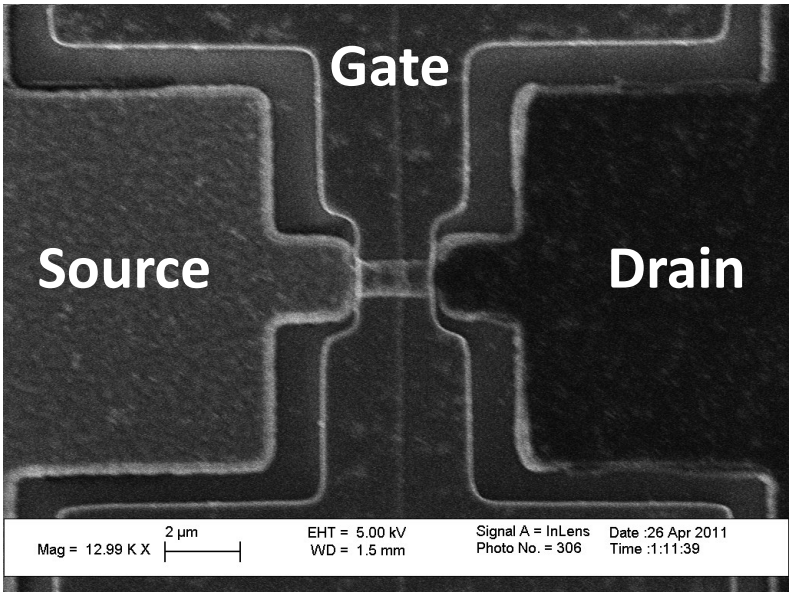


Fig. 4.9 Plan view scanning electron micrograph of the Ge-source TFET after the drain-implant half-gate-masked anisotropic etch process of poly-Ge.

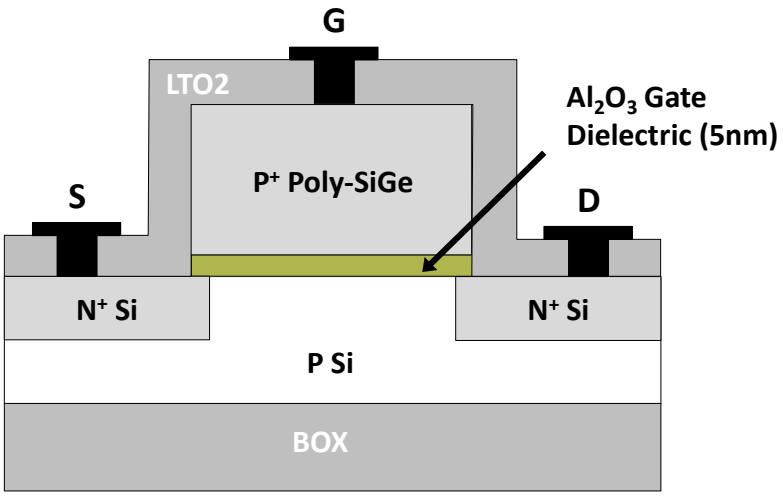


Fig. 4.10 Schematic cross section of the n-channel MOSFETs which were co-fabricated with the n-channel TFETs.

4.3.2. Polycrystalline Germanium Doping Characterization

As addressed in chapter 3, BTBT in a Ge-source TFET is heavily dependent on the Ge doping concentration in the source region and the corresponding optimal value was found to be ~1×10^{19} cm^{-3} for perpendicular tunneling [4]. Hence, in order to maximize the performance of the *as*-fabricated device, a proper characterization and understanding of the active carrier concentration is mandatory. Three methods have been employed to characterize the poly-Ge doping profile: Hall measurements, 4-pt probe measurements, and secondary ion mass spectrometry (SIMS) analysis.

The samples were prepared on (100)-oriented lightly doped p-type SOI wafers with 100 nm of Si and 200 nm of buried-oxide layer. 100 nm of *in-situ* boron-doped poly-Ge was deposited in a hot-wall LPCVD reactor, using GeH_4 (15sccm) as the Ge source gas and 1%BCl_3 /99%He (variable fluxes, in sccm) as the dopant source gas at 425°C and 400 mT. The Hall samples were prepared by dicing the poly-Ge deposited SOI substrates into 5 mm × 5 mm squares, after which indium (In) was manually pressed at each corners to form contact region.

Fig. 4.11(a) shows the dependence of the active carrier concentration on the BCl_3 flux rate comparing Hall and 4-point probe measurements. As expected, the carrier concentration increases with BCl_3 flux rate but begins to saturate for ≥ 35 sccm due to lower solubility limit imposed by the Ge grains [12-16]. Fig. 4.11(b) and (c) show the corresponding resistivity and mobility measurements, respectively; the results exhibit peak resistivity (and corresponding minimum mobility - Hall measurements only) for BCl_3 of 25 sccm, which suggest a change in the polycrystalline morphology with respect to this flux rate [13]. SIMS analysis is performed on the optimal deposition condition (BCl_3 flux rate = 35 sccm) and is confirmed to match against the Hall and 4-pt probe measurements (Fig. 4.12).

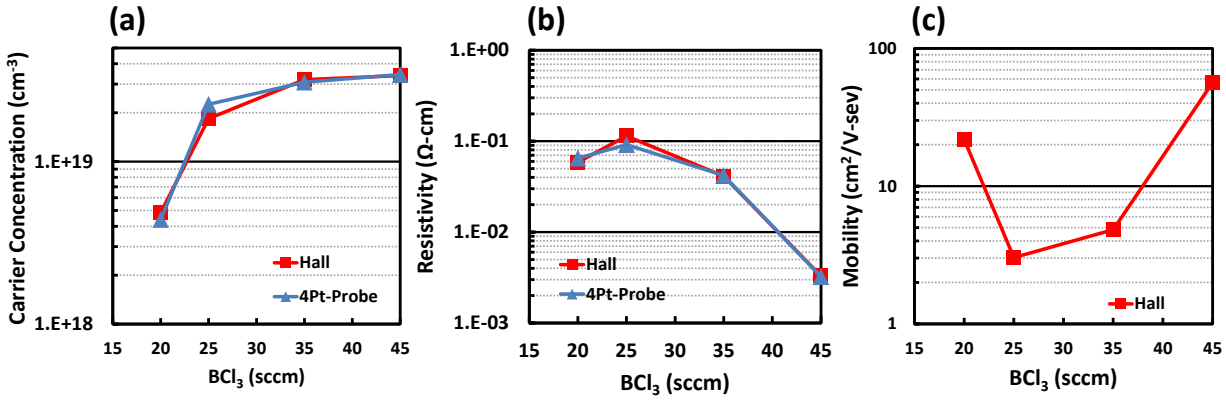


Fig. 4.11 Comparison between Hall and 4-point probe measurements for the (a) active carrier concentration, (b) resistivity, and (c) mobility *vs*. BCl_3 flux rate of the LPCVD furnace. The samples were prepared by depositing 100 nm of poly-Ge on p-type SOI substrates.

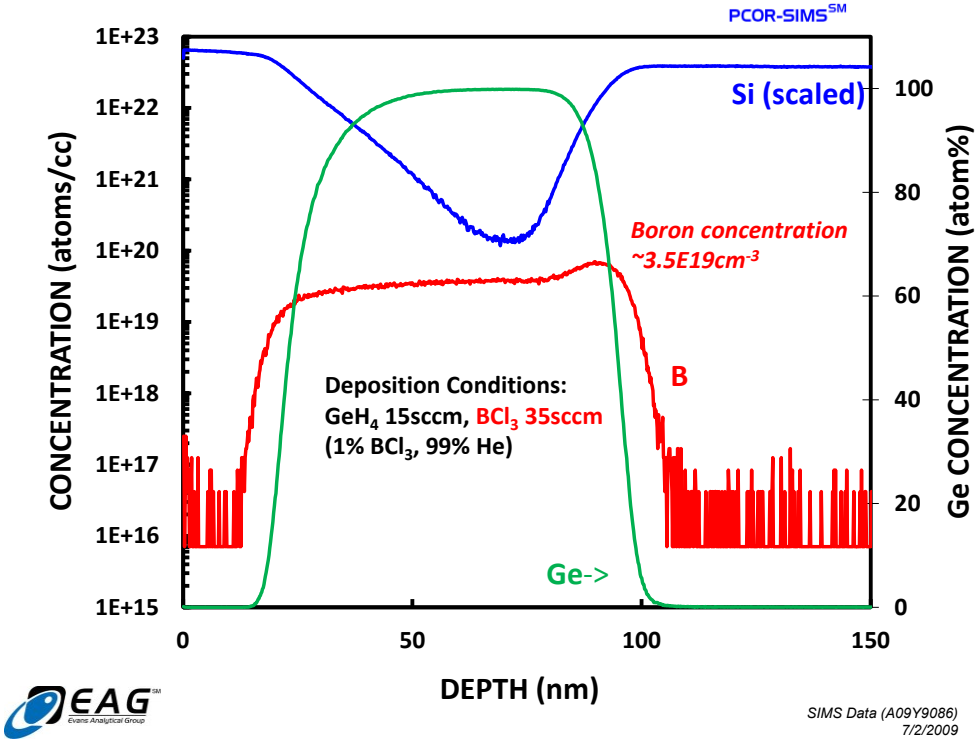


Fig. 4.12 Secondary ion mass spectrometry (SIMS) analysis for the optimal BCl_3 flux rate of 35 sccm. The measured B concentration (~3.5×10^{19} cm^{-3}) agree well with Hall and 4-point probe measurements.

4.4 Device Measurements

The measured I_{DS} *vs*. V_{GS} characteristics and the corresponding S *vs*. V_{GS} are plotted for various V_{DS} values in Fig. 4.13 for a long-channel (2 µm) raised Ge-source TFET with T_{Ge} = 90 nm. The leakage current is shown to increase exponentially (from 50 fA/µm to 1pA/µm) with V_{DS} due to enhanced ambipolar tunneling current from the drain to the channel. I_{ON} (I_{DS} at V_{GS} = 2.5 V) also exhibits drain voltage dependence since V_{DS} couples laterally within the source (rather than across the source to channel junction) to modulate the perpendicular tunneling rate [5]. Despite the use of the P+ poly-$Si_{0.4}Ge_{0.6}$ gate for an n-channel device, the threshold voltage remains moderate which is likely to be compensated by the relatively large fixed charge density at the Al_2O_3/Ge interface [17].

Fig. 4.13(b) shows that the subthreshold swing rather poor with its minimum around 200 mV/dec. This is attributed to the rough Ge surface profile near the gate-dielectric interface formed during the anisotropic etch process as a result of a non-uniform etch rates imposed by the poly-Ge grain

boundaries (Fig. 4.14). The consequence of this rough topology is that it introduces local variation in the effective oxide thickness (EOT) which results in non-uniform BTBT rates across the source region. The net subthreshold swing is then defined by the envelope of these different turn-on behavior, which results in degrade characteristics.

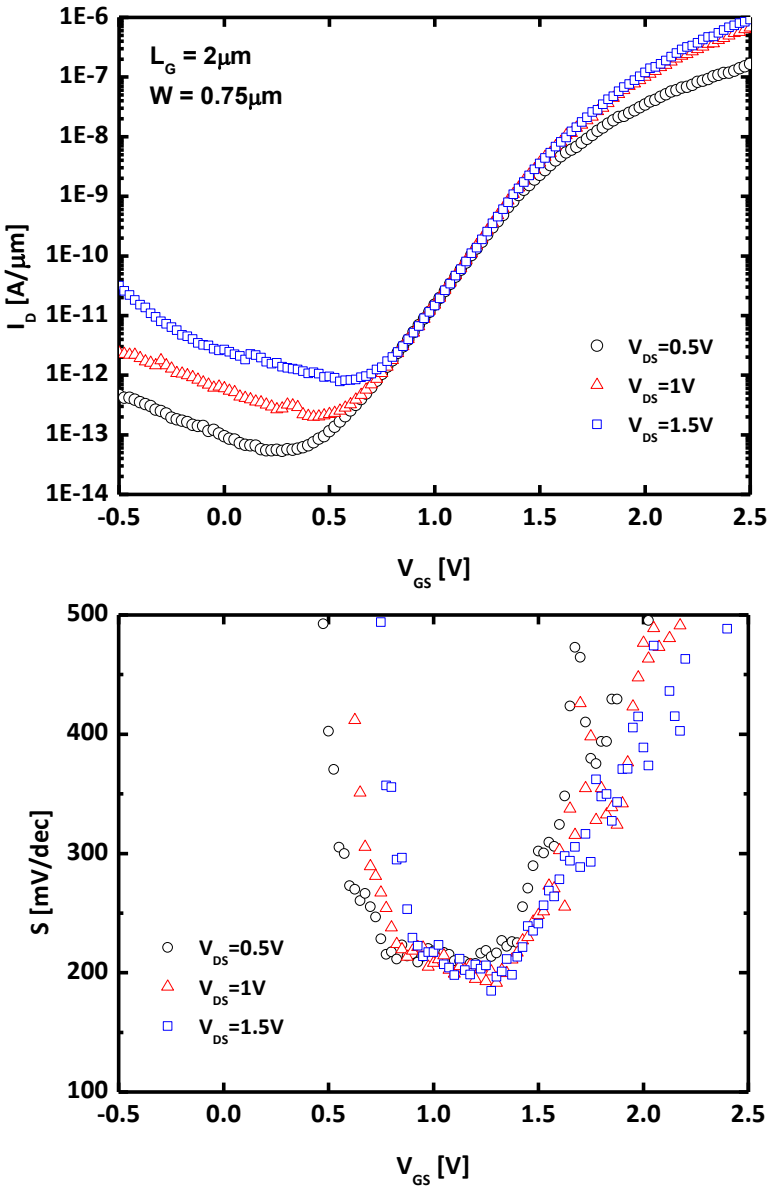


Fig. 4.13 (a) Measured I_{DS}-V_{GS} and (b) S-V_{GS} characteristics for various V_{DS} values of a long-channel (2 μm) TFET.

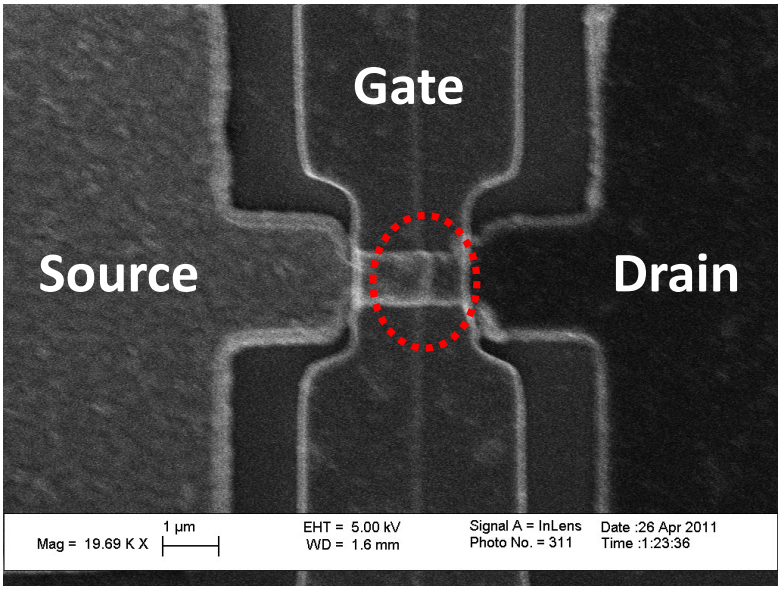


Fig. 4.14 Higher magnification plan-view SEM of Fig. 4.9. The Ge-source region near the gate-dielectric interface is shown to be rough due to non-uniform etch rate introduced by the poly-Ge grain boundaries.

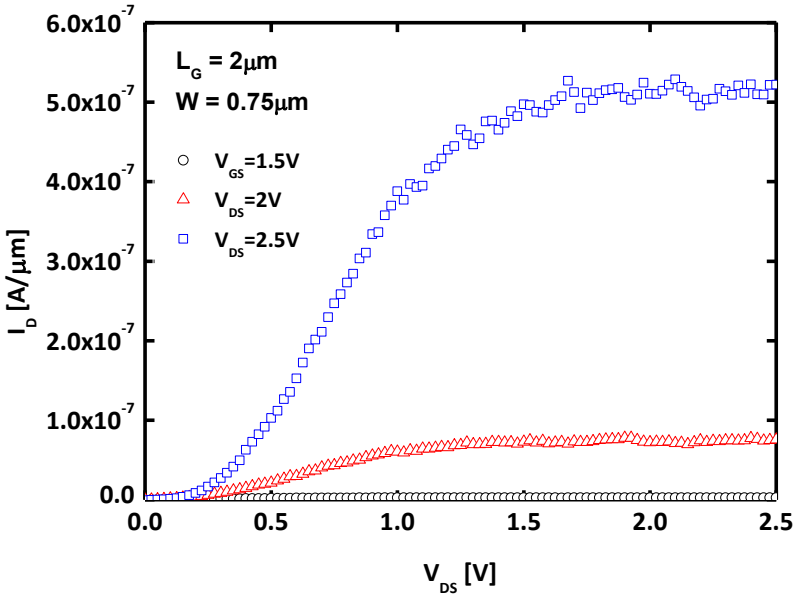
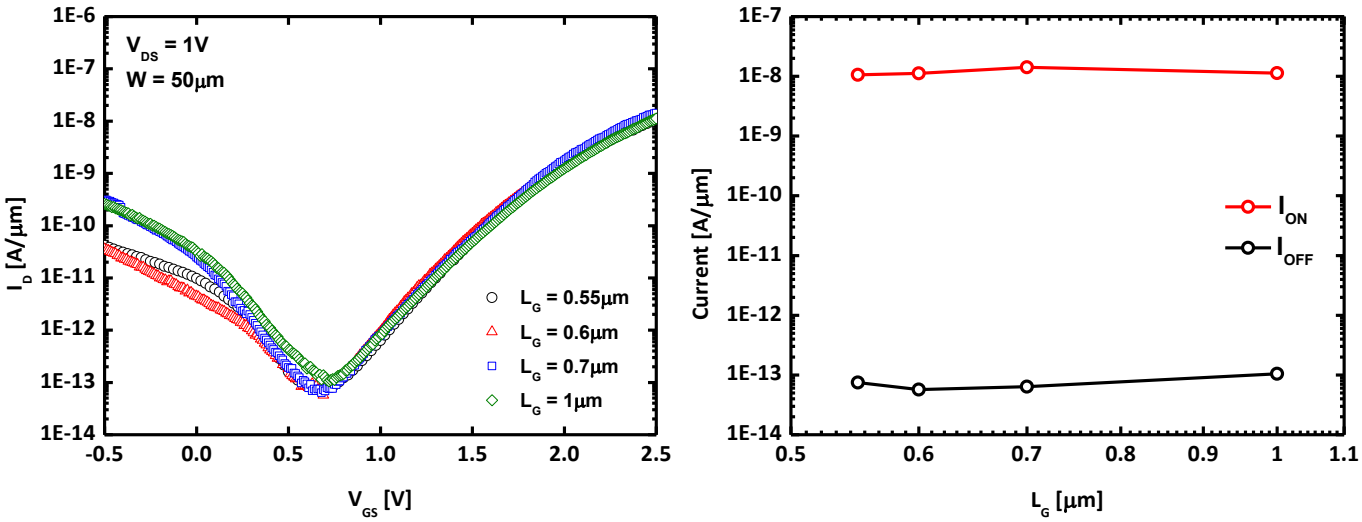


Fig. 4.15 Meaured I_{DS}-V_{DS} characteristics for various V_{GS} values showing non-linear turn-on characteristics.

The measured output characteristics are shown in Fig. 4.15. The drive current for 2.5 V supply voltage operation is 0.5 µA/µm. A non-linear turn-on behavior is expected for a raised Ge-source TFET since the drain voltage is dropped laterally within the Ge source (due to reduced potential drop across the source to channel junction) which leads to a direct modulation of the tunnel barrier thickness [5]. These results are consistent with the simulation results (Fig. 4.2 inset).

Similar to the behavior of the planar Ge-source design, the drive current of a raised source structure shows minimal dependence on gate length (Fig. 4.16) since the I_{ON} is source-side BTBT limited [18]. I_{OFF} is also shown to be immune to L_G, but is expected to degrade for sub-0.05 µm gate lengths [6, 7]. The gate-width dependence on the transfer characteristics is shown in Fig. 4.17 for TFETs with L_G = 1µm. The degraded I_{OFF} for narrower devices suggests that the ambipolar tunneling current across the drain to channel junction is enhanced due to additional gate-fringing electric field towards the edges.

Fig. 4.18 shows the measured transfer characteristics for the n-MOSFETs that were fabricated using the same masks as the n-TFETs. Due to a non-optimized MOSFET design, an L_G = 1µm device exhibits large threshold voltage rolloff due to short-channel effects (SCE) and I_{OFF} degradation from gate-induced drain leakage (GIDL) [19]. The saturation region also suggests large contact resistance associated with TiN and Al and require further optimized process flow [20].



(a) (b)

Fig. 4.16 (a) Meaured I_{DS}-V_{DG} characteristics for various L_G and corresponding (b) I_{ON} and I_{OFF} *vs.* L_G. I_{ON} is defined as I_{DS} for 2.5 V gate voltage swing; I_{OFF} is defined as the minimum I_{DS}.

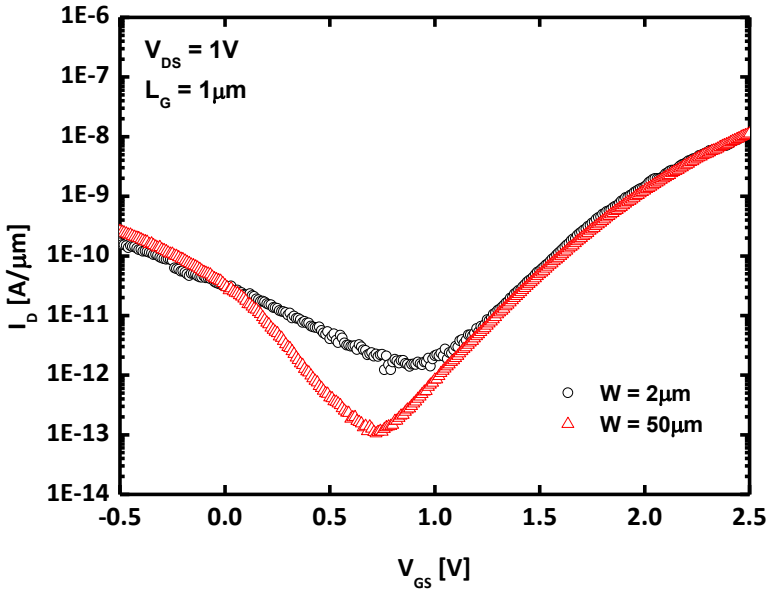


Fig. 4.17 Measured I_{DS}-V_{DG} characteristics for various device widths. I_{OFF} degradation is observed for narrower W devices.

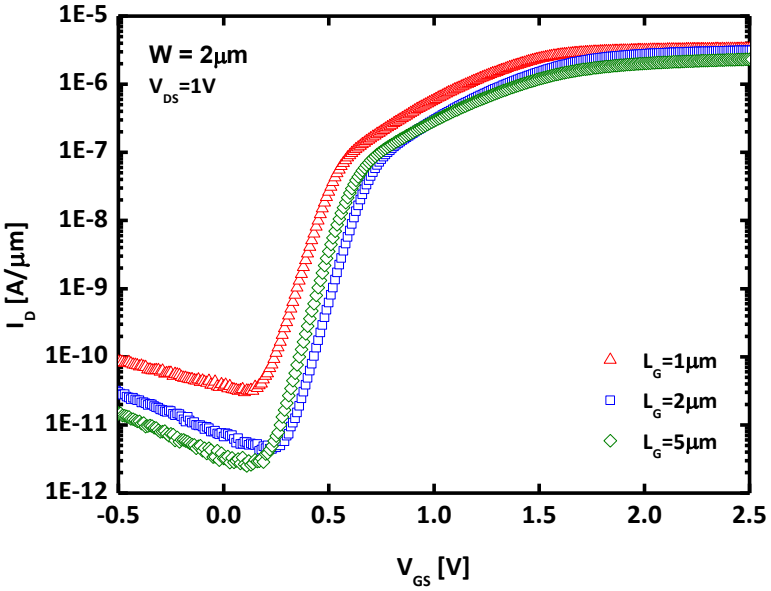


Fig. 4.18 Measured I_{DS}-V_{DG} characteristics for n-MOSFETs that were fabricated using the same masks as the n-TFETs.

4.5 Summary

This chapter proposed and demonstrated raised Ge-source n-channel TFET which overcame the fundamental limits associated with the planar design. The raised structure was shown to suppress lateral tunneling and achieve steeper switching behavior and higher I_{ON} for an even lower supply voltage operation. DC and AC simulation results were used to determine the energy and delay performance from which the optimal Ge thickness for the greatest energy efficiency was found. The performance of this new TFET design was then benchmarked against that of CMOS technology and other Ge-source TFET design, and demonstrated that it can offer lower energy per operation for throughput in the frequency range up to 1 GHz for sub-0.5 V operation. A significant improvement in terms of the device scalability was also discussed.

Raised Ge-source n-channel TFETs were experimentally demonstrated using the gate-last approach based on conventional CMOS process flow. The device measurements for the best performing device showed I_{OFF} of 1 pA/μm and I_{ON} of 1 μA/μm for 2.5 V gate voltage swing. It is expected that an optimized poly-Ge etch process to minimize the surface roughness and more aggressive gate-dielectric scaling would improve the subthreshold swing and I_{ON}. Various methods to characterize the polycrystalline Ge doping concentration were discussed and the corresponding results compared for consistency.

4.6 References

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4.7 Appendix: Process Flow for Raised Ge-Source TFET

Step	Process Name	Process Specification	Equipment
0.01	Wafers	6 six inch prime SOI wafers and 22 test wafers	Soitec
0.02	Labeling	Label the wafers	
0.03	Si (SOI) Thickness Measurement	Recipe: 4. Polysilicon on Oxide, record in A	nanoduv
0.04	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
0.05	LTO Deposition	Recipe: 11SULTOA - 20min (dep. rate ~125A/min) Recipe: 12LTO400 - O2 135sccm, SiH4 90sccm, PH3 0sccm, 15min (dep. rate ~93A/min)	tystar11 tystar12
0.06	LTO Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
1.00	**Alignment Mark(PM)**		
1.01	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
1.02	Alignment Mark (PM) Lithography *(lithography 1)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle: BA-COMBI-4X, Reticle ID: **45440204D176**, Layer ID: PM Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure	svgdev6

		bake(PEB), vacuum hotplate 130C, 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	
1.03	Inspection	Microscope - PM mark inspection	uvscope
1.04	Hard Bake	UV bake: Program U, 140C, 1min	uvbake
1.05	Alignment Mark(PM) Etch	Recipe: shpkim_5003_OB_ME OB: 13mT, TCP RF 200W, bias RF 40W, CF4 100sccm, 5sec ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm, 32sec ME c-Si E.R. ~50A/sec	lam8
1.06	PR Ashing	Recipe: std - 3.75T, 400W, 250C, MFC1 40% O2, 2min 30sec	matrix
1.07	Post Cleaning	piranha, 120C, 10min	msink8
2.00	**Drain Implantation**		
2.01	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
2.02	Implant-Barrier Oxidation (Dry)	Recipe: 1DRYOXA - dry O2, 835C, 1min Post N2 anneal 950C 20min, ramp to 950C 5min	tystar1
2.03	Oxide Thickness Measurement	record in A	sopra
2.04	Gate Lithography *(lithography 2)* ***(Double lithography 1/2)***	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEVGRPCLR**, Layer ID: Poly (Image ID #1) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6

2.05	Inspection	Microscope - gate lithography inspection	uvscope
2.06	Hard Bake	UV bake: Program U, 140C 1min	uvbake
2.07	Drain Implant Lithography *(lithography 3)* ***(Double lithography 2/2)***	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEV_GRP_TFET**, Layer ID: Actv (Image ID #3) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
2.08	Inspection	Microscope - double lithography inspection	uvscope
2.09	Hard Bake	UV bake: Program U, 140C 1min	uvbake
2.10	N+ Drain Implant	As, 7E13cm-2, 15keV, 7 tilt	Core Systems
2.11	PR Ashing	Recipe: std - 3.75T, 400W, 250C, MFC1 40% O2, 2min 30sec	matrix
2.12	Post Cleaning	Piranha, 120C, 10min	msink8
2.13	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
2.14	RTA, Drain Activation Anneal	Recipe: SHPKIM10 Delay: 10sec, 0C, 1 (steady intensity factor) Ramp: 20sec, 450C, 1 Steady: 30sec, 450C, 0.8 Ramp: 10sec, 950C, 1 Steady: **5sec, 950C**, 1	heatpulse4
2.15	Post Cleaning	piranha, 120C, 10min	msink8
3.00	**Ge + LTO1 Deposition**		
3.01	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
3.02	Ge Deposition	Recipe: SGDEPF.019 - 400mT, 425C, GeH4 15sccm, BCl3 35sccm, 5min	tystar19

	(P+ poly-Ge)	(dep. rate ~60A/min)	
3.03	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
3.04	LTO1 Deposition	Recipe: 11SULTOA - 10min (dep. rate ~125A/min)	tystar11
3.05	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
3.06	Ge Deposition (P+ poly-Ge)	Recipe: SGDEPF.019 - 400mT, 425C, GeH4 15sccm, BCl3 35sccm, 10min (dep. rate ~60A/min)	tystar19
3.07	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
3.08	LTO1 Deposition	Recipe: 11SULTOA - 10min (dep. rate ~125A/min)	tystar11
3.09	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
3.10	Ge Deposition (P+ poly-Ge)	Recipe: SGDEPF.019 - 400mT, 425C, GeH4 15sccm, BCl3 35sccm, 15min (dep. rate ~60A/min)	tystar19
3.11	Preclean	piranha, 120C, 10min / 25:1 HF 1min	msink6
3.12	LTO1 Deposition	Recipe: 11SULTOA - 10min (dep. rate ~125A/min)	tystar11
3.13	LTO1 Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
4.00	**Active S/D Area Etch**		
4.01	Preclean	piranha, 120C, 10min	msink8
4.02	Active S/D Area Lithography *(lithography 4)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive	svgcoat6

		DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	
		Exposure - Reticle ID: **DEVGRPCLR**, Layer ID: Actv (Image ID #3) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
4.03	Inspection	Microscope - active S/D area lithography inspection	uvscope
4.04	Hard Bake	UV bake: Program U, 140C 1min	uvbake
4.05	Active S/D Area Etch (LTO1 etch)	Recipe: MXP_OX_VAR - 200mT, 700W, Ar 150sccm, CF4 15sccm, CHF3 60sccm E.R. ~70A/sec (recipe identical to MXP_OXIDE_ETCH) *Time: **dm-LTO1** (sec), **dm-LTO3** (sec), **L5W1** (sec), **2** (sec), **3** (sec), **4** (sec), **5** (sec), **6** (sec)*	centura-MxP
4.06	Active S/D Etch (Ge and SOI Etch)	Recipe: shpkim_8003 OB: 13mT, TCP RF 200W, bias RF 40W, CF4 100sccm, 3sec ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm *Times: **L5W1** (sec), **2** (sec), **3** (sec), **4** (sec), **5** (sec), **6** (sec)* OE: 80mT, TCP RF 200W, bias RF 150W, HBR 100sccm, O2 1sccm, He 100 sccm *Time: **L5W1** (sec), **2** (sec), **3** (sec), **4** (sec), **5** (sec), **6** (sec)*	lam8
4.07	BOX Thickness Measurement 1	Recipe: 1. Oxide on Silicon, record in A	nanoduv
4.08	PR Removal	PRS 3000, 80C, 5min	msink16
4.09	Post Cleaning	Acetone, 2min / DI rinse / 100:1 HF, 20sec / DI rinse	msink7
5.00	**Drain-Side LTO1/Ge/Si Etch**		

5.01	Preclean	Acetone, 2min / DI rinse	msink7
5.02	Drain Implant Lithography *(lithography 5)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEV_GRP_TFET**, Layer ID: Actv (Image ID #3) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
5.03	Inspection	Microscope - drain implant lithography inspection - verify alignment with 1/2·Lg	uvscope
5.04	Hard Bake	UV bake: Program U, 140C 1min	uvbake
5.05	LTO1 Etch	Recipe: MXP_OX_VAR - 200mT, 700W, Ar 150sccm, CF4 15sccm, CHF3 60sccm E.R. ~70A/sec (recipe identical to MXP_OXIDE_ETCH) *Time:* ***dm-LTO2*** *(sec),* ***dm-Ge5*** *(sec),* ***dm-Ge6*** *(sec),* ***L5W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	centura-MxP
5.06	BOX Thickness Measurement 2	Recipe: 1. Oxide on Silicon, record in A	nanoduv
5.07	Ge and Si Trench Etch	Recipe: shpkim_5003_OB_ME OB: 13mT, TCP RF 200W, bias RF 40W, CF4 100sccm, 3sec ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm *Time:* ***L5W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	lam8

5.08	BOX Thickness Measurement 3	Recipe: 1. Oxide on Silicon, record in A	nanoduv
5.09	PR Removal	PRS 3000, 80C, 5min	msink16
5.10	Postclean	Acetone, 2min / DI rinse / 100:1 HF, 20sec / DI rinse	msink7
5.11	X-SEM	X-SEM - Ge-LTO1 profile inspection	leo
6.00	**Gate Stack Deposition**		
6.01	Preclean	Acetone, 2min / DI rinse / 100:1 HF, 10sec / DI rinse	msink7
6.02	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
6.03	Al2O3 Gate-Dielectric Deposition	Recipe: Al2O3 - 300C, 55cycles ~= 5nm	picosun
6.04	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
6.05	SiGe Gate Deposition (P+ poly-Si0.4Ge0.6)	Recipe: SIGENUCF.020 Nucleation - 300mT, 410C, Si2H6 100sccm, 5min = 1nm a-Si Deposition - 600mT, 410C, SiH4 140sccm, BCl3 45sccm, GeH4 60sccm, 45min (dep. rate = ~55.6A/min)	tystar19
6.06	Dit Measurement	record Dit in cm-2	sca
6.07	Al2O3 Thickness Measurement	record in A	sopra
6.08	SiGe Thickness Measurement X-SEM	X-SEM - measure SiGe thickness - Ge-to-gate profile inspection	nanoduv
6.09	Postclean	piranha, 120C, 10min	msink8
7.00	**Gate Stack Etch**		
7.01	Preclean	piranha, 120C, 10min	msink8
7.02	Gate Lithography *(lithography 6)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm	svgcoat6

		PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	
		Exposure - Reticle ID: **DEVGRPCLR**, Layer ID: Poly (Image ID #1) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
7.03	Inspection	Microscope - gate lithography inspection	uvscope
7.04	Hard Bake	UV bake: Program U, 140C 1min	uvbake
7.05	P+ SiGe Gate Etch	Recipe: shpkim_8003 OB: 13mT, TCP RF 200W, bias RF 40W, CF4 100sccm, 3sec ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm *Time:* ***L5W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)* OE: 80mT, TCP RF 200W, bias RF 150W, HBR 100sccm, O2 1sccm, He/Ar 100 sccm *Time:* ***L5W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	lam8
7.06	BOX Thickness Measurement 3	Recipe: 1. Oxide on Silicon, record in A	nanoduv
7.07	PR Removal	PRS 3000, 80C, 5min	msink16
7.08	Postclean	Acetone, 2min / DI rinse / 100:1 HF, 20sec / DI rinse	msink7
8.00	**Passivation (Spacer) Deposition**		
8.01	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
8.02	Preclean	Acetone, 2min / DI rinse	msink7
8.03	LTO2 Deposition	Recipe: 12LTO400 - O2 135sccm, SiH4 90sccm, PH3 0sccm, 8min (dep. rate ~93A/min)	tystar12
8.04	LTO2 Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv

9.00	**Contact Via Etch**		
9.01	Preclean	piranha, 120C, 10min	msink8
9.02	Preclean	Acetone, 2min / DI rinse	msink7
9.03	Contact Lithography *(lithography 7)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEVGRPDRK**, Layer ID: Poly (Image ID #1) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
9.04	Inspection	Microscope - contact lithography inspection	uvscope
9.05	Hard Bake	UV bake: Program U, 140C 1min	uvbake
9.06	LTO2 and 1 Etch - Dry	Recipe: MXP_OX_VAR - 200mT, 500W, Ar 120sccm, CHF3 60sccm E.R. ~70A/sec (recipe identical to MXP_OXIDE_ETCH) *Time:* ***L5W1*** *(sec),* ***2*** *(sec),* ***3*** *(sec),* ***4*** *(sec),* ***5*** *(sec),* ***6*** *(sec)*	centura-MxP
9.07	PR Removal	PRS 3000, 80C, 5min	msink16
9.08	LTO2 and 1 Etch - Wet	100:1 HF / DI rinse	msink7
9.09	BOX Thickness Measurement 4	Recipe: 1. Oxide on Silicon, record in A	nanoduv

******** PRELIMINARY TFET MEASUREMENTS (without metalization) ********

10.00	**Metalization**		
10.01	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	msink6
10.02	Preclean	Acetone, 2min / DI rinse / 100:1 HF, 10sec / DI rinse	msink7
10.03	AlSi Deposition	Recipe: LWAL - 30sec => ~150nm of Al	novellus
10.04	Metal Lithography *(lithography 8)*	PR Coating: Program 1 - HMDS prime, bake temp. 100C, prime 60sec, chill 60sec PR Coating: Program 2 - Rohm-Haas positive DUV 210 resist, 0.9um, 1480rpm PR Coating: Program 1 - soft bake, 130C, 60sec, chill 6sec	svgcoat6
		Exposure - Reticle ID: **DEVGRPCLR**, Layer ID: Metal (Image ID #4) Job: Device_Group/STD_devgrp2011, Control Mode: C, Batch Type: P, Energy 18mJ/cm^2	asml300
		Development: Program 1 - post exposure bake(PEB), vacuum hotplate 130C 1min, chill 6sec Development: Program 1 - developer: Rohm-Hass MF-26A, spray/puddle, 21.5C, 45sec Development: Program 9 - no hard bake	svgdev6
10.05	Inspection	Microscope - metal lithography inspection	uvscope
10.06	Hard Bake	UV bake: Program U, 140C 1min	uvbake
10.07	X-SEM	SEM - Al thickness measurements	leo
10.08	AlSi Etch	Recipe: MET_AL_VAR - 10mT, RF 1000W, Bias 100W, BCl3 45sccm, Cl2 90sccm E.R. ~ A/sec (recipe identical to MET_AL_ME) *Time: **L5W1** (sec), **2** (sec), **3** (sec), **4** (sec), **5** (sec), **6** (sec)*	centura-MET
	P+ SiGe Etch (MOSCAP)	Recipe: shpkim_8003 OB: 13mT, TCP RF 200W, bias RF 40W, CF4	lam8

		100sccm, 3sec ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm *Time:* ***dm-imp-moscap*** *(sec)* OE: 80mT, TCP RF 200W, bias RF 150W, HBR 100sccm, O2 1sccm, He/Ar 100 sccm *Time:* ***dm-imp-moscap*** *(sec)*	
10.09	PR Ashing	Recipe: std - 3.75T, 400W, 250C, MFC1 40% O2, 2min 30sec	matrix
10.10	Postclean	Acetone, 2min / DI rinse	msink7

******** dm-imp-moscap ready for C-V measurements ********
******** dm-imp-diode ready for MS diode measurements ********
******** SECONDARY TFET MEASUREMENTS ********

11.00	**Forming Gas Anneal**		
11.01	Preclean	Acetone, 2min / DI rinse	msink7
11.02	Forming Gas Anneal	Recipe: H2SINT4A.018, 400C, forming gas(10% H2, 90% N2, 3000sccm), 30min	tystar18

******** Final MOSCAP and MS diode measurements ********
******** Final TFET MEASUREMENTS ********

Chapter 5

Germanium-Source TFET-Based Digital Logic Design

5.1 Introduction

The previous chapters have investigated planar and raised Ge-source n-channel TFETs and have shown that progressing from the planar to the raised-source design suppresses lateral tunneling and achieves steeper switching behavior for a higher on-state drive current (I_{ON}) at a lower supply voltage (V_{DD} < 0.5 V) [1]. The next step is to employ the optimized raised Ge-source TFETs to examine their application for digital logic. This chapter will begin by addressing the fundamental challenges associated with TFETs for logic design. Then, in order to mitigate these challenges, a circuit-level solution based on n-TFET pass transistor logic will be proposed and demonstrated through mixed-mode simulations. The accompanying design modifications required at the device level will be discussed.

5.2 TFET-Based Circuit Design Constraints

5.2.1 One-Way Current Flow

Due to its symmetric source and drain structures, a MOSFET can conduct current in both directions (from source to the drain and vice versa) depending on the terminal voltages. A TFET, however, utilizes asymmetric source and drain structures (p-i-n design) and is designed to conduct on-state current in only one direction [2, 3]. For an n-channel TFET, band-to-band tunneling (BTBT) generated electrons flow from the P^+ source to the N^+ drain; for a p-channel TFET, BTBT generated holes flow from the N^+ source to the P^+ drain (Fig. 5.1). This constraint

does not limit the design of static logic gates, since pull-up (PU) and pull-down (PD) transistors always flow current in one direction [2]. However, any logic topologies utilizing pass-transistor (PT) or transmission-gate (Tx-gate) require two-way current flow [4], which means that the design of non-static latches and registers, and the access transistors in static random access memory (SRAM), will inevitably require higher transistor counts to perform the computation (necessitating larger layout area).

5.2.2 Forward Bias Diode Current

In addition to the one-way current flow, a TFET's inherent p-i-n structure permits large parasitic diode current (I_S or I_{DIODE}) to flow when the source-to-drain junctionis forward biased [2]. This issue is exacerbated by the use a small bandgap material (*i.e.* Ge) in the source region to maximize TFET I_{ON}, because it reduces the built-in diode potential [5]. In the Ge-source n-TFET, electron injection into the p-type Ge source along the channel comprises the dominant component of forward-bias diode current (Fig. 5.2(a)) which flows independently of the gate bias (Fig. 5.2(b)). The severity of this parasitic current can be observed in Fig. 5.3, which exhibits comparable current magnitudes between BTBT current (I_{BTBT}) and forward-bias diode current. Consequently, I_{DIODE} along with one-way current flow constraint further limits the use of pass-transistor and transmission-gate-based logic styles.

The impact of I_{DIODE} on a logic output can be illustrated by a simple example of a transmission-gate latch (Fig. 5.4(a)) [4]. Assume that initially the output (Q) is low, input (D) high, and clock signal (CLK) low, which would force the output to retain its state until CLK turns on. However, the transient response shows that Q begins to rise from its intended low-state, which is attributed to the top n-TFET discharging node D through I_{DIODE} (Fig. 5.4(b)). Now consider the case when Q is high, D low, and CLK low, a state for which the output should remain high. This time, however, the bottom p-TFET discharges node D through I_{DIODE} disrupting the logic level (Fig. 5.4(b)). In short, the charge leakage associated with I_{DIODE} not only dissipates large standby power, but can also potentially induce logic failures.

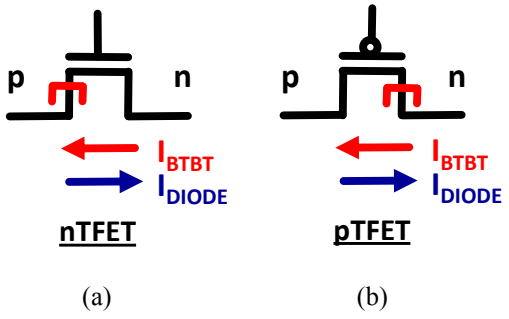


Fig. 5.1 Schematics of the circuit symbols for an (a) n-channel and (b) p-channel TFET. Tunneling junctions are highlighted with ⊓. In addition to the BTBT current, a parasitic forward-bias current can flow in the opposite direction.

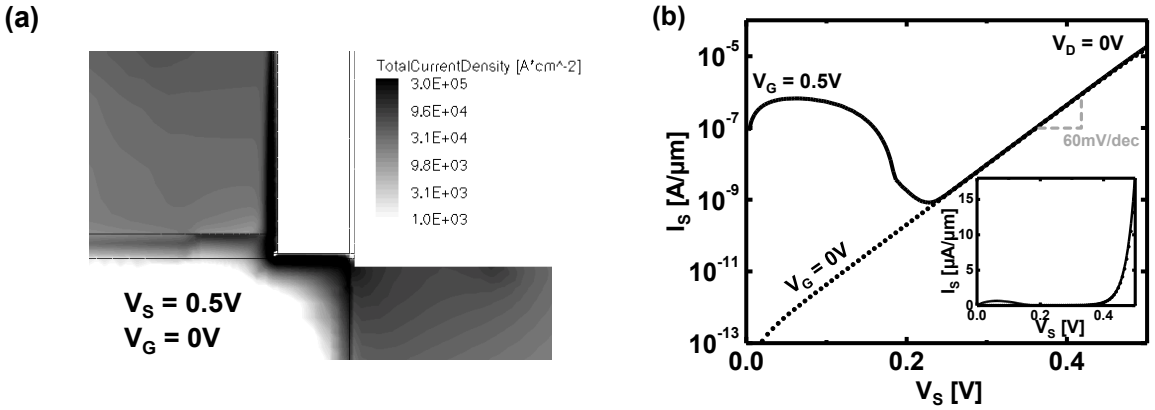


Fig. 5.2. (a) Simulated current density contour plot of a raised Ge-source n-TFET (T_{Ge} = 45 nm) showing electron injection from the N^+ drain into the P^+ Ge to be the predominant source of diode current (surface element). (b) Forward-bias source-drain current (I_S or I_{DIODE}) of a TFET for V_G=0 and 0.5V.

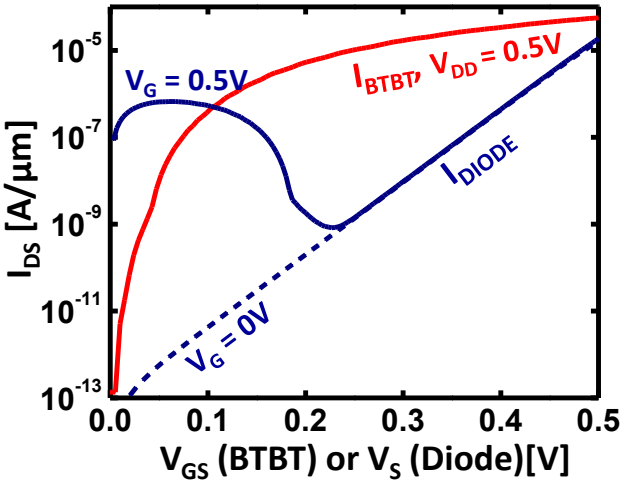


Fig. 5.3. Simulated I_{DS} (I_{BTBT}) *vs.* V_{GS} and I_{DIODE} *vs.* V_S. A large I_{DIODE} flows regardless of gate-bias and the current magnitude is comparable to I_{BTBT}.

In order to mitigate the parasitic forward-bias diode current (dominated by the injection of electrons into P^+ Ge along the surface of the channel, Fig. 5.2(a)), a straightforward method that can be employed is to increase the gate work function in an n-channel TFET (lower work function for p-channel TFET) to increase the potential barrier height seen by the electrons (holes). However, this method comes at the cost of degraded TFET I_{ON}/I_{OFF} (Fig. 5.5) and hence would not be acceptable [6].

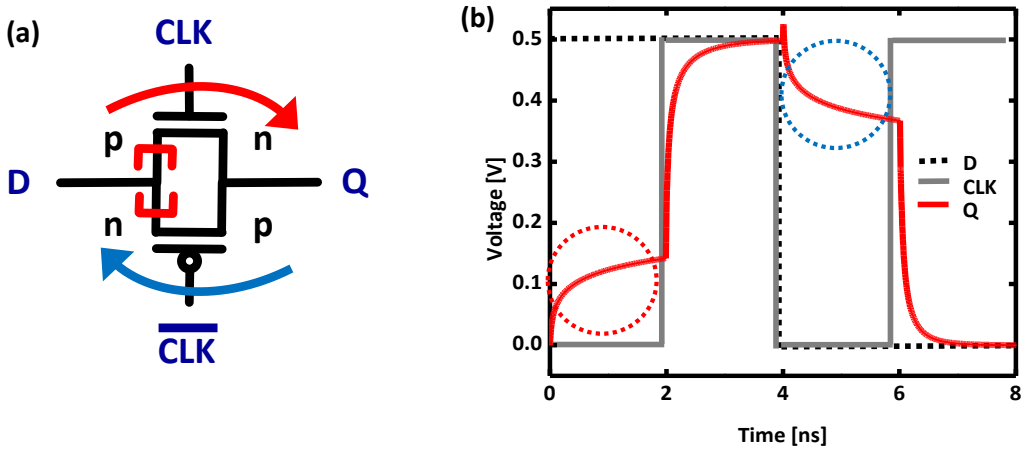


Fig. 5.4. (a) Circuit schematic of the raised Ge-source TFET-based transmission gate. (b) Transient response of the Tx-gate for various input signals, showing that I_{DIODE} can potentially induce logic failures.

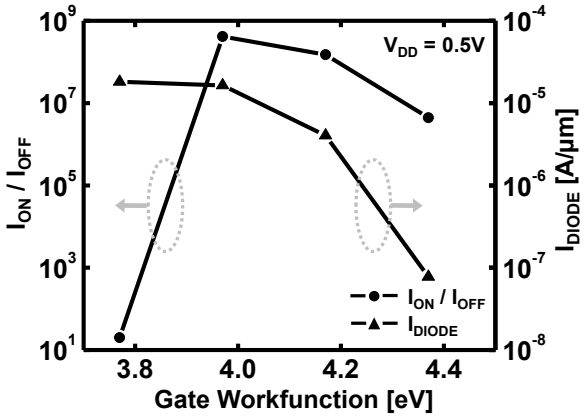
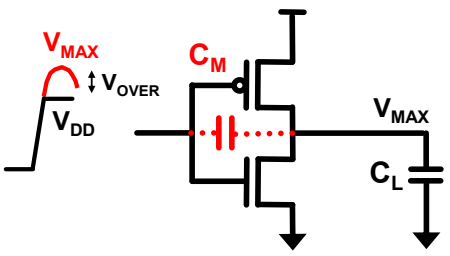


Fig. 5.5 Simulated I_{ON}/I_{OFF} and I_{DIODE} vs. gate work function for a raised Ge-source nTFET. Increasing the gate work function can reduce I_{DIODE}, but comes at the cost of degraded I_{ON}/I_{OFF}.

5.2.3 Large Parasitic Capacitances

In addition to the one-way current flow and forward-bias diode current, large parasitic capacitances associated with a TFET impose another severe limitation in the circuit design. As described in Chapter 4, the presence of a large tunnel resistance induces carrier pinch off towards the source region of the device, and hence gate-to-(N^+)drain capacitance (C_{GD}) of a TFET dominates the total gate capacitance, which is almost always larger than that of a MOSFET [7-9]. In digital logic, the detrimental impact of large C_{GD} is exhibited through Miller capacitance (C_M), which captures the effect of dynamic capacitance being larger than the sum of the static capacitances [8]. In other words, a larger C_{GD} (and hence larger C_M) allows for a capacitive coupling of the input signals to the output and induces voltage overshoot (V_{OVER}) or undershoot (V_{UNDER}) for low-to-high and high-to-low input transitions, respectively. Fig. 5.6 shows analytical formulation of V_{OVER} with respect to C_M and load capacitance, C_L [10].

The severity of C_M on the transient response of a TFET can be investigated from an example of a TFET D-latch (Fig. 5.7). Note that this is merely a static version of the Tx-gate latch shown in Fig 5.4(a) with identical functionality. In order to reduce the simulation times, a Verilog-A Lookup Table has been created based on the DC and AC simulation results of a raised Ge-source TFET (T_{Ge} = 45 nm); the performance of a p-channel device is assumed to be commensurate to an n-channel TFET. The transient response clearly highlights the severity of the voltage over/undershoot (Fig. 5.7(b)) with its magnitude as large as $V_{DD}/2$. These glitches can potentially induce logic failures for subsequent logic stages [10]. The mathematical formulation from Fig. 5.6 suggests that V_{OVER} (and V_{UNDER}) can be mitigated by an increase in the load capacitance, but this method comes at the cost of reduced switching speed.



$$C_L V_{MAX} + C_M (V_{MAX} - V_{DD}) = (C_M + C_L) V_{DD}$$
$$V_{OVER} = V_{MAX} - V_{DD}$$
$$C_L V_{OVER} + C_L V_{DD} + C_M V_{OVER} = (C_M + C_L) V_{DD}$$
$$V_{OVER} (C_M + C_L) = C_M V_{DD}$$
$$\therefore V_{OVER} = \frac{C_M}{C_M + C_L} V_{DD}$$

Fig. 5.6 Schematic illustration and derivation [10] of voltage overshoot (V_{OVER}) with respect to the input voltage (V_{DD}), load capacitance (C_L), and miller capacitance (C_M).

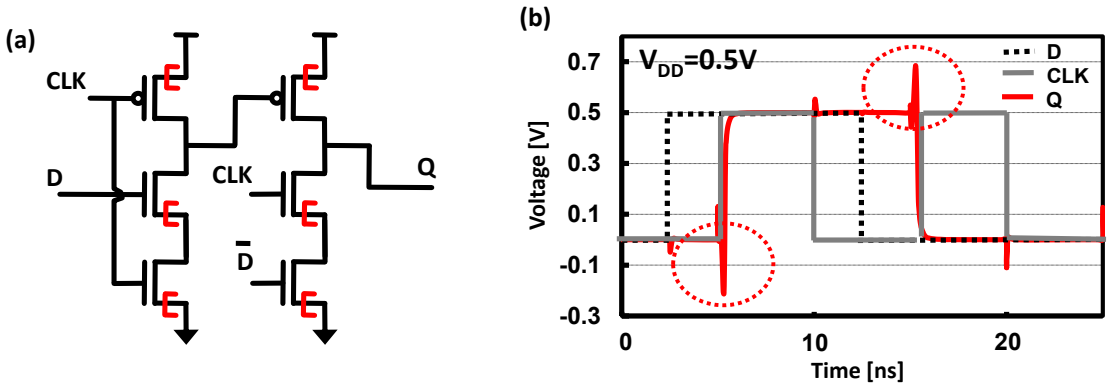


Fig. 5.7. (a) Circuit schematic of the raised Ge-source TFET based static D-latch. (b) Corresponding transient response for various input signals, showing that V_{OVER} and V_{UNDER} can be as large as $V_{DD}/2$.

5.3 nTFET-Based Pass Transistor Logic

The previous section addressed the fundamental challenges associated with TFET-based digital logic design. The applications based on a pass-transistor or transmission-gate was realized to be limited due to one-way current flow and parasitic forward-bias diode current. Furthermore, large C_{GD} inherent to a TFET placed another severe restriction on the design of static gates due to its impact on V_{OVER} and V_{UNDER}. These constraints suggest that the conventional CMOS logic style cannot be directly applied to a TFET circuit design. Hence, this section will propose new logic styles that are applicable for TFETs and demonstrate how some of the aforementioned constraints can be addressed and even be used to for their advantage.

5.3.1 Motivation for nTFET-Based Pass Transistor Logic

The goal of this section is to demonstrate the attractiveness of nTFET-based pass-transistor logic (PTL) for low power design and benchmark its performance to CMOS static gates operated in subthreshold regime. Before discussing the details, it is important to highlight the reasons for investigating n-TFET PTL. The primary motivation for studying the n-TFET-based pass-transistor logic topologies is due to a lack of a complementary Ge-source TFET (p-channel) design with commensurate performance. This is fundamentally due to the large valence-band

energy offset (ΔE_V) between Ge and Si [11], which complicates the leveraging of the lower energy bandgap of Ge to achieve high I_{ON} for a Ge-Si p-channel TFET.

Another motivation for the use of nTFET-based PTL is that the optimized Ge-source n-TFET can achieve much steeper switching behavior than a MOSFET (Fig. 5.8(b)). This implies that it can have significantly lower threshold voltage (V_{TH}) and achieve lower on-state resistance than a MOSFET for a given I_{OFF} specification, at low supply voltage. Fig. 5.9 shows the transient response comparing the discharging and charging characteristics of nTFET *vs*. nMOSFET. It can be seen that the nTFET not only provides for faster discharging characteristics (Fig. 5.9(a)), but also exhibits improved pull-up behavior (Fig.5.9(b)). A fully-depleted (FD) nMOSFET [12], designed to meet ITRS design specifications at the same gate length, was utilized for the comparative study [13].

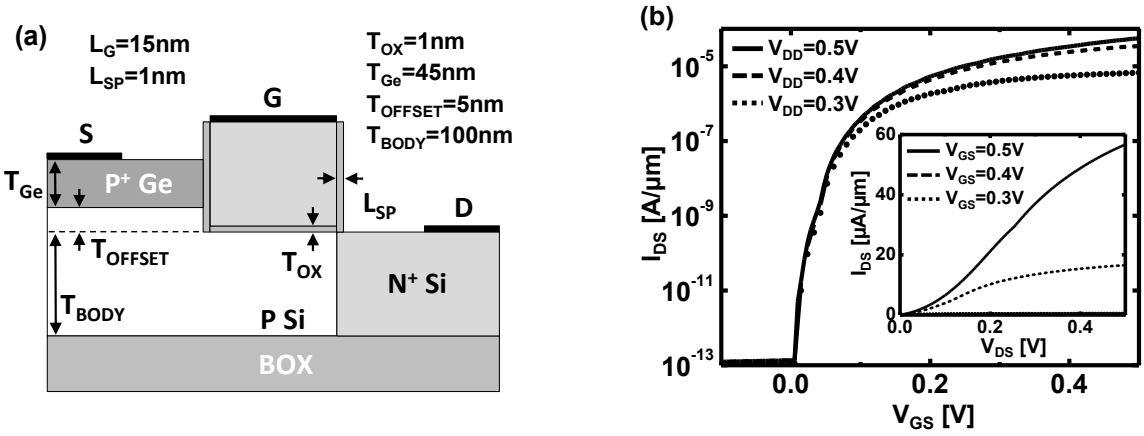


Fig. 5.8. (a) Schematic cross-sectional view of the optimized raised Ge-source nTFET and device parameters. (b) Transfer characteristics (inset: output characteristics) for various V_{DD}.

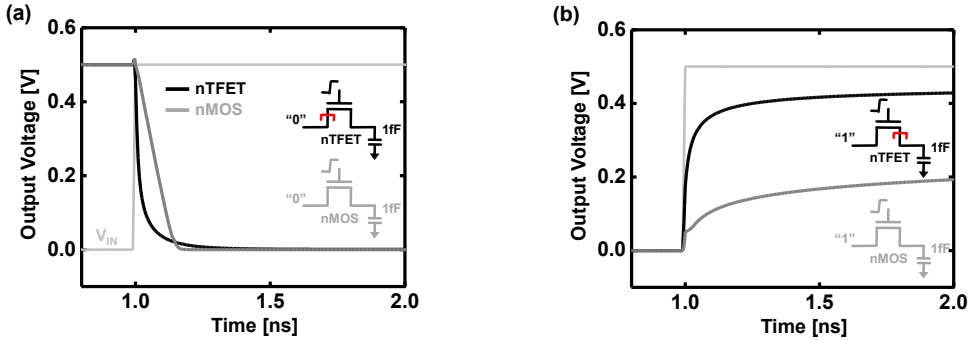


Fig. 5.9. Comparison of the (a) discharging and (b) charging characteristics of the nTFET *vs*. nMOSFET. Inset: symbols and the input signals for the two devices.

5.3.2 nTFET Pass Transistor Logic: AND/NAND and OR/NOR Gates

2-input AND/NAND and OR/NOR gates implemented with n-TFETs are shown in Fig. 5.10(a) and (b), respectively [6]. As compared with nMOSFET implementations (Fig 5.10(c) and (d) for AND/NAND and OR/NOR, respectively) [4], the n-TFET-based designs require one additional transistor for each output in order to address the one-way current flowing constraint.

In order to prevent the forward bias diode current from opposing the intended pull-down or pull-up operation, the number of input signals to the source and drain terminals have been reduced. The inputs of the PU TFETs are tied to V_{DD} (M2 and M3 in Fig. 5.10(a)) and the PD TFETs to ground (M2 and M3 in Fig. 5.10(b)) which prevents undesired charge leakage and supply, respectively. The aforementioned wiring scheme also allows for the leveraging of the I_{DIODE} to assist the intended PU of PD operations. For example, for the NAND gate (Fig. 5.10(a)) with inputs A = 0 and B = 1, transistor M3 pulls up the output node via BTBT current and is assisted by M1 which supplies current to the output node via I_{DIODE}. For the NOR gate (Fig. 5.10(b)) with inputs A=1 and B=0, M3 discharges the output node via BTBT current and is assisted by M1 via I_{DIODE}. The reduction of the number of input signals to the source/drain terminals also mitigates the capacitive feedthrough effects associated with larger Miller capacitance [8].

Although n-TFET offers extremely small V_{TH}, nTFET-based PU voltage is still fundamentally limited by V_{GS}-V_{TH} [4]. Hence, level restoration to V_{DD} is required in-between stages, in order to fully benefit from the extremely low leakage power of the TFET. This is practically achieved with weak pMOSFET PU devices (Fig. 5.11(a)) since the raised Ge-source n-TFET is compatible with CMOS fabrication process. The corresponding transient response of the n-TFET NAND gate for various input signals is shown in Fig. 5.11(b).

The leakage power (P_{LEAK}) and switching energy ($E_{DYNAMIC}$) for n-TFET PTL NAND is assessed by calculating the average power/energy dissipated for all combinations of the input signals, while accounting for the contributions from the weak PMOS level-restorer. The performance is benchmarked against CMOS NAND for various delay constraints (Fig. 5.12). (Static CMOS NAND is chosen for comparison due to its minimal energy dissipation [14].) For delays down to 100 ps, the n-TTFET PTL implementation is more energy efficient.

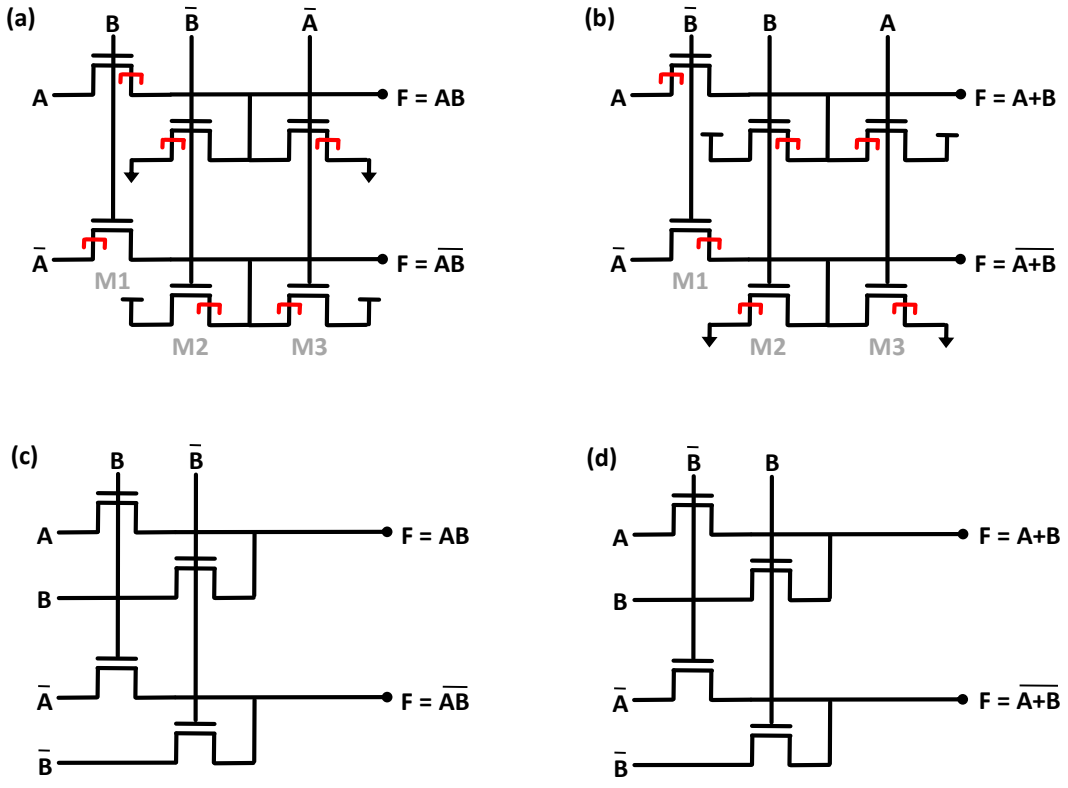


Fig. 5.10. 2-input nTFET PTL schematics for (a) AND/NAND and (b) OR/NOR, and 2-input CMOS PTL schematics for (c) AND/NAND and (d) OR/NOR.

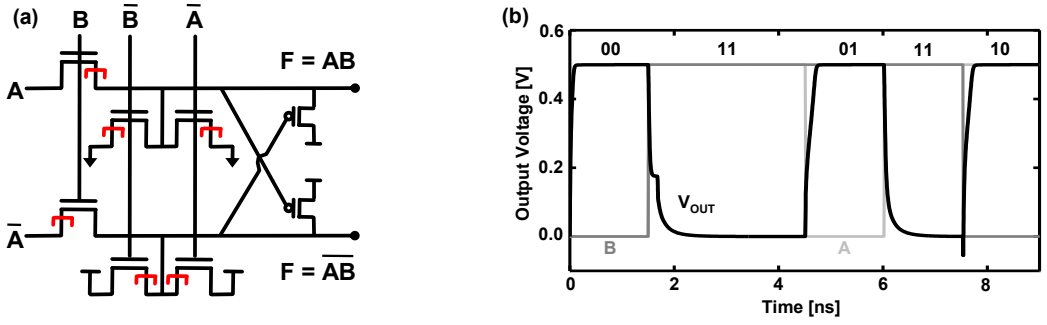


Fig. 5.11. (a) Minimum-sized weak pMOSFET pull-up devices can be used to restore high outputs to V_{DD}. (b) Transient response of the nTFET NAND for various combinations of the input signals A and B. Gate work function = 4eV, $I_{OFF,\ nTFET}$ = 0.1pA/μm, and $I_{OFF,\ PMOS}$ = 10pA/μm.

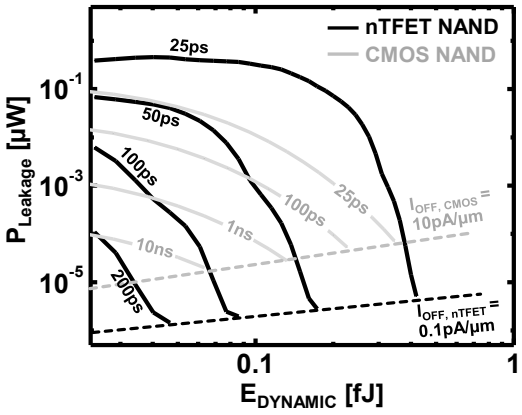


Fig. 5.12. Average $P_{Leakage}$ *vs*. $E_{DYNAMIC}$ for a nTFET NAND gate (with minimum-sized PMOS level restorers as in Fig. 6(a)), compared against a conventional CMOS NAND gate (W_PMOS/W_NMOS = 1.2), for various delay constraints.

5.4 Device-Level Solutions (Future Work)

The previous section demonstrated how nTFET-based pass-transistor logic can be employed as a circuit-level solution to address the fundamental challenges associated with TFETs. Although it was shown to be more energy efficient for low throughput applications, a major drawback with n-TFET PTL topology is due to its requirement for additional transistor count as compared to nMOSFET and CMOS-based logic styles. As a result, this motivates the investigation of device-level design changes necessary to address the circuit-level requirements. The following sections will present improved raised Ge-source TFET designs which can effectively mitigate the constraints in one-way current flow, parasitic forward-bias diode current, and larger parasitic capacitances. A design for a p-channel raised Ge-source TFET will also be presented.

5.4.1 Ultra-Thin Body-Buried Oxide (UTBB) Ge-Source TFET

It has been reported that the introduction of the gate-to-drain underlap region (L_{UN}) reduces the gate-to-drain capacitance in a TFET [7-9]. Due to gate fringing electric field, however, carrier injection from the drain region still results in a large parasitic forward-bias diode current. In order to minimize C_{GD} and I_{DIODE} simultaneously, an insertion of a large potential barrier to the

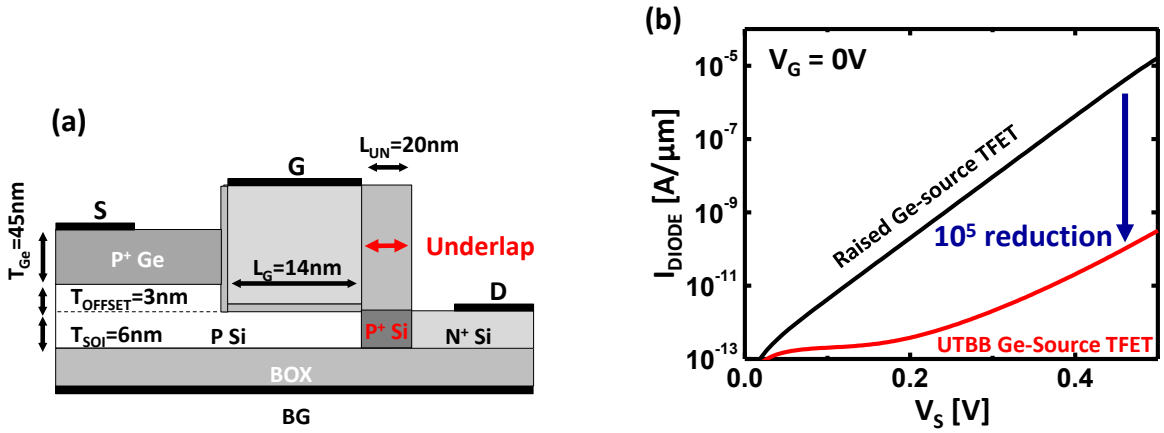


Fig. 5.13. (a) Schematic of the ultra-thin body-box (UTBB) Ge-source TFET. The P^+ Si underlap layer suppresses forward-bias diode current and reduces gate-to-drain capacitance. (b) Comparison of I_{DIODE} for UTBB *vs*. raised Ge-source TFET (Fig. 5.8(a)) showing 5 orders of magnitude reduction.

carriers in the drain is necessary. This can be achieved in a raised Ge-source TFET by an introduction of a heavily doped P region (1×10^{19} cm^{-3}) adjacent to the drain (Fig. 5.13(a)). The new design also utilizes ultra-thin body (T_{SOI} = 6 nm) to effectively suppress any parasitic junction leakage.

The heavily doped P^+ Si underlap region results in 5 orders of magnitude reduction of I_{DIODE} as shown in Fig. 5.13(b) due to larger potential barrier seen by the drain electrons. Although not shown here, C_{GD} is observed to be reduced by 3x. Although I_{ON} degrades by 2x due to larger series resistance imposed by the P^+ Si underlap, the benefit in reduced I_{DIODE} permits UTBB Ge-source TFET to be attractive for the use of transmission-gate latch (Fig. 5.4(a)).

5.4.2. Symmetric Source and Drain Ge-Source TFET

The major restriction in employing CMOS logic topologies for TFET circuit design is attributed to one-way current flow. It has been previously shown that this can only be compensated by increased number of transistor counts, which inevitably necessitates larger layout area. Hence, if area is considered as a performance metric along with the energy-delay product (*i.e.* power × speed × cost), then TFETs may not be attractive for complex logic gates. This motivates the examination of a TFET design which permits current flow in both directions.

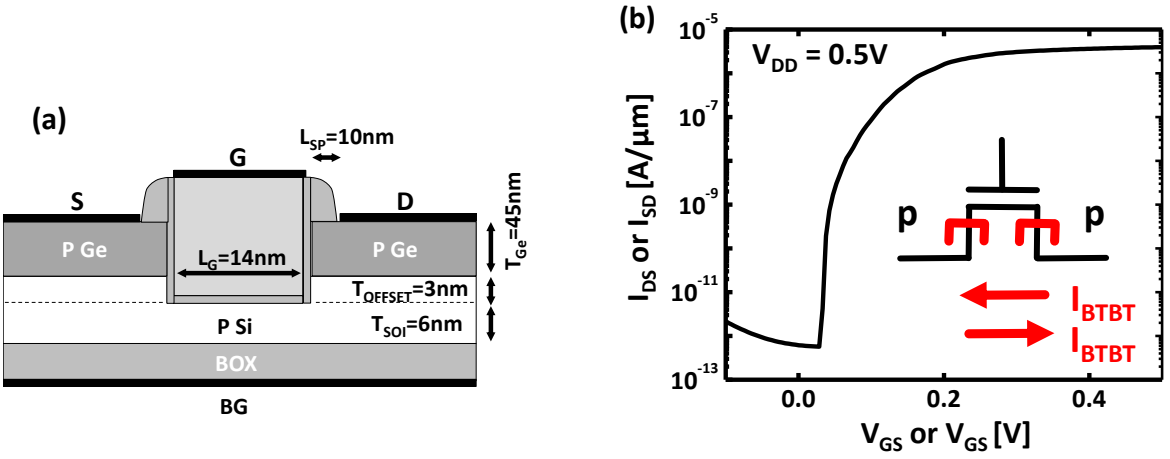


Fig. 5.14. (a) Schematic of the symmetric source-drain Ge-source TFET (S-TFET) and its (b) transfer characteristics demonstrating bi-directional current flow.

The bi-directional current flow can be achieved in a raised Ge-source TFET by introducing symmetric source and drain regions (S-TFET) as shown in Fig. 5.14(a). When the device is in the on-state (V_{GS} = V_{DS} = V_{DD}), P Ge source generates carriers via BTBT process while P Ge drain region along the gate-sidewall and towards the drain contact becomes depleted of holes. BTBT does not occur in the drain since V_{DS} lowers the Fermi level in the quasi-neutral region of the drain so that energy band bending due to V_{GS} is reduced. The BTBT generated carriers flow from the source region towards the drain contact via depleted channel region of the drain along the gate-sidewall dielectric. Since this TFET design is symmetric, the source and drain terminals are interchangeable as in a MOSFET and results in identical transfer characteristics as shown in Fig. 5.14(b). The series resistance inherent to a S-TFET can be optimized by changing the spacer thickness.

5.4.3. Raised Ge-Source P-Channel TFET

So far, the discussion on various designs of Ge-source TFET has focused only on the n-channel device, while simulations requiring a complementary design assumed a p-TFET with commensurate performance to an n-TFET. As addressed previously, the biggest challenge in designing a p-channel Ge-source TFET is attributed to the large valence-band energy offset (ΔE_V) between Ge and Si [11]. The presence of this large potential barrier for holes fundamentally complicates the leveraging of the lower energy bandgap of Ge to achieve high I_{ON} for a Ge-Si p-channel TFET.

In response to these design constraints, a natural choice would be to adopt all-Ge-based pTFET. However, although high I_{ON} can be sustained, degradation in I_{OFF} associated with the thermal leakage of Ge would degrade I_{ON}/I_{OFF} as compared to a Ge-source n-channel TFET [15].

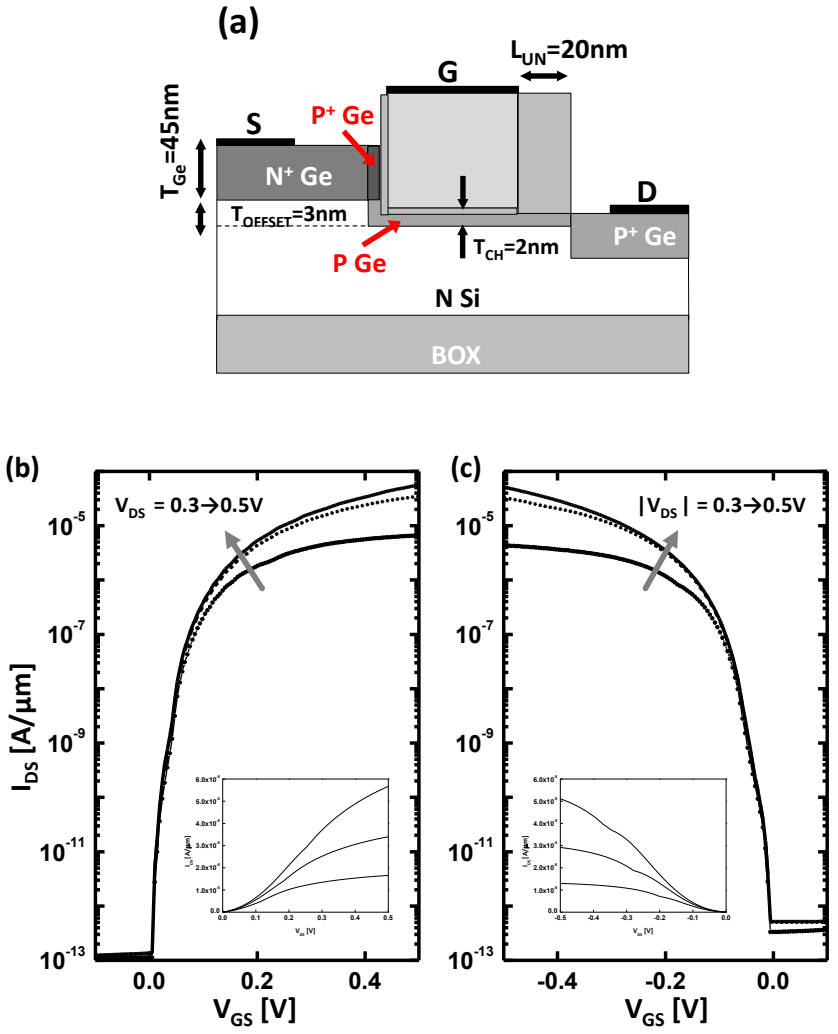


Fig. 5.15. (a) Schematic of the raised Ge-source p-channel TFET. The use of Ge in the active regions of the device allows for a high I_{ON}/I_{OFF}. Comparison of the transfer characteristics of the raised Ge-source (b) n-TFET (Fig. 5.8(a)) and (c) p-TFET showing closely matched performance.

Fig. 5.15(a) shows a raised Ge-source p-TFET structure which employs an epitaxially grown thin Ge channel (T_{CH} = 2 nm) that connects the Ge source and drain regions. Since Ge is used in all active regions of the device, this design avoids the issues associated with ΔE_V seen by the holes. Thin channel in conjunction with a gate-to-drain underlap (20 nm) reduces C_{GD} and I_{DIODE}. The P^+ Ge layer (1×10^{19} cm^{-3}) forms a pn junction with the N^+ Ge-source, which enhances energy band bending in response to a gate bias. Fig 5.15(b) and (c) shows the closely-matched dc characteristics of the n-TFET (from Fig. 5.8(a)) *vs*. p-TFET design.

5.5 Summary

This chapter examined the application of the optimized raised Ge-source TFETs for digital logic. It was highlighted that a direct application of CMOS logic topologies to TFET-based circuit design was challenging due to fundamental limitations in one-way current flow, forward-bias diode current, and larger parasitic capacitances.

Due to its steep switching characteristics, raised Ge-source n-TFET was shown to provide for lower threshold voltage and hence less on-state switching resistance than an nMOSFET, which motivated its application towards nTFET-based pass-transistor logic. The new circuit design addressed the aforementioned design constraints by increasing the number of transistor count and properly routing the input signals to prevent I_{DIODE} from the intended PU or PD action. It was also shown that n-TFET PTL implementation can be more energy efficient for low throughput applications.

The analysis at the circuit level further motivated device-level design changes. UTBB Ge-source TFET was shown to be capable of reducing I_{DIODE} through the insertion of a heavily doped region adjacent to the drain. S-TFET demonstrated bi-directional current flow which made it attractive for the access transistors in SRAM. Lastly, a p-channel TFET design was proposed with closely matching performance to an n-TFET.

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Chapter 6

Conclusions

6.1 Perspectives

Driven by a strong demand for mobile and portable electronics, the chip market will undoubtedly impose "low power" as the key metric for transistor design in the future. Current Complementary-Metal-Oxide-Semiconductor (CMOS) technology has already confronted a major roadblock; today's typical microprocessor operates at around the power density of a nuclear reactor [1]. Because of this, improvements in chip performance have been achieved primarily through parallelism, for recent CMOS technology generations. However, because the total energy consumed per digital operation reaches a minimum when transistors operate in the sub-threshold regime, this approach will become ineffective when the operating voltage (V_{DD}) is reduced below the transistor threshold voltage (V_{TH}).

Significant efforts have been placed to reduce power consumption at all levels of hierarchy in current chip industry. Some of these include employing dynamic substrate biasing to increase the threshold voltage (V_{TH}) of the transistor in the *off*-state (circuit-level technique) [2] and using active parallelism to adapt the operating voltage and clock speed to match the workload (system-level technique) [3]. Despite these higher-level methods to minimize power, it is important to note that the fundamental limit in the overall energy efficiency of a system is still rooted in the Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) operating principle and its immutable physics: an injection of thermally distributed carriers will not allow for switching characteristics better than 60 mV/dec at room temperature [4]. This constraint ultimately defines the lowest energy consumed per digital operation attainable with current MOSFET technology.

In order to address this issue, alternative transistor designs are required. And from power, performance, and cost perspective, any alternative logic switch technology should achieve the following characteristics: steeper switching characteristics than the MOSFET to permit for lower

threshold and supply voltage (V_{DD}) operation (*i.e.* hence attaining the desired *on* to *off* current ratio (I_{ON}/I_{OFF}) at lower voltage), and compatibility with current CMOS fabrication process flow with minimal layout area penalty. To date, numerous steeply switching devices have been proposed and demonstrated but their feasibility and practicality are questionable due to the requirement for either 1) high V_{DD} operation to induce internal voltage loop (*i.e.* Impact-Ionization Metal-Oxide-Semiconductor [5] and Feedback Field Effect Transistor [6]), or 2) fabrication process significantly deviating from CMOS designs with larger layout area penalty (Nano-Electro-Mechanical Relays [7]). On the other hand, a tunnel field effect transistor (TFET) can meet all of the above requirements of a steep switching device and provide for an attractive solution for future low power transistor design.

This thesis has focused on investigating the promise and challenges associated with Germanium(Ge)-source TFET technology for future "greener" electronic devices. The scope of this work ranged from TFET fabrication and analysis, Technology Computer Aided Design (TCAD) based device design optimization, and TFET-based digital logic circuit design. The following section summarizes the contributions of this research in more detail.

6.2 Summary of Work

In Chapter 2, the fundamental concepts of a TFET were introduced. It began by discussing the differences in the device structure and the resulting carrier injection mechanism as compared to a MOSFET. The physics of band-to-band tunneling (BTBT) based on Kane's formulation was summarized, followed by discussion of two BTBT modes (point *vs*. line tunneling) that can be employed for a TFET design. An overview of the BTBT model used in the simulation package (Sentaurus Device) was provided.

Chapter 3 presented a new TFET design – the planar Ge-source TFET. The main difference as compared to a conventional TFET was that the Ge-source structure employs a small bandgap material (Ge) only in the source region of the device with a gate-to-source overlap area for line tunneling, to achieve steep switching behavior and enhance the tunneling current. The experimental results demonstrated a record high I_{ON}/I_{OFF} ratio ($> 10^6$) for low supply voltage ($V_{DD} = 0.5$ V) operation. These results were then used to calibrate Sentaurus Device which was subsequently used for a detailed device design optimization study.

Chapter 4 addressed the performance limitations associated with the planar TFET design and proposed an improved Ge-source TFET structure with an elevated source design. This raised Ge-source TFET was demonstrated to suppress "parasitic" lateral tunneling and achieve steeper switching behavior and higher I_{ON} for an even lower supply voltage operation ($V_{DD} < 0.5$ V). The performance of this new TFET design was then benchmarked against that of CMOS technology and other Ge-source TFET designs, and showed that it can offer lower energy per operation for frequency range up to 1 GHz for sub-0.5 V operation. Device fabrication process based on CMOS gate-last approach and various methods employed to characterize Ge doping concentration were demonstrated. Measurement results were subsequently presented and

discussed.

In Chapter 5, the optimized raised Ge-source TFET was employed to examine its applicability for digital logic. It was highlighted that there were three physical challenges associated with TFETs in logic design: 1) one-way current flow, 2) parasitic forward-bias diode current, and 3) larger parasitic capacitances. In order to mitigate these constraints, a circuit-level solution based on n-TFET Pass Transistor Logic (PTL) was proposed through mixed-mode device simulations, and 2-input complementary AND/NAND and OR/NOR logic gates were designed. The circuit-level constraints and the accompanying device-level design modifications required were discussed.

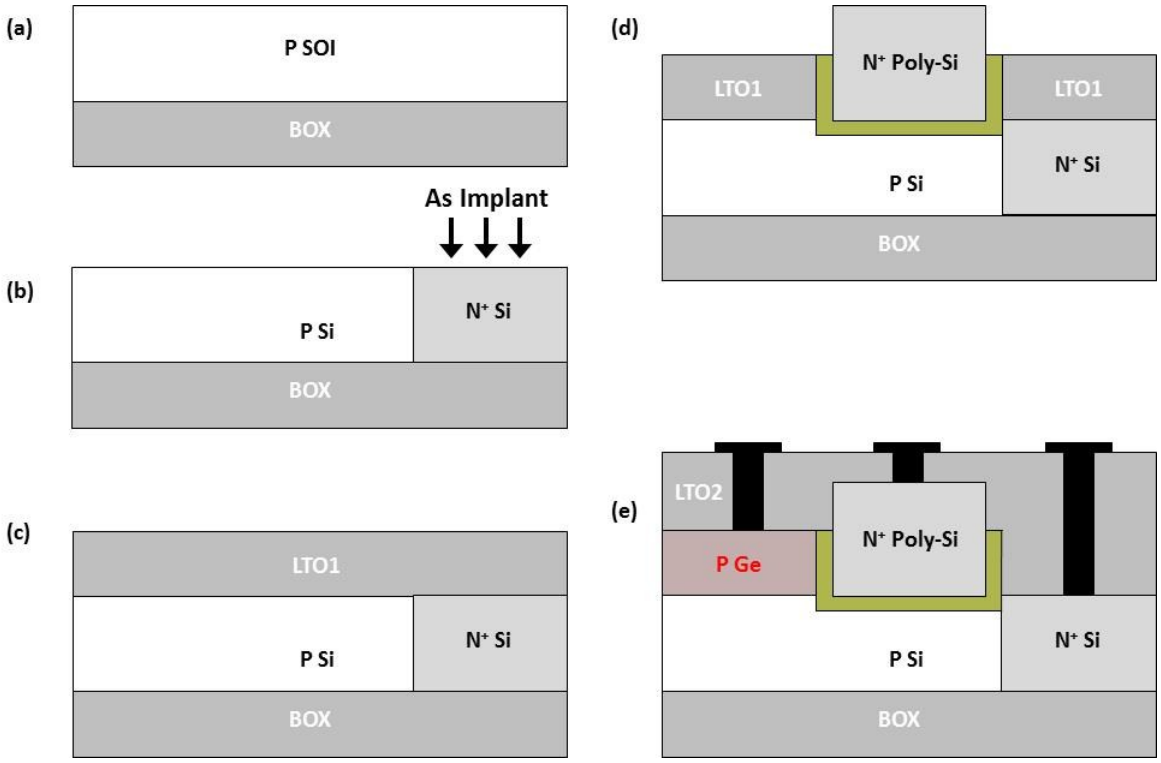

Figure 6.1 Proposed modified process flow of the raised Ge-source n-channel TFET.

6.3 Future Directions

6.3.1 Modified Process Flow for Raised Ge-Source N-Channel TFET

The simulation results presented in Chapter 4 have demonstrated that the raised Ge-source TFET can achieve steeper switching characteristics and larger I_{ON} for an even lower voltage operation as compared to the planar design. Unfortunately, the experimental results were unsatisfactory due to rough Ge surface in contact with Al_2O_3 gate-dielectric, which degraded the gate electrostatics (Fig. 4.14). This was attributed to the non-uniform etch rate associated with grain boundaries of polycrystalline (poly) Ge.

In order to avoid direct etching of poly-Ge, the modified fabrication process for the raised Ge-source TFET should rely on selective Ge deposition after the gate-stack deposition. The proposed process flow is as follows; starting with a silicon-on-insulator (SOI) substrate (Fig. 6.1(a)) and implanting the drain region with As^+ (Fig. 6.1(b)), the substrate is deposited with low-temperature oxide (LTO) hardmask (Fig. 6.1(c)). Then the inverse-gate-mask is used to pattern the gate region (with an over-etch to introduce Si offset region), after which Al_2O_3 gate-dielectric and N^+ poly-Si gate are deposited and patterned (Fig. 6.1(d)). Subsequently, LTO from the source region is etched away followed by selective deposition of poly-Ge (Fig. 6.1(e)). After depositing another LTO capping layer, the contact holes are patterned and deposited with TiN and Al for contact (Fig. 6.1(e)).

The new process flow is expected to result in uniform interface between poly-Ge and gate-sidewall dielectric. This factor accompanied by more aggressive gate-dielectric scaling should provide for maximum electrostatics to induce steeper than 60 mV/dec turn on characteristics and large I_{ON}.

6.3.2 Fabrication of the Symmetric Source and Drain Ge-Source TFET

As addressed in Chapter 5, a major constraint in TFET-based circuit design is associated with one-way current flow [8, 9]. This inevitably entails the use of more transistors to perform a logical function, resulting in larger layout area as compared with CMOS designs. In order to avoid this issue, the symmetric source and drain Ge-source TFET (S-TFET) has been proposed via device simulations (Fig. 5.14). To date, the bi-directional current flow in a TFET has not been discussed. Hence, experimental demonstration of an S-TFET as well as its proper latch operation would be a great leap forward in the TFET community.

S-TFET can be fabricated with only minimal changes to the process flow for the raised Ge-source n-channel TFET. Starting with an SOI substrate (Fig. 6.2(a)), LTO layer is deposited (Fig. 6.2(b)). Then the inverse-gate-mask is used to pattern the gate region (with an over-etch to introduce Si offset region), after which Al_2O_3 gate-dielectric and N^+ poly-Si gate are be deposited and patterned (Fig. 6.2(c)). Subsequently, LTO from the source and drain regions is etched away, followed by selective deposition of poly-Ge (Fig. 6.2(d)). After depositing another

LTO capping layer, the contact holes are patterned and deposited with TiN and Al for contact (Fig. 6.2(d)).

6.3.3 Fabrication of the Raised Ge-Source P-Channel TFET

While this research has focused primarily on Ge-source n-channel TFET, an optimal p-channel design based on Ge and Si needs to be determined and experimentally demonstrated. The challenge lies in the large valence-band energy offset (ΔE_V) between Ge and Si [10], which complicates the leveraging of the lower energy bandgap of Ge to achieve high I_{ON} for a p-TFET. One possible solution was proposed in Chapter 5 which employs an epitaxially grown thin Ge channel that connects the Ge source and drain regions (Fig. 5.15(a)). The processing challenges require further investigation.

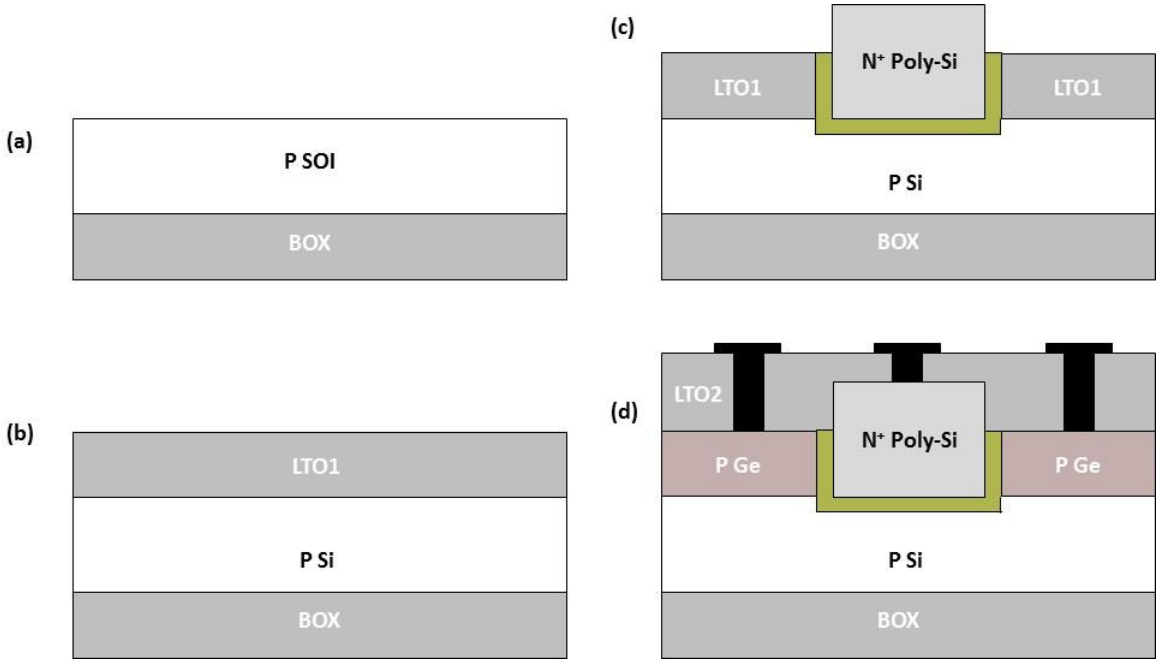

Figure 6.2 Proposed process flow of the symmetric source and drain raised Ge-source TFET.

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