MODULARLY INTEGRATED MEMS TECHNOLOGY

By

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B.S. (Virginia Union University) May 2001
M.S. (University of California, Berkeley) May 2003

A dissertation submitted in partial satisfaction of the
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Committee in Charge
Tsu-Jae King, Chair
Roger T. Howe
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Department of Electrical Engineering and Computer Sciences
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Abstract

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Professor Tsu-Jae King, Chair

Process design, development and integration to fabricate reliable MEMS devices on top of VLSI-CMOS electronics without damaging the underlying circuitry have been investigated throughout this dissertation. Experimental and theoretical results that utilize two "Post-CMOS" integration approaches will be presented.

The first integration approach uses SiGe MEMS technology for the "Post-CMOS" monolithic integration of the MEMS devices with electronics. Interconnects between SiGe MEMS and Al-TiN metallized layers have been characterized and optimized. A thorough study on Boron doping and Ge content effects on the electrical, mechanical, and chemical properties of SiGe MEMS technology has been performed. Two CMOS-compatible micromachining fabrication procedures have been developed for RF and inertial sensing MEMS applications. First, a process flow that uses Ge ashing technique to define nanogaps in SiGe electrostatic MEMS transceivers for wireless communication applications has been demonstrated. Second, a multilayer SiGe MEMS process flow has been implemented for the fabrication of a freely moving disk used to pave the way towards an integrated electrostatically levitated disk sensor system for low loss inertial sensing applications. The sensor system is comprised of a disk-shaped proof-mass that is

to be electrostatically suspended between sense and drive electrodes located above, below, and at the sides of the disk.

The second "Post-CMOS" integration employs the state-of-art "back-end" materials already available in the integrated circuitry to fabricate the MEMS devices. Copper-based MEMS technology is used for the fabrication of low loss RF MEMS switches directly on top of the electronics. A model accounting for multilayer cantilever beam deflection suitable for MEMS devices fabricated with conventional "back-end" materials was derived. Experimental results characterizing stress gradients in copper-based RF MEMS switches will be presented. The effect of Physical Vapor Deposition (PVD), Atomic Layer Deposition (ALD) deposited TaN films, and compressive SiN films on beam deformation have been studied, as well as the effect of annealing on the reliability properties of the RF MEMS switches.

Professor Tsu-Jae King,
Dissertation Committee Chair

To my mother

"Thanks for everything you've poured into my life!"

"I have learnt in life that success should not be defined by the position that someone holds; rather, it should be measured through all the obstacles that one has overcome while trying to succeed"

Booker T. Washington

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Acknowledgements

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- The bottom $Si_{1-x}Ge_x$ layer was deposited at 425°C and 600 mTorr, with GeH_4 flow rate = 70 sccm, SiH_4 flow rate = 105 sccm and BCL_3 flow rate = 12 sccm, σ=-51MPa
- The top $Si_{1-x}Ge_x$ layer was deposited at 410°C and 600 mTorr, with GeH_4 flow rate = 50 sccm, SiH_4 flow rate = 125 sccm and BCL_3 flow rate = 12 sccm, σ=-215MPa

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Chapter 1

Introduction

1.1. Integration of MEMS with Electronics

1.1.1. What are MEMS?

Micro-Electro-Mechanical Systems (MEMS) are micron-scale devices that can sense or manipulate the physical world. MEMS are usually created using micromachining processes (surface or bulk micromachining), which are operations similar to those used to produce integrated circuits (ICs) devices, except that the final MEMS devices are released (free to move) at the end of the fabrication procedure [1.1]-[1.3].

To date, MEMS represent a growing technology with critical applications across diverse fields (optical, electrical, mechanical, biology, chemistry, biomedical…etc). Pressure sensors, accelerometers and angular rate gyroscopes still represent the vast majority of high-volume MEMS production. In the next decade, other MEMS devices such as optical MEMS switches, RF MEMS filters and chemical/biological MEMS sensors are predicted to experience widespread applications [1.4].

1.1.2. The need for a monolithic modularly integrated technology

The decision to merge CMOS and MEMS devices to realize a given product is mainly driven by performance and cost.

On the performance side, co-fabrication of MEMS structures with drive/sense capabilities with control electronics is advantageous to reduce parasitics, device power consumption, noise levels as well as packaging complexities, yielding to improved system performance [1.5]-[1.10]. With MEMS and electronic circuits on separate chips, the parasitic capacitance and resistance of interconnects, bond pads, and bond wires can attenuate the signal and contribute significant noise (**Figure 1.1**). Therefore, fabricating the MEMS devices directly on top of the CMOS metal interconnects will result in a reduction of the parasitics, that will greatly improve the system performance.

On the economic side, an improvement in system performance of the integrated MEMS device would result in an increase in device yield and density, which ultimately translates into a reduction of the chip's cost. Moreover, eliminating wire bonds to interconnect MEMS and ICs could potentially result in reduced packaging complexities which will eventually lead to more reliable systems, and in lower manufacturing cost.

However, in order to achieve high performance, reliable, and modularly integrated MEMS technology, many issues still need to be resolved. Some of these issues have been addressed and investigated in this dissertation with the use of two "Post-CMOS" low temperature MEMS technologies approaches: poly-$Si_{1-x}Ge_x$ and copper-based MEMS technologies.

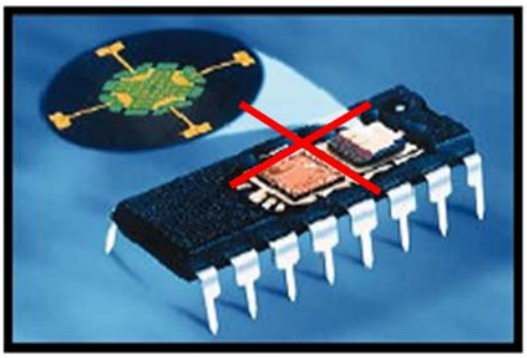


Figure 1.1: An early accelerometer from *Motorola Inc*. showing a MEMS chip placed next to a CMOS chip placed in a ceramic package. Electrical connection is made possible by using metal wires. These wires introduce unwanted parasitics that cause degradation of the system performance [Howe lecture notes, 2005].

1.2. Different modular integration approaches

Modular integration will allow the separate development and optimization of electronics and MEMS processes. There are three main integration strategies that have been presented in the literature: "Pre-CMOS", "Post-CMOS" and the "interleaved approach". A schematic description of these three basic approaches is shown on **Figure1.2**.

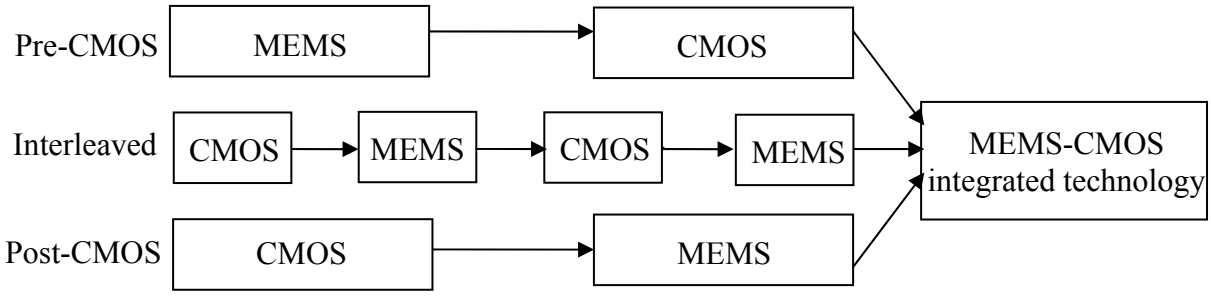


Figure 1.2: Schematic description of the three monolithic integration schemes approaches that could be used to integrate micromachined devices with CMOS electronics [1.5].

The first integration approach is the "Pre-CMOS" scheme that was first demonstrated by *Sandia National Laboratory* through their IMEMS foundry process [1.11]. With the use of surface micromachining process, the IMEMS process utilizes one sacrificial oxide layer and one structural poly-Si layer. High performance MEMS are fabricated in a trench etched in the silicon wafer. The trench is filled with PECVD (Plasma Enhanced Chemical Vapor Deposited) oxides and planarized to reduce the films' surface topography for further processing steps. Then, the MEMS devices are annealed to release their residual stress. After the annealing procedure, a passivation step of the MEMS is needed so that subsequent CMOS processes are MEMS compatible (in this case LPCVD nitride was used as the passivation layer). Next, a conventional CMOS fabrication process is performed followed by passivation of the CMOS devices. Finally, a trench is opened and the MEMS structures are released using hydrofluoric acid. A cross section of the integrated MEMS is shown in **Figure 1.3**.

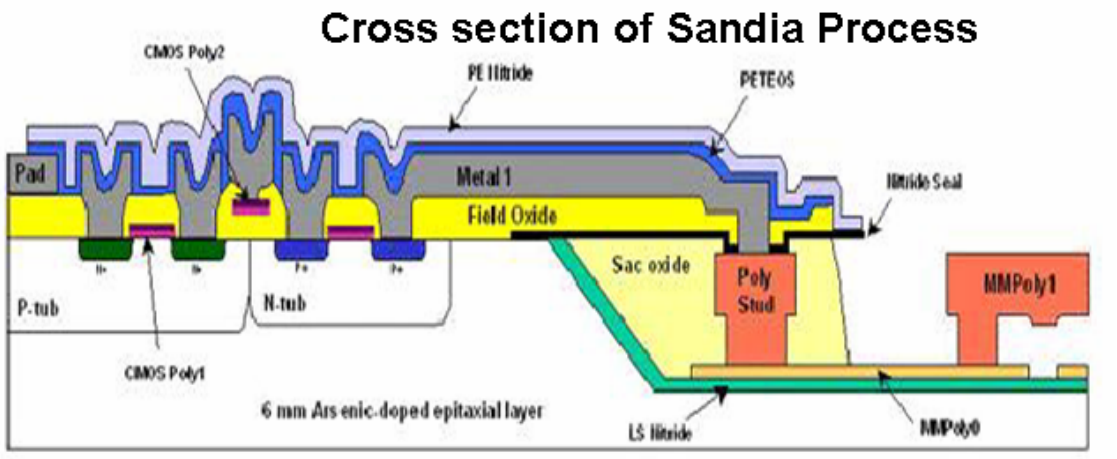
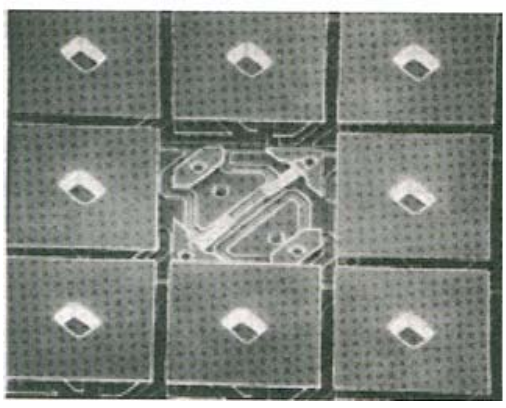


Figure 1.3: Cross section of the *Sandia National Laboratory* IMEMS foundry process where MEMS are fabricated inside a trench before the definition of the electronics [1.11].

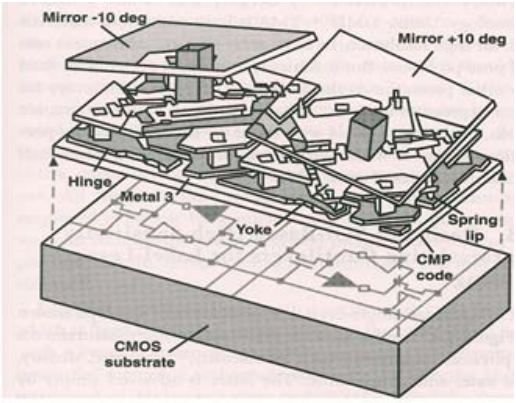
The major hurdles of the "Pre-CMOS" approach include the MEMS topography which can compromise subsequent state-of-the art CMOS lithography steps, larger die areas due to the fact that the MEMS and CMOS devices cannot be easily stacked and the fact that that integrated circuits foundries are usually not inclined to accept pre-processed wafers because of material compatibility and contamination issues.

The second integration approach is the "Post-CMOS" scheme which was successfully demonstrated by *Texas Instruments Inc.* through the DMD (Digital Micro-Mirror Device), which uses an electrostatically controlled mirror to modulate light digitally, thus producing a stable high quality image on a screen (**Figure 1.4a**) [1.12]. Each mirror corresponds to a single pixel programmed by an underlying SRAM cell (**Figure 1.4b**). Post-CMOS integration process is made possible through the usage of low temperature metal films (aluminum) as the structural layer and polymers (photoresist) as the sacrificial material.

The main hurdle when using the "Post-CMOS" integration approach is the temperature compatibility of both processes, so that a low temperature MEMS process is necessary to avoid damaging the CMOS interconnects.



(a)

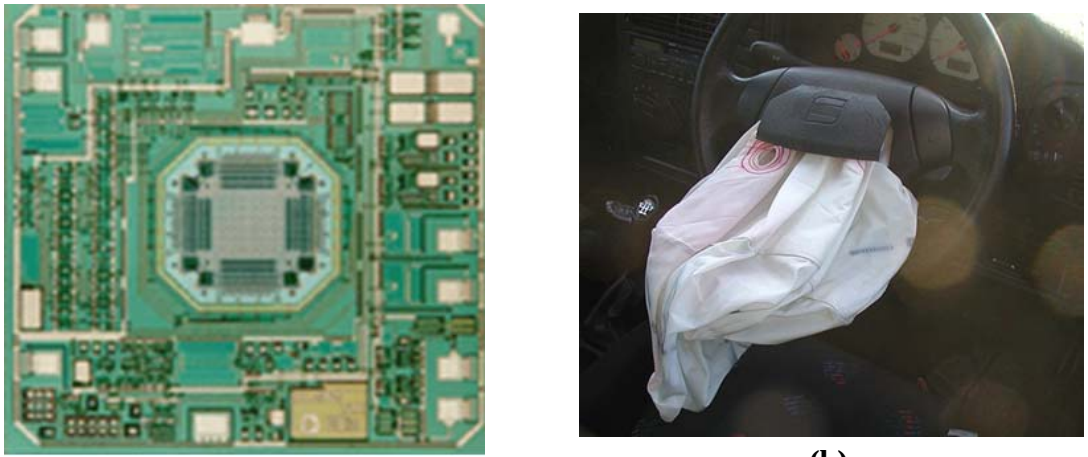


(b)

Figure 1.4: Plan and cross section view of the DMD (Digital Micro-Mirror) device developed by *Texas Instruments Inc.* Here, MEMS are fabricated using Al films after the CMOS electronics [1.12].

In this work, two "Post-CMOS" integrations approaches have been studied with the use of SiGe MEMS technology and copper-based MEMS technology.

The third integration approach is the interleaved approach. This approach has been successfully demonstrated by *Analog Devices Inc.* in their 50G accelerometer (ADLX 50) technology which was the first commercially proven MEMS-CMOS integrated process [1.13]. While the main advantage of an interleaved integration process approach is the potential better control of both the MEMS and the CMOS process, the major drawback is the often need for a compromise of the MEMS and/or CMOS steps to achieve the necessary performances. A figure showing a complete integrated ADLX 50 chip is shown in **Figure 1.5**.



(a) **(b)**

Figure 1.5: **(a)** The *Analog Devices Inc.* ADLX-202 of about 5mm^2 holding in the middle a MEMS accelerometer around which are electronic sense and calibration circuitry. Hundreds of such devices have been sold. **(b)** Airbag of car that crashes into the back of a stopped Mercedes. Within 0.3 seconds after the deceleration, the air bag is empty, so that driver does not get hurt [1.13].

1.3. Poly SiGe, a low temperature mechanical material

1.3.1. Summary of SiGe research for VLSI-CMOS applications

Very recently, there has been a growing body of knowledge on silicon germanium technology within the integrated circuit community for multiple applications across the electronics manufacturing industry. While silicon germanium films have been intensively used for hetero-junction bipolar transistors, recent studies have shown silicon germanium as a good candidate for the replacement of poly-silicon gate technology in CMOS applications. Gate work function engineering can be performed by adjusting the Ge content in the films so that a complementary CMOS technology can still be implemented on the same substrate [1.14]-[1.15]. Strained silicon germanium channels are also being studied for the increase of electron mobility in CMOS technology [1.16]-[1.17]. Finally, silicon germanium can also be used in elevated source-drain CMOS technology for the reduction of the series resistance, thus increasing the transistor ON-current [1.18]-[1.19].

Taking advantage of such an extensive body of knowledge and experience on silicon germanium technology for VLSI-CMOS applications, MEMS researchers could build-up their wisdom from the integrated circuit community in order to implement this semiconductor alloy for micromachining applications.

1.3.2. Summary of recent SiGe MEMS research

An extensive overview of the research in SiGe MEMS technology has been recently been published by *S. Sedky* [1.20]. Two groups have been leading research in this field. Here at the University of California-Berkeley, the initial work of silicon germanium as a potential material for surface micromachining applications was performed by *A. Franke et al.* who successfully fabricated low frequency comb-drives devices on top of 0.25 μm CMOS circuitry (with the electronics fully operational after the MEMS fabrication process) [1.21]-[1.22]. During the same period of time, *S. Sedky et al.* working at the Interuniversity MicroElectronics Center (IMEC) in Leuven (Belgium), also investigated the structural and mechanical properties of polycrystalline silicon germanium for micromachining applications [1.23]-[1.24].

In more recent years, there have been further investigations of the mechanical, electrical and chemical properties of poly-$Si_{1-x}Ge_x$ MEMS technology. Polycrystalline p+ Ge films was suggested to be a convenient sacrificial layer with p+$Si_{1-x}Ge_x$ as the structural layer since it can be selectively etched with peroxide at a temperature of 90ºC [1.25]-[1.26], and an etching model was developed to optimize the Ge content in the films [1.27]. Other wet chemical etchants have been reported to release p+$Si_{1-x}Ge_x$ micromachined films [1.28]-[1.29].

Phosphine doped poly-$Si_{1-x}Ge_x$ films have been investigated for micromachining applications [1.30]. Two main findings came out of that study. Firstly, similar to phosphorus in poly-Si, phosphorus atoms retard the deposition of poly $Si_{1-x}Ge_x$ films. The slower deposition rate of the n-type $Si_{1-x}Ge_x$ films would result in an increase in the cost of the technology. Secondly, it was found that the resistivity of the n-type $Si_{1-x}Ge_x$ films

was unacceptably high for most MEMS applications. Therefore, a high temperature annealing process (> 450ºC) was often necessary to activate the dopants, thus reducing the films' resistivity [1.22],[1.30].

More lately, poly-$Si_{1-x}Ge_x$ was reported to be a high Q mechanical material for both low and high frequency applications. Q value above 30,000 has been achieved for low frequency filtering applications (f=15kHz) [1.31] as well Q value ~ 30,000 for high frequency wireless communications (f=30MHz) [1.32].

Moreover, new techniques that include multilayer approach [1.33] and laser excimer annealing crystallization [1.6],[1.34]-[1.36] to reduce the stress and strain gradient of $Si_{1-x}Ge_x$ films have been reported. All the studies performed in the SiGe MEMS Berkeley group use a Low Pressure Chemical Vapor Deposition (LPCVD) process to form the polycrystalline $Si_{1-x}Ge_x$ films. LPCVD is a well understood technique that yields films with properties that are relatively insensitive to the process tool [1.37]-[1.38]. Also LPCVD is an extremely conformal process, which is important for the reliable fabrication of simple MEMS structures such as beam anchors.

Researchers at IMEC have intensively investigated Plasma Enhanced Chemical Vapor Deposition (PECVD) polycrystalline $Si_{1-x}Ge_x$ films for MEMS applications. The main advantage of using a PECVD deposition process as compared to a LPCVD deposition process is a tremendous increase in deposition rate that greatly affects the cost of the technology. The PECVD poly-$Si_{1-x}Ge_x$ films have been demonstrated to have properties comparable to LPCVD poly-$Si_{1-x}Ge_x$ films qualities [1.39]-[1.42]. Novel processes that include metal induced crystallization [1.41] and multilayer approach to reduce the strain gradient of PECVD poly-$Si_{1-x}Ge_x$ films have been reported [1.42].

Micro gyroscopes inertial sensor devices have been successfully fabricated on top of standard 0.35µm Al-CMOS process using low strain gradient multilayered PECVD Si_xGe_{1-x} structural films [1.43].

1.3.3. Properties of poly-$Si_{1-x}Ge_x$

The mechanical properties of silicon germanium are comparable to those of polycrystalline silicon [1.44]-[1.45], and the films can be deposited in a conformal process (**Figure 1.6**) using low pressure chemical vapor deposition or plasma enhanced chemical vapor deposition [1.43]. **Table 1.1** compares the mechanical properties of silicon to those of germanium.

Certainly the most exciting characteristic of poly-$Si_{1-x}Ge_x$ film, which makes this film a great candidate for MEMS micromachining integrated technology, is its low thermal budget that allows modular integration of MEMS with electronics by relaxing the high processing temperature required when poly-silicon films are used as the MEMS structural layers.

From **Table 1.1**, it is important to note that the density of poly-germanium film is almost twice that of poly-silicon, making it attractive for inertial sensing applications where a large mass is crucial to provide a large momentum for the achievement of high accuracy and precision in linear or angular acceleration measurements. Another valuable property of interest for MEMS applications is the smaller band gap of germanium, which yields to its low intrinsic resistivity compared to poly-silicon films.

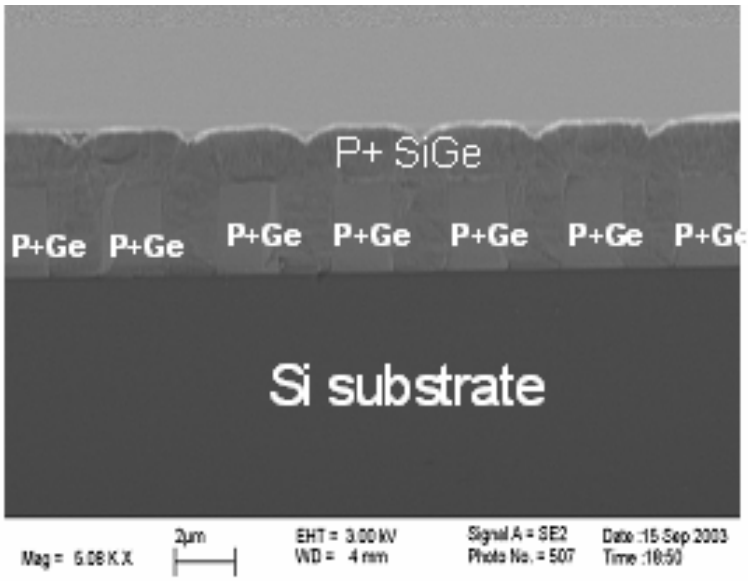


Figure 1.6: SEM showing conformal deposition of p+ Ge sacrificial films on top of p+ $Si_{1-x}Ge_x$ films. After complete fabrication of the MEMS devices, the p+ Ge films are often released using H_2O_2, which does not attack $Si_{1-x}Ge_x$ ($x<0.65$).

Table 1.1: Mechanical properties of poly-Si compared to those of poly-Ge [1.46]-[1.47].

	Poly Si	**Poly Ge**
Density (g/cm^3)	2.32	5.33
Young modulus (GPA)	170	130
Melting point (^oC)	1412	937
Thermal Conductivity $W(cm\ ^oK)^{-1}$	1.5	0.6
Lattice constant	5.4307	5.6575
Coef. of thermal expansion $(^oK)^{-1}$	$2.5x10^{-6}$	$5.7x10^{-6}$
Dielectric constant	11.7	16
Bandgap at 300^oK (eV)	1.12	0.66
Electron mobility (cm^2/Vs)	1350	3900
Hole mobility (cm^2/Vs)	480	1900
Intrinsic resistivity (Ω-cm)	$2.3x10^5$	47
Quality Factor	$45\text{-}80{,}000_{n+poly}$	$30{,}000_{n+\ poly}$

1.3.4. Deposition of poly-$Si_{1-x}Ge_x$

$Si_{1-x}Ge_x$ films are deposited in a conventional LPCVD reactor using germane (GeH_4) as the germanium source gas, in addition to silane (SiH_4) or disilane (Si_2H_6) as the silicon source gas, and phosphine (PH_3), diborane (B_2H_6) or boron-trichoride (BCL_3) [1.48] as the *in-situ* doping gas sources. The alloy composition during film deposition is dependent on several parameters: the deposition temperature, the gas partial pressure and the gas flow ratio. If the films are deposited on oxides, a very thin (<10nm thick) amorphous-Si seed layer is often needed to reduce the incubation time, thus allowing easy nucleation of the poly- $Si_{1-x}Ge_x$ films on SiO_2.

1.3.5. Etching of poly-$Si_{1-x}Ge_x$

The wet etching properties of polycrystalline boron doped silicon germanium and germanium films have been characterized by *J. Heck* for MEMS applications [1.25]. It was found that germanium films are easily etched in a 90°C heated solution of peroxide (H_2O_2), thus can be used as sacrificial material with p+ $Si_{0.4}Ge_{0.6}$ as structural films. **Table 1.2** summarizes the main findings of this work. Other wet chemical etchants have been reported in [1.26].

Table 1.2: Table showing etching rate/chemistries of poly-Ge, p+ poly-$Si_{0.2}Ge_{0.8}$, p+ poly-$Si_{0.4}Ge_{0.6}$, p+ poly-Si and annealed Phospho-silicate glass (etch rates are in μm/min) [1.25].

	HF	RCA, SC1	H_2O_2	Cl_2/HBr Plasma
Poly-Ge	~0	3.0	0.4	0.41
Poly-$Si_{0.2}Ge_{0.8}$	~0	0.75	0.08	0.37
Poly-$Si_{0.4}Ge_{0.6}$	~0	0.06	~0	0.31
Poly-Si	~0	~0	~0	0.16
Annealed PSG	3.6	~0	~0	~0

1.4. Dissertation overview

The monolithic integration of MEMS with CMOS remains an active research area that is crucial for the large scale production of high performance, high yield and low cost MEMS devices. It is important to mention that the right integration approach is largely dependent on a specific MEMS application.

This dissertation has investigated two "Post-CMOS" modular integration approaches:

1. Boron doped poly-$Si_{1-x}Ge_x$ MEMS films for high performance MEMS applications.
2. Copper-based MEMS technology for low loss RF MEMS applications.

Chapter 2: In order to attain a robust modular integration using SiGe MEMS technology, the poly-$Si_{1-x}Ge_x$ micromachined films need to be deposited directly on top of the CMOS metalized lines to reduce parasitic capacitances and resistances. For this to be possible, the contact resistance between $Si_{1-x}Ge_x$ films and Al-CMOS interconnects needs to be as low as possible *i.e.* comparable to that achieved between metal and poly silicon in modern integrated circuits ($< 10^{-6}$ Ω-cm^2). This chapter reports experimental results of contacts study between p+ poly-$Si_{1-x}Ge_x$ films and aluminum interconnects when the poly-$Si_{1-x}Ge_x$ MEMS devices are fabricated directly on top of the Al-CMOS circuitry lines. Process development and optimization have been intensively performed to reduce the contact resistivity to the desired minimal value (~10^{-7} Ω-cm^2) [1.49]-[1.51].

Chapter 3: In order to achieve a high performance integration technology scheme of the poly-$Si_{1-x}Ge_x$ micromachined devices, the $Si_{1-x}Ge_x$ films need to be heavily doped with boron to reduce the films resistivity as well as increase the films deposition rate [1.20]. In this chapter, a thorough study on the effects of boron doping and germanium content on the properties of p+ poly-$Si_{1-x}Ge_x$ MEMS films has been performed. Experimental results will be presented as they pertain to the effects of boron concentration on the chemical, electrical, and mechanical properties of p+ polycrystalline germanium (poly-Ge) film used as sacrificial layer and p+ polycrystalline silicon germanium (poly-$Si_{1-x}Ge_x$) film used as structural layer [1.52]. The ultimate goal of this study is to pave the way for the realization of a robust and reliable SiGe MEMS technology, by providing a better understanding of the film property dependence on boron doping and Ge content.

Chapter 4: After understanding the effects of Ge and B concentrations on the mechanical, electrical and chemical properties of SiGe MEMS, we can go ahead and fabricate functioning MEMS devices using SiGe MEMS technology. This chapter presents experimental results of two MEMS systems fabricated using p+ $Si_{1-x}Ge_x$ MEMS technology. First, results of a short loop fabrication procedure that used Ge ashing technique to fabricate reliable RF MEMS filters for wireless communication applications are presented [1.53]-[1.55]. Second, surface micromachining results of a fabricated poly-$Si_{1-x}Ge_x$ free moving disk used to pave the way towards an integrated electrostatically levitated disk sensor system for low loss inertial sensing applications are reported [1.56].

Chapter 5: The unknown reliability of many MEMS devices limits their incorporation into commercial products. The long-term stability of these devices can only be ensured with greater knowledge of the basic material properties and failure mechanisms of the materials employed in MEMS designs. In this chapter, reliability issues of MEMS structures as they pertain to the intrinsic stress gradient of MEMS switches used in low loss RF MEMS applications have been addressed [1.57]. An analytic model that predicts the deflection of RF MEMS switches fabricated using the state-of-the art copper-based "back-end" technology has been generated. The model matches the experimental data within 20% and could be used for design and process optimization in order to attain a low loss modularly integrated MEMS technology. Moreover, experimental evidence that provides a better understanding of the copper stress relaxation behavior is presented; this turns out to be essential for designing MEMS devices tolerant to high temperature packaging process.

Chapter 6: This chapter summarizes the main findings of this work as well as provides future directions for the modular integration MEMS field that utilizes p+$Si_{1-x}Ge_x$ and copper-based MEMS technologies. A thorough study on the "long-term stability" of p+ $Si_{1-x}Ge_x$ MEMS devices (switches, resonators, gyroscopes…etc) remains necessary in order bring $Si_{1-x}Ge_x$ MEMS devices into high volume production as well as the development of a low temperature CMOS-compatible packaging technology that is needed for the vacuum encapsulation of many integrated MEMS systems.

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Chapter 2

Low Contact Resistance $Si_{1-x}Ge_x$ MEMS Technology

2.1. Motivation

Depending on the application, it is often desirable to fabricate the MEMS structures directly on top of the CMOS circuitry, in order to achieve a high performance "Post-CMOS" MEMS integrated technology. Direct deposition of micromachined structures onto metallized films will result in a reduction of the parasitics associated with the MEMS to CMOS routing [2.1]-[2.3].

Figure 2.1 presents a cross-sectional view of a "Post-CMOS" integrated technology of micromechanical resonators with electronics. The poly-SiGeØ layer is deposited directly on top of the CMOS interlayer dielectric, through which contact openings have been formed. Any parasitic resistance will cause degradation of the signal that needs to be amplified by the CMOS circuitry and transferred through the sense-drive electrodes [2.4]-[2.5].

Since the MEMS micromachined structures are deposited directly on top of the ASIC circuitry, the interconnect resistance between the MEMS and routing metal lines needs to be low in order to minimize signal losses. Ideally, the specific contact resistivity (ρ_c) should be comparable to that achieved between metal and poly silicon in modern integrated circuits ($< 10^{-6}\ \Omega\text{-cm}^2$) [2.6]-[2.7].

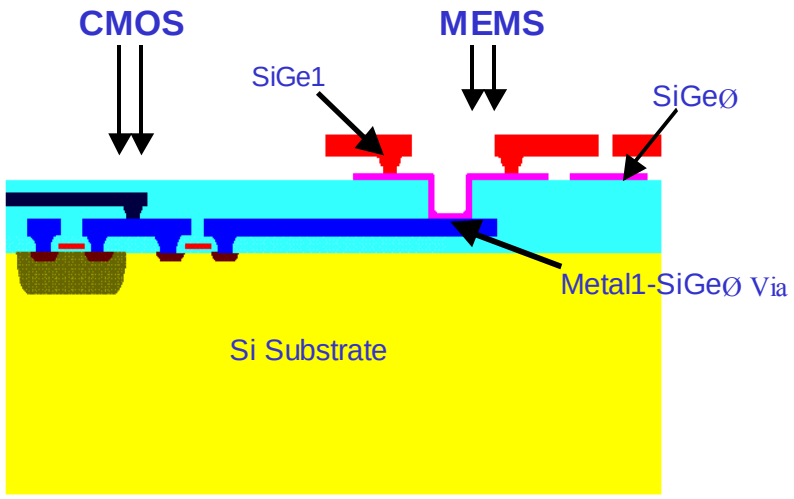


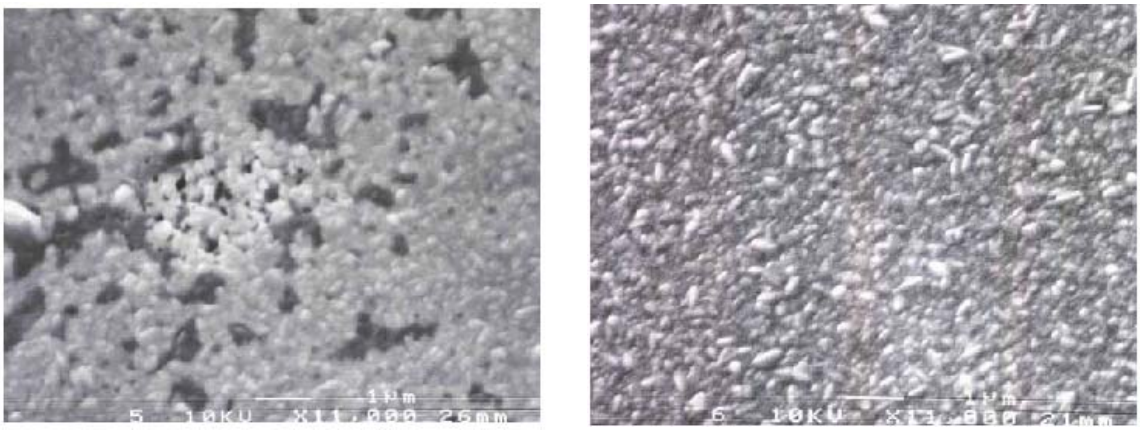
Figure 2.1: Schematic cross-section of modularly integrated SiGe MEMS technology. The "SiGe0" layer is used for routing of electrical signals between the MEMS and electronics.

2.2. Fabrication process flow

2.2.1. Test Structures

A new mask set that included Kelvin test structures of different contact dimensions was designed for the purpose of this study. These Kelvin structures were used to determine the specific contact resistivity of p+$Si_{1-x}Ge_x$ films deposited onto Al-Si(2%)-

TiN films [2.8]-[2.9]. Contact areas ranged between $2\mu m^2$ and $20\mu m^2$. Thermally oxidized (100) Si wafers were used as the starting material, to electrically isolate the fabricated structures from the substrate. Using a Novellus m2i sputtering tool, a 0.5μm layer of Al-Si(2%) was sputtered onto the thermal SiO_2. It was previously shown that aluminum segregates in the germanium films to form pinholes in the contact regions (**Figure 2.2**) [2.10]. In order to remedy this problem, a thin barrier layer of TiN (50nm) was sputtered on top of Al-Si(2%) to prevent the diffusion of p+ poly $Si_{1-x}Ge_x$ into the Al-Si(2%).



(a) **(b)**

Figure 2.2: **(a)** Poly $Si_{1-x}Ge_x$ on Al showing pinholes and **(b)** on Al with TiN (no pinholes).

The metal stack was then patterned using conventional lithography and reactive-ion-etch (Cl_2 based chemistry) processes (**Figure 2.3b**). Afterwards, a 0.4μm-thick interlayer dielectric of low temperature oxide (LTO) was deposited by LPCVD at 400ºC. This temperature ensures that the underlying metallization remains intact. Contact holes were opened in the oxide layer using conventional lithography and dry etching process (CF_4 chemistry), creating straight side-walls (**Figure 2.3c**).

2.2.2. Cleaning issues for metallized wafers

Since Piranha easily attacks aluminum, it is not possible to use standard Piranha-based cleaning techniques to pre-clean the wafers for the removal of contaminant organics prior to poly-$Si_{1-x}Ge_x$ deposition. Various pre-cleaning treatments were designed and modified during the course of this study to improve the contact interface. After patterning and etching of contact holes, the wafers were dipped in a heated solution of PRS3000 for 15 minutes to strip the light-sensitive layer of photoresist. The wafers were then precleaned with a diluted solution of hydrofluoric acid to remove the native oxides for two to five minutes.

2.2.3. Deposition of p+ poly $Si_{1-x}Ge_x$ films

Boron i*n-situ* doped $Si_{1-x}Ge_x$ alloys were deposited in a LPCVD furnace at 400°C and 450°C using SiH_4 and G_eH_4 precursors. As the dopant atoms naturally occupy substitutional sites during a LPCVD process, there was no need for a high temperature annealing process to activate the dopants. The $Si_{1-x}Ge_x$ alloys were patterned and etched using a standard poly-Si etch process using Cl_2 and HBr chemistries (**Figure 2.3d**). A reasonable etch selectivity against silicon dioxide was observed. A final masking step was used to pattern the interlayer oxide to allow for direct probing of metal pads (**Figure 2.3e-f**).

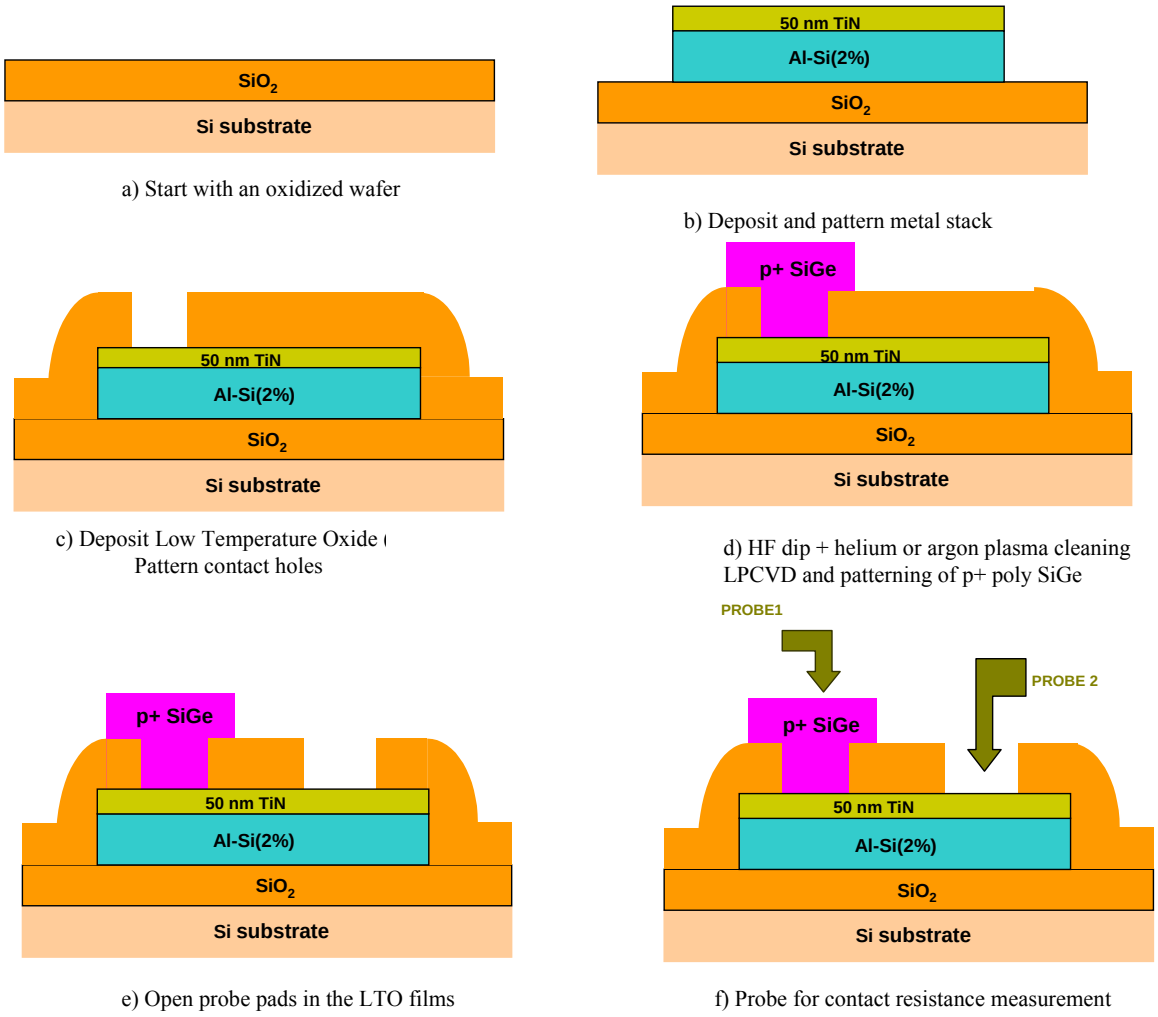


Figure 2.3: Fabrication process flow for the Kelvin test structure used to measure contact resistance.

2.3. Characterization of $Si_{1-x}Ge_x$ films

In an effort to integrate $Si_{1-x}Ge_x$ MEMS micromachined structures with electronics, a full experiment was conducted to determine the effect of deposition temperature, deposition pressure and Ge content on the mechanical properties of p+ poly $Si_{1-x}Ge_x$ films. Low residual stress (-9Mpa, compressive) and low strain gradient ($1x10^{-5}\mu m^{-1}$) were achieved in as-deposited poly-$Si_{0.4}Ge_{0.6}$ films deposited at 450°C and 600mTorr. These results are promising for achieving as-deposited flat microstructure p+$Si_{1-x}Ge_x$ films. Since amorphous films are not conductive enough for most MEMS applications, as-deposited polycrystalline films can be achieved at a deposition temperature below 450°C, with a germanium concentration above 60%. Similar poly $Si_{1-x}Ge_x$ deposition parameters were used in this study. The precursor gas flow rates for this experiment as well as the $Si_{1-x}Ge_x$ films deposition conditions are summarized in **Table 2.1**.

Table 2.1: P+ poly- $Si_{1-x}Ge_x$ deposition parameters

Parameters	**Films deposited at 400°C**	**Films deposited at 450°C**
SiH_4/B_2H_6 flow rates	100 sccm/60 sccm	100 sccm/58 sccm
GeH_4 flow rate	60 sccm	60 sccm
Pressure	600 mTorr	600 mTorr
Ge content	65%	65%
Average film thickness	0.6 μm	0.9 μm
Resistivity	1.2 mΩ-cm	1.5 mΩ -cm

2.3.1. Resistivity

The sheet resistance of the $Si_{1-x}Ge_x$ films was measured with a four-point probe instrument at four different positions on the wafer and the average values have been reported (**Table 2.1**). The film thickness was determined with a calibrated spectroscopic reflectometer. Results provided expected values matching the published etch rate of p+ $Si_{0.4}Ge_{0.6}$ of about 1μm/hour [2.11]-[2.13]. The resistivity of the films was in the acceptable range of 1.0mΩ to 2.0mΩ.

2.3.2. Ge concentration and film microstructure

Secondary Ion Mass Spectrometry (SIMS) was used to determine the Ge content of the films, which was found to be around 65%.

A scanning electron micrograph of the completed Kelvin test structure is shown in **Figure 2.4**. It can be seen that the films are polycrystalline with large grains, and that the deposition inside the contact holes is very conformal.

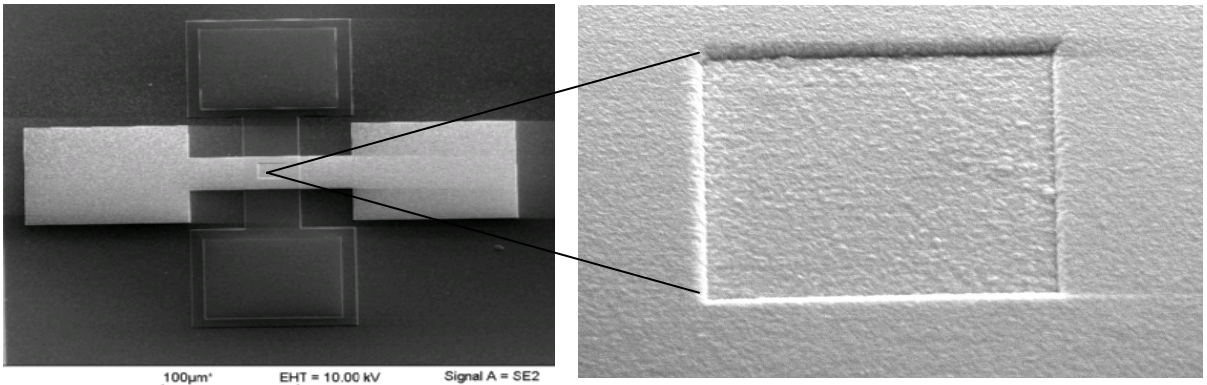


Figure 2.4: **(a)** Scanning electron micrograph of fabricated Kelvin test structure **(b)** Close-up view of a $(10\ \mu m)^2$ contact.

2.4. Contact resistance

An HP4155 precision semiconductor parameter analyzer was used to measure the current-vs-voltage (*I*-*V*) characteristics of the fabricated Kelvin structures. For each sample, several structures were measured and a standard linear regression procedure was employed to extract the contact resistivity, ρ_c.

$$R_c = \frac{\Delta V}{I} \text{ and } \rho_c = R_c \times ContactArea \quad (\textbf{\textit{Equation 2.1}})$$

As expected, it was observed that the contact resistance decreases with increasing contact area. Most of the $2\mu m^2$ contact holes of this run did not print. Careful inspection with an optical microscope shows that the contact areas were smaller than the dimensions designed on the mask. This was attributed to poor lithography resolution, which did not allow for complete etching of the contact holes. Scanning Electron Microscopy (SEM) provided a better estimation of the exact dimensions of contact holes after all lithographic steps. These experimental values were used to compute the contact resistivity (ρ_c).

2.4.1. Pre-cleaning issues

For VLSI MOS clean LPCVD processes, processing experience from the IC industry has helped to develop a standard pre-cleaning treatment prior to $Si_{1-x}Ge_x$ deposition. However, no IC foundries will allow non-MOS compatible MEMS wafers to be processed with CMOS wafers because of contamination issues. In order to demonstrate a reliable, high performance modular integration of MEMS structures with electronics, a non-MOS clean LPCVD furnace, where $Si_{1-x}Ge_x$ micromachined structural layers could be deposited on metallized wafers was acquired. Since there was no prior

experience in cleaning metallized wafers, one of the challenges encountered throughout this study was to develop an optimum and reliable pre-cleaning process prior to p+ $Si_{1-x}Ge_x$ deposition. This turned out to be very critical for achieving a good surface interface between the films. It was found that p+ poly $Si_{1-x}Ge_x$ deposited directly onto metal without any pre-deposition treatments yields a high contact resistance, with ρ_c ranging from $7\times10^{-5}\Omega$-cm^2 to $10^{-3}\Omega$-cm^2 (**Figure 2.5**). Therefore, various pre-cleaning processes prior to poly-$Si_{1-x}Ge_x$ deposition were subsequently investigated to improve the contact interface between the $Si_{1-x}Ge_x$ and the metal stack.

2.4.1.1. Helium plasma pre-cleaning

First, helium plasma exposure prior to $Si_{1-x}Ge_x$ deposition was studied. In a parallel-plate reactive-ion etcher, the wafers were submitted to a helium plasma treatment for about 7 minutes followed by poly- $Si_{1-x}Ge_x$ deposition. This yielded a lower contact resistivity ($\sim \rho_c \sim 7\times10^{-6}$ Ω-cm^2) than $Si_{1-x}Ge_x$ depositions without any special pre-cleaning process, but still higher than desired. **Table 2.2** summarizes contact measurements of wafers pre-cleaned with helium plasma. The standard deviation for smaller contact dimensions was quite high compared to that of larger contact areas.

Table 2.2: Average contact resistance and resistivity for $Si_{0.65}Ge_{0.35}$ deposited at 450°C.

Contact Area	Average Contact Resistance(Ω)	Average Contact Resistivity (Ω-cm^2)	Standard Deviation
1.40×10^{-7}cm^2	24.6	3.46×10^{-6}	10.2
3.42×10^{-6}cm^2	2.4	8.36×10^{-6}	1.04
3.61×10^{-6}cm^2	2.3	8.33×10^{-6}	1.01

2.4.1.2. Argon plasma pre-cleaning

The atomic weight of Argon (40g/mol) is ten times larger than the atomic weight of helium (4g/mol). Therefore, it is expected that an argon plasma sputter etch would be more efficient than a helium plasma treatment for clearing the surface of contaminants. IC processing often involves an argon sputter etch before any thin film deposition in order to insure a good interface between the thin films to be sputtered and the underlying layers [2.6]. A negative bias relative to the plasma is applied to the wafer electrode, which becomes electrically isolated from the chamber walls. Positive argon ions from the plasma are accelerated towards the wafers on the substrate carrier and sputter off impurity atoms. The energy of the ions (thus the sputtering yield) can be controlled by controlling the substrate bias [2.6].

A new cleaning process using argon plasma was investigated and implemented. An argon sputter etch was performed in a PVD cluster tool at 75 Celsius using a 60Mhz RF generator. During the 30 second sputter etch procedure, no deposition was allowed to occur in the wafer. A controlled thickness of surface material was sputtered off the wafer, removing any contaminants and native oxides. The new cleaning process involving argon plasma was as follow: after contact opening on the LTO layer, the wafers were dipped in a solution (100:1) of 49% concentrated hydrofluoric acid for 1 minute to etch away any residual native oxides. Then they were placed in a sputter system for the argon sputter-etch. **Figure 2.5** shows that the specific contact resistivity of films cleaned with argon plasma improved by a factor of three compared to the films that had been cleaned with helium plasma. Detailed process parameters for both pre-clean processes are presented in **Table 2.3**.

Table 2.3: Helium plasma pre-clean treatment compared to argon plasma pre clean treatment.

Pre-cleaning Process	**argon pre-cleaning**	**helium pre-cleaning**
Tool	Physical Vapor Deposition System (Sputter/Etcher)	Parallel plate Plasma Etcher
RF power	250watts	300watts
Sputter Etch Pressure	4mtorr	300mtorr
Cleaning time	30 to 60 seconds	7 minutes
Contact Resistivity for $2\mu m^2$ contact hole	Avg. ρ_c: $3.1\times10^{-6}\ \Omega\text{-cm}^2$	Avg. ρ_c: $9.5\times10^{-6}\Omega\text{-cm}^2$
	σ: 1.9×10^{-7}	σ: 1.2×10^{-6}

Note: σ represents the standard deviation of the measurements

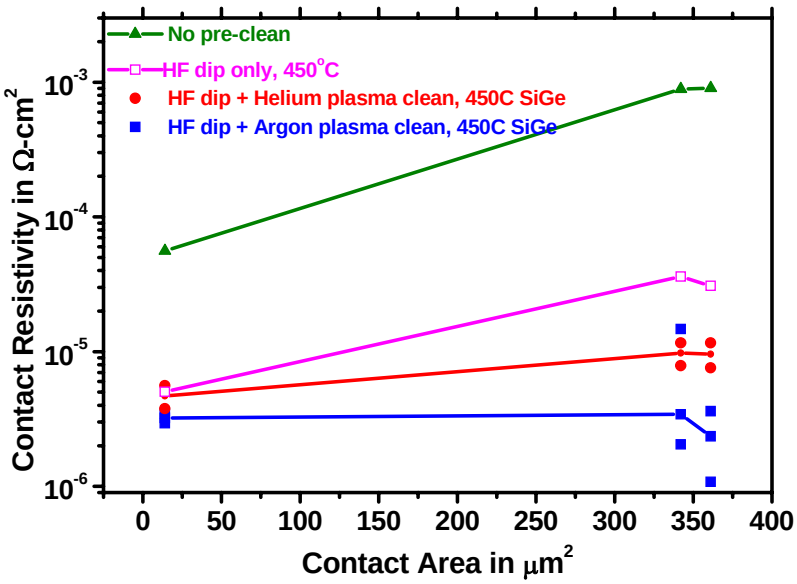


Figure 2.5: Effect of pre-clean treatment on contact resistivity of $Si_{1-x}Ge_x$ films deposited at 450°C for a $(5\mu m)^2$ contact.

Two process parameters of the pre-clean treatments were modified to further improve the contact interface, thus potentially reducing R_c.

- Increasing the HF dip time did not bring much improvement.
- Argon pre-cleaning sputter time was consecutively increased from one to fifteen minutes. No significant improvement was noticed.

It was not desirable to increase the RF power of the PVD tool in order to avoid significantly etching the metal stack, which would yield to a rougher surface interface.

2.4.1.3. Discussion

Although an HF dip followed by a special pre-clean treatment (argon or helium plasma) was performed before the wafer loading step in the LPCVD furnace, the wafers still remained at atmospheric pressure during the furnace temperature stabilization step for about thirty minutes. As a result, native oxides could still grow on the surface of the wafers during this time interval.

The fact that argon plasma pre-clean treatment provides lower contact resistance than helium plasma is expected since the atomic mass of argon is larger than that of helium. Therefore, ion kinetic energy considerations suggest that the argon sputtering treatment would be more effective at removing interface contaminants.

To improve the interface prior to $Si_{1-x}Ge_x$ deposition, different pre-cleaning treatments have been investigated. A comparative study of helium and argon plasma pre-clean was performed. It was observed that an argon sputter etch lowers contact resistance by a factor of three compared to the standard helium pre-clean treatment. Yet this might not be the optimum cleaning process for batch processing of MEMS integrated devices. In order to sputter clean the wafers, the wafers were carried out of the Microfabrication Laboratory to another laboratory where the PVD sputter tool system was located. A more reliable process for batch processing of MEMS integrated structures will require an *in-*

situ pre-clean process inside the LPCVD furnace prior to $Si_{1-x}Ge_x$ deposition [2.14]. This would provide an even better surface interface. Further interface improvements might be obtained with *in-situ* cleaning processes such as pure germanium flow prior to the actual deposition. It was previously reported that Ge does not form a stable oxide [2.15]-[2.16]. Since GeOx is volatile, flowing pure germanium prior to $Si_{1-x}Ge_x$ deposition could help to remove the inevitable native oxide that gets formed when the wafers remain in atmospheric pressure during the furnace temperature stabilization step. Contact measurements results using Ge *in-situ* cleaning are presented in Section 2.7.3.

2.4.2. $Si_{1-x}Ge_x$ deposition temperature effects

2.4.2.1. Contact measurements results

The effect of $Si_{1-x}Ge_x$ deposition temperature on contact resistance was investigated. **Figure 2.6** shows contact resistance measurements obtained for a $5\mu m^2$ contact for a wafer pre-cleaned using helium plasma. From the plot, we can see that films deposited at 450°C show lower contact resistance than films deposited at 400°C.

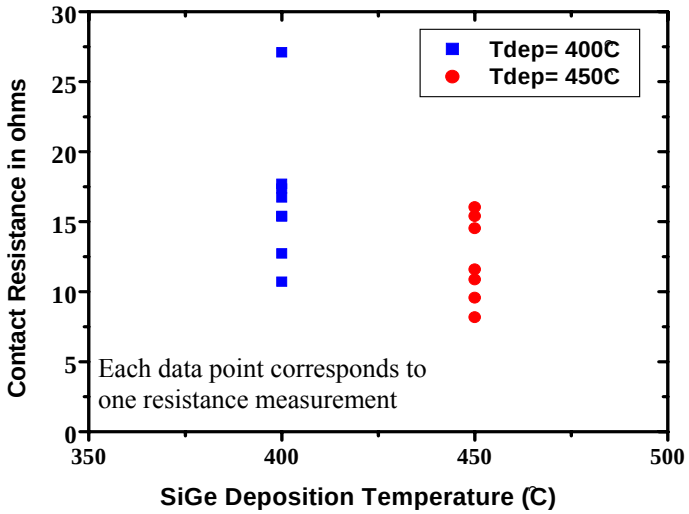


Figure 2.6: Effect of poly- $Si_{1-x}Ge_x$ deposition temperature on contact resistance for a $(5\mu m)^2$ contact. HF dip + helium plasma were used as pre-furnace cleaning treatments. Ge concentration are similar at both temperatures.

2.4.2.2. Discussion

For a fixed Ge content, the contact resistance decreases with increasing $Si_{1-x}Ge_x$ deposition temperature (**Figure 2.7**), probably because of enhanced reaction between poly-$Si_{1-x}Ge_x$ alloy and the underlying metal film. However, there is even stronger dependence of the contact resistance on Ge content, so that higher Ge content films deposited at lower temperature yield significantly lower contact resistance than lower Ge content films deposited at higher temperatures (**Figure 2.7**). *Jeon et al.* reported similar results for n-type $Si_{1-x}Ge_x$ films [2.17]. Overall, these new results confirm previous studies that have demonstrated that Ge rich films provide lower resistivity, and now lower contact resistance.

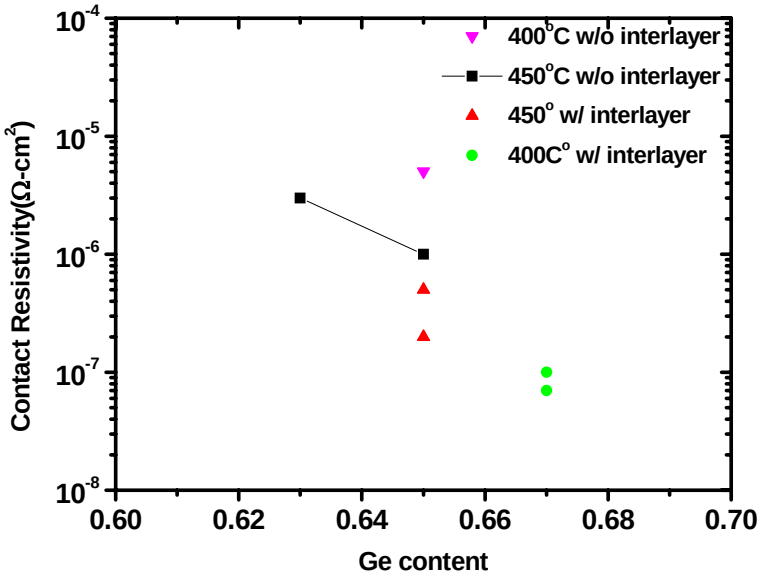


Figure 2.7: Contact resistivity dependence on Ge content and temperature for a $(5\mu m)^2$ contact. HF dip + Ar plasma were used as the pre-furnace cleaning treatments

2.5. Germanosilicide process

2.5.1. Fabrication process flow

Silicides are routinely used in the IC industry to provide low contact resistance between silicon and metal interconnects. Recently, nickel germanosilicide was reported to form low resistivity contacts to $Si_{1-x}Ge_x$ at ~400°C in advanced Source/Drain CMOS technology [2.18]. Therefore, a slight modification to the metal interconnect stack was explored to achieve even lower contact resistance to p+ $Si_{1-x}Ge_x$ film. As shown in **Figure 2.8**, a thin Ni layer (20 nm) was sputtered onto TiN (with capping Al) prior to patterning of the metal stack. After the deposition of an oxide interlayer dielectric and patterning of contact holes, poly-$Si_{1-x}Ge_x$ was deposited at 400°C or 450°C using the same deposition conditions reported in Table 2.1. A short HF dip was used to pre-clean the wafers prior to LPCVD treatment. It is important to note that it is not possible to deposit nickel after contact-hole formation, due to the poor adhesion of nickel to SiO_2.

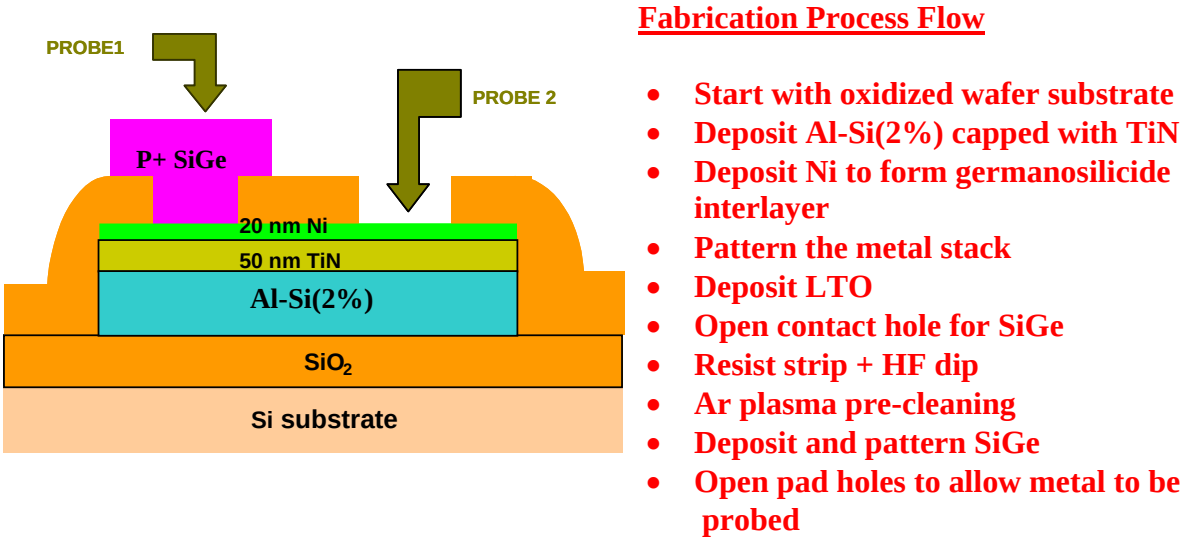


Figure 2.8: Schematic cross-section and fabrication process flow of Ni-germanosilicide contact process.

2.5.2. Contact measurement results

As shown in **Figure 2.9**, the average ρ_c falls below 10^{-7} Ω-cm^2, which represents over an order of magnitude improvement compared to contacts formed without the Ni interlayer. SIMS analysis revealed that the Ge concentration in the films deposited at 400°C was larger than those deposited at 450°C, since these showed relatively lower contact resistivity values.

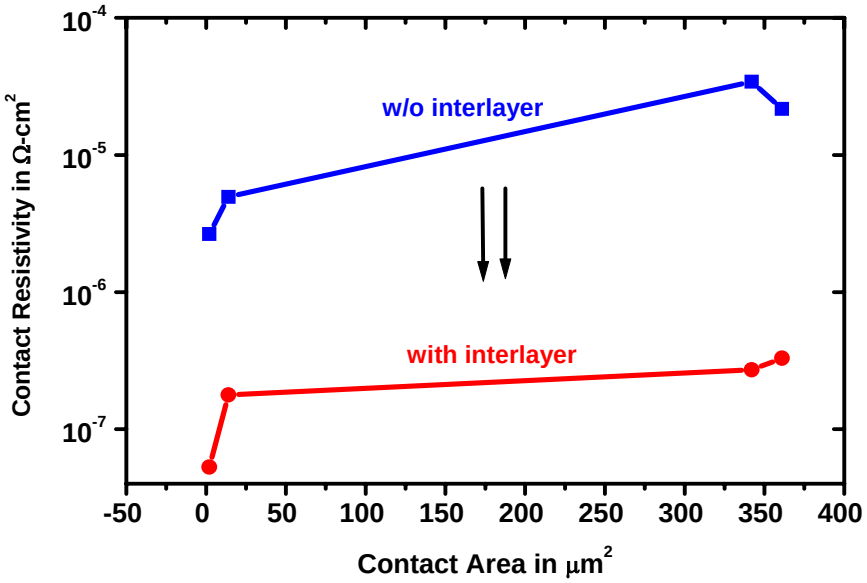


Figure 2.9: Comparison of contact resistivity measurement for process flow with an interlayer metal against that without an interlayer. HF dip + Ar plasma were used as pre-furnace cleaning treatments. $Si_{1-x}Ge_x$ was deposited at 400°C.

Figure 2.10 shows a cross-sectional transmission electron micrograph of the contact area. Elemental analysis was performed and indicates that Ni reacted with poly-$Si_{1-x}Ge_x$ to form a low resistivity intermediate layer of germanosilicide. In addition, we can see that the Ni-germanosilicide has very rough microstructure grains, which is representative of silicide films.

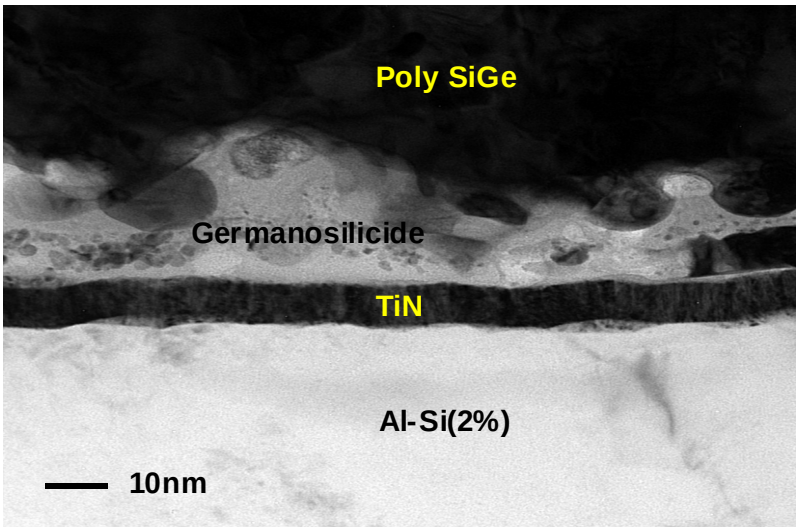


Figure 2.10: TEM micrograph showing cross section of the contact region using a silicide interlayer. P+$Si_{0.35}Ge_{0.65}$ films were deposited by LPCVD at 450°C.

2.5.3. Discussion

It was demonstrated that it is possible to achieve a very low contact resistance between $Si_{1-x}Ge_x$ and Al in the acceptable range of 10^{-8} Ω-cm^2 to 10^{-7} Ω-cm^2, by using a germanosilicide interlayer. However, some important issues need to be addressed before this process can be used for mass production of the MEMS integrated devices:

- Process complexity: It is always desirable to keep the fabrication process as simple as possible to increase yield. This requires adding one more deposition and etching step, which makes the process flow more complex.
- Cost: The addition of one more deposition step makes the process less economical. Although nickel by itself is not expensive, the usage and

maintenance of the sputter PVD cluster tool used for nickel deposition would make the fabrication process more costly.

In the future, low resistivity silicides might also be formed with other materials such as platinum, which was also reported to reduce parasitic series resistance in an advanced S/D CMOS technology [2.18].

2.6. Annealing effects

Other approaches to lower the specific contact resistivity within a low thermal budget were explored. These include thermal annealing and laser annealing crystallization.

2.6.1. Thermal annealing

Depending on the particular application, it is often desirable to anneal MEMS structural films to lower the resistivity, the residual stress and strain gradient of micromachined structures [2.19]. This is accomplished by exposing the wafers to a suitable temperature treatment (~500°C to 600°C) in an inert environment for a few minutes. The process activates the dopants that initially occupy interstitial sites, yielding a reduction in the film resistivity.

It was previously demonstrated that aluminum can withstand a thermal annealing process at 550°C for an average time of an hour [2.20]. In this study, the effect of a one hour 450°C anneal on contact resistance was investigated. No major change was

observed from the measurements. A second annealing treatment at the same temperature and same duration did not bring much improvement.

2.6.2. Excimer laser annealing

Pulsed-excimer–laser annealing was reported to be a low temperature annealing technique that improves the residual stress and the strain gradient of micromachined poly-$Si_{1-x}Ge_x$ films [2.21]-[2.23]. Using a pulsed laser source (KrF of wavelength 248nm) with laser energy varying from 120mJ/cm^2 to 790mJ/cm^2, the grain microstructure of $Si_{1-x}Ge_x$ can be changed from amorphous to polycrystalline. The laser impulse causes melting of the $Si_{1-x}Ge_x$ surface in a few nanoseconds, and then it recrystallizes in about 10ns. This eventually yields a significant reduction in the resistivity of the $Si_{1-x}Ge_x$ films [2.23].

The effects of pulsed-excimer laser annealing were investigated in view of improving the $Si_{1-x}Ge_x$ to Al contact interface. The goal was to melt and recrystallize the $Si_{1-x}Ge_x$ alloys at the surface, but also throughout the film. Sample dies were submitted to short pulsed-laser annealing of 30ns duration, with energies ranging from 300mJ/cm^2 to 600mJ/cm^2. No improvement was noticed after contact resistance measurements.

2.6.3. Discussion

Thermal annealing lowers films resistivity by activating the dopants, while laser annealing lowers resistivity by changing the grain microstructure of the films from amorphous to polycrystalline. However, if the contact interface between the p+ poly- $Si_{1-x}Ge_x$ films and the metal interconnect is very poor, neither of these techniques is expected

to bring much improvement. Therefore, it is concluded that an improvement of the surface interface is the most critical step necessary to achieve low $R_{C.}$

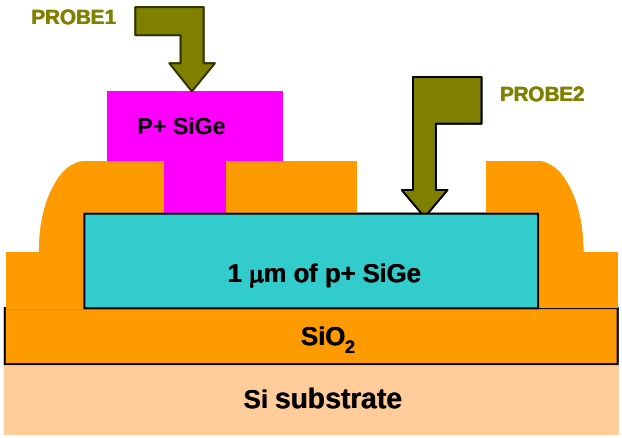
2.7. SiGe to SiGe contact resistance

2.7.1. Motivation

In a modularly integrated MEMS technology, the structural layer (SiGe1) is usually anchored to a ground-plane layer (SiGe0) – see **Figure 2.1**. The contact between poly-SiGe1 and poly-SiGe0 must be electrically conductive, to allow for DC biasing of the structural layer. Low contact resistance is necessary for good system performance. Therefore, a study of the SiGe1-to-SiGe0 contact resistance was conducted.

2.7.2. Experiments

The fabrication process flow used for this present study is analogous to that described in Section 2.2. The only difference is the fact that a second layer of p+ poly $Si_{0.36}Ge_{0.65}$ film replaced the metal stack. In addition, a new *in-situ* pre-cleaning treatment using a high flow of GeH_4 gas prior to $Si_{1-x}Ge_x$ deposition was implemented to further improve the contact interface. Poly $Si_{1-x}Ge_x$ deposition parameters were similar to that described in **Table 2.1,** except that the deposition temperature was reduced to 425°C. The resistivity of the films was consistent with previous results (~ 2mΩ-cm). **Figure 2.11** presents the cross-section of the Kelvin test structure after fabrication and describes the process flow.



Fabrication Process Flow

- **Start with oxidized Si wafer substrate**
- **Deposit and pattern p+SiGe**
- **Deposit SiO_2 (LTO)**
- **Open contact hole for SiGe**
- **Resist strip + HF dip (then in situ cleaning in LPCVD furnace)**
- **Deposit and pattern second layer of p+ poly SiGe**
- **Open pad holes to allow SiGe to be probed**

Figure 2.11: Cross-section of the Kelvin structure used for SiGe to SiGe contact

2.7.3. Ge in-situ pre-cleaning process

For batch processing of MEMS integrated structures, a more reliable cleaning process would require an *in-situ* cleaning process inside the LPCVD furnace prior to $Si_{1-x}Ge_x$ deposition. It was previously reported that Ge does not form a stable oxide [2.15]. Since Germanium oxide is volatile, flowing pure germanium prior to $Si_{1-x}Ge_x$ deposition can help to remove the inherent native oxide that is formed when the wafers remain in atmospheric pressure during the temperature stabilization step.

After contact openings of the LTO layer, the wafers were pre-cleaned with a concentrated solution of hydrofluoric acid as described before, and no plasma cleaning treatment was used after the HF dip. Then the wafers were submitted for ~ 2 minutes to a GeH_4 flow followed by $Si_{1-x}Ge_x$ deposition. A standard seed layer recipe presented in **Table 2.4** was created for this purpose.

Table 2.4: P+ poly $Si_{1-x}Ge_x$ deposition conditions of seed layer and $Si_{1-x}Ge_x$ layers.

	Seed layer of pure Germanium	**p+ poly $Si_{1-x}Ge_x$**
Temperature	425°C	425°C
SiH_4/B_2H_6 flow rates	0sccm/0sccm	100 sccm/60 sccm
GeH_4 flow rate	150sccm	60 sccm
Pressure	600 mTorr	600 mTorr
Deposition time	2 minutes	55 minutes
Resistivity	----	2 mΩ-cm
Expected Ge concentration	----	63%

2.7.4. Contact measurement results

The measurement procedure described in section 2.4 was used to measure the contact resistance. In order to get a more accurate estimation of R_C, the series resistance resulting from $Si_{1-x}Ge_x$-to-$Si_{1-x}Ge_x$ contacts needed to be taken into account (**Figure 2.12**).

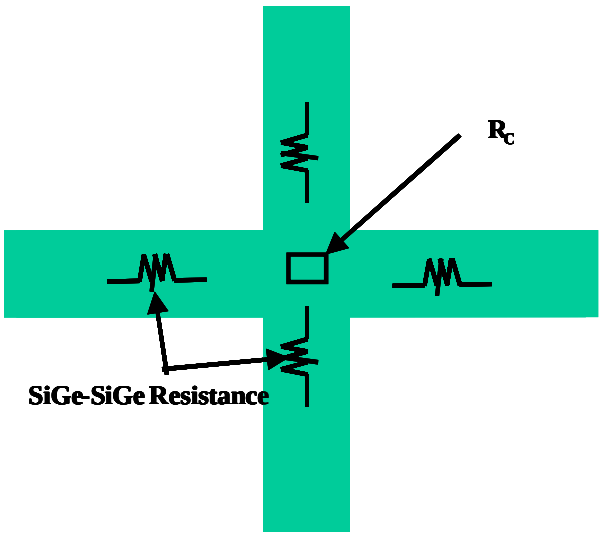


Figure 2.12: Kelvin structure taking into account series resistance $Si_{1-x}Ge_x$ -to- $Si_{1-x}Ge_x$.

This parasitic resistance was neglected in the contact measurement between Al and $Si_{1-x}Ge_x$ because Al has almost zero series resistance. However as a semiconductor, the $Si_{1-x}Ge_x$ film has a finite inherent resistance that cannot be neglected. ***Equation 2.2*** was used to estimate the true value of the contact resistance.

$$TrueR_c = MeasuredR_c - \rho_{SiGe}\left(\frac{1\mu m}{ContactArea}\right) \quad (\textbf{\textit{Equation 2.2}})$$

The series resistance extracted from this formula turned out to be about 10% for the 5μm contact hole, and more significant for larger contact dimensions. The results indicate that $\rho_c \sim 1\times10^{-6}$ Ω-cm^2, which is comparable to that of metal-to-Si contacts in modern integrated circuits. Also, an *in-situ* pre-cleaning treatment (exposure to pure GeH_4) prior to p+ poly-$Si_{0.35}Ge_{0.65}$ deposition was beneficial to reduce ρ_c (**Figure 2.13**).

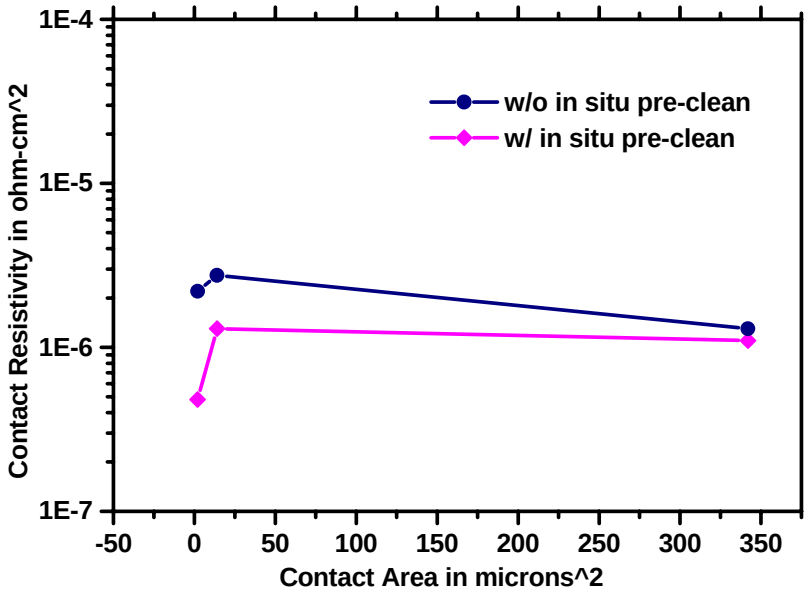


Figure 2.13: $Si_{1-x}Ge_x$ to $Si_{1-x}Ge_x$ contact resistivity results with and without *in-situ* treatment.

2.7.5. Discussion

Ideally, we would expect zero resistance between two analogous materials if the surface interface is totally free of contaminants and oxides. But the measurement shows that the average $Si_{1-x}Ge_x$-to-$Si_{1-x}Ge_x$ resistivity is around $1\times10^{-6}\Omega$-cm^2; this clearly indicates the presence of some remnant native oxide in the contact area.

In addition, it was demonstrated that GeH_4 pre-cleaning could be an acceptable *in-situ* cleaning treatment for improving the contact interface prior to $Si_{1-x}Ge_x$ deposition. **Table 2.5** presents the contact resistivity data obtained with and without a Ge *in-situ* cleaning treatment.

Table 2.5: Contact resistance and resistivity compared for process with and without *in-situ* cleaning.

Contact Area	**Without *in-situ* Cleaning**			**With *in-situ* Cleaning**		
	***M-R_c(Ω)**	**T-R_c(Ω)**	**T-ρ_C(Ω-cm^2)**	***T-R_c(Ω)**	**T-R_c(Ω)**	**T-ρ_C(Ω-cm^2)**
4×10^{-8} cm^2	55	50	2.0×10^{-6} Ω-cm^2	12Ω	7Ω	2.8×10^{-7} Ω-cm^2
2.5×10^{-7} cm^2	11	10.2	2.5×10^{-6} Ω-cm^2	5.5Ω	4.7Ω	1.2×10^{-6} Ω-cm^2
1.0×10^{-6} cm^2	1.3	1.1	1.1×10^{-6} Ω-cm^2	1.1Ω	0.9Ω	0.9×10^{-7} Ω-cm^2

Note: *M-R_c means measured contact resistance data

*T-R_c means true contact resistance values

2.8. Summary

The contact resistance of a p+ poly-$Si_{1-x}Ge_x$ film deposited directly onto TiN-capped Al-Si (2%) by LPCVD at temperatures compatible with CMOS electronics was investigated.

Without any pre-cleaning treatment, the contact resistivity ρ_c was found to exceed $10^{-5}\Omega$-cm^2, which is too high for forming low-resistance contacts between SiGe MEMS devices and the underlying CMOS circuitry. For fixed Ge content, a higher deposition temperature (450ºC) yields lower contact resistance. A plasma pre-cleaning treatment prior to $Si_{1-x}Ge_x$ deposition substantially improves the contact resistivity, with Ar plasma being more effective than He plasma for this purpose. The most dramatic improvement in contact resistivity is achieved by capping the metal with a thin Ni layer, so that an intermediary germanosilicide layer is formed between the metal and the $Si_{1-x}Ge_x$ film during the $Si_{1-x}Ge_x$ deposition process. This yields a very low contact resistivity of $10^{-7}\Omega$-cm^2, which is suitable for forming low-resistance contacts between the MEMS and CMOS devices.

SiGe-to-SiGe contacts were also characterized, and the resistivity was found to be around $1\times10^{-6}\Omega$-cm^2, what indicates that there could still be some remnant native oxide in the contact area. An *in-situ* pre-cleaning treatment (exposure to pure GeH_4) prior to p+ poly-$Si_{0.35}Ge_{0.65}$ deposition was found to be helpful for reducing ρ_c.

The results of this study reveal that it is possible to achieve contact resistivity in the acceptable range of $10^{-6}\Omega$-cm^2 (and even lower), which is needed for modularly integrated MEMS devices. This is attained through a proper cleaning of the wafers prior

to LPCVD treatment, as well as the usage of an intermediate silicide layer. The findings of this study are summarized in **Table 2.6**.

Table 2.6: Summary of specific contact resistivity (Ω-cm^2) of this study. Data was extracted for a $(2\mu m)^2$ contact.

	SiGe Deposited at 400^{o}C		**SiGe Deposited at 450^{o}C**	
	Average	σ	Average	σ
No pre-cleaning	Not investigated		8.4×10^{-4}	3.2×10^{-5}
helium pre-cleaning	5.5×10^{-5}	3.2×10^{-6}	9.5×10^{-6}	1.2×10^{-6}
argon pre-cleaning	8.7×10^{-6}	8.3×10^{-6}	3.1×10^{-6}	1.9×10^{-7}
Silicide interlayer	7.8×10^{-8}	3.2×10^{-8}	9.4×10^{-7}	3.5×10^{-7}

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Chapter 3

Boron Doping Effect on Structural Properties of $Si_{1-x}Ge_x$ Films

3.1. Introduction

Previous studies on n-type $Si_{1-x}Ge_x$ films doped with phosphorus show that the as-deposited films have a very high resistivity (>200mΩ-cm), so that a high temperature annealing procedure is necessary to activate the dopant atoms in order to reduce the films resistivity. For this purpose, n+ poly $Si_{1-x}Ge_x$ samples are routinely placed for four to five hours in standard furnaces with temperature above 450^{o}C or for one to five minute in rapid thermal annealing (RTA) furnaces [3.1]-[3.5]. However, according to recent findings on the reliability of ICs after annealing, CMOS back-end-process that uses aluminum interconnects can withstand one minute of a 550^{o}C furnace annealing procedure [3.6]. Further studies reveal that the interconnects' vias of a state-of-the art CMOS technology would start degrading after six hours at a 450^{o}C annealing temperature [3.7]. These results place a stringent temperature limitation requirement for the usage of n-type $Si_{1-x}Ge_x$ films for modularly integrated system.

In the case of p-type poly-$Si_{1-x}Ge_x$ films, dopants are easily activated during the films deposition, thus eliminating the need for post-deposition annealing process for the reduction of the films' resistivity. Therefore, as-deposited p-type $Si_{1-x}Ge_x$ films can have lower resistivity compared to as-deposited n-type films. Moreover, the deposition rate of the p-type $Si_{1-x}Ge_x$ films is twice that of n-type $Si_{1-x}Ge_x$ films since boron increases the deposition rate while phosphorus retards it [3.1]. A higher deposition rate of the films would eventually lead to a lower manufacturing cost of the MEMS integrated systems when p-type poly-$Si_{1-x}Ge_x$ films are used instead of their n-type counterpart.

Considering the two main benefits mentioned previously, p-type polycrystalline $Si_{1-x}Ge_x$ film has been adopted as a baseline material for the realization of a robust, reliable, high performance and low cost SiGe MEMS technology. Ideally both the structural p+ $Si_{1-x}Ge_x$ films and sacrificial p+ Ge films are heavily doped to increase the deposition rate of the films, thus reducing the cost of the technology and avoiding dopant codiffusion within the films' interface [3.8]-[3.10]. In this chapter, a thorough study on the effects of boron doping in the electrical, mechanical, chemical and material properties of $Si_{1-x}Ge_x$ technology was performed for optimization of the films' deposition conditions [3.11]. P+ poly-Ge was used as the sacrificial layer while p+ poly-$Si_{1-x}Ge_x$ films were used as the structural layer for the integrated MEMS devices.

3.2. Experimental details

3.2.1. Processing of p+poly-Ge sacrificial layer

P-type Ge films were deposited at 350°C and 300mTorr onto oxidized Si wafers, with a very thin (<10nm thick) amorphous-Si seed layer, in a conventional low-pressure chemical-vapor deposition (LPCVD) system using GeH_4 (170 sccm) as the Ge precursor gas, and B_2H_6 as the dopant gas. The B_2H_6 is diluted (to 10%) in H_2 and is introduced from the back of the furnace through an injector that has different sizes of holes in order to minimize gas depletion effects, while the GeH_4 is introduced through a ring at the front of the tube. Because of this arrangement, the boron and germanium concentration on the silicon wafers vary based on the wafer position inside the LPCVD furnace. For the same recipe, the germanium content increases from the front to the back of the tube, while it's the opposite in the case of the boron content (the boron content in the $Si_{1-x}Ge_x$ films increases from the back to the front of the tube) (**Figure 3.1**).

Moreover, when using B_2H_6 as the dopant gas source, boron atoms tend to accumulate over time inside the injector. This often leads to the undesirable situation in which the injector holes get clogged so that the effective boron doping transferred into the tube can be significantly altered with time. In order to eliminate this problem, thus providing a more repeatable and robust boron doped SiGe MEMS process, the $Si_{1-x}Ge_x$ films reported in this study were deposited within the same period of time (a week time span). More recently, BCl_3 doping gaseous source was demonstrated to be an alternative p-type doping source that facilitates the decomposition of the reactive species without forming a solid around the injector holes, so that the injector clogging issue often encountered with B_2H_6 doping source is eliminated [3.12]-[3.13].

The sheet resistance of the films was measured at several points of each wafer using a four-point probe instrument, average values are reported herein. Measurement of the films' thickness is not accurate using optical measurement because the unknown refraction index of the $Si_{1-x}Ge_x$ films which is highly dependant on the Ge concentration in the films. Therefore, a step-height measurement technique was used to characterize the $Si_{1-x}Ge_x$ films' thickness. For this purpose, the p+ Ge films were patterned into test structures using conventional optical lithography and etched using Cl_2/HBr reactive ion etch (RIE) chemistry. The film thickness was determined from step-height measurements using an alpha step IQ surface profiler. The same test structures were used for the characterization of the etch rate of p+ Ge films with various doping concentration in a 90°C heated solution of hydrogen peroxide (H_2O_2). For this experiment, H_2O_2 solution was placed in a plastic beaker that was set to rest in a larger, heated beaker half-filled with water. A thermometer was used to monitor the temperature inside the peroxide bath to keep it at the 90°C set-point. A figure showing a schematic of the experimental set-up for characterization of the wet release process of p+ poly-Ge in H_2O_2 is presented in **Figure 3.2**. The Ge etch rate was characterized by monitoring the step height in between different release process for films of various Ge and B content.

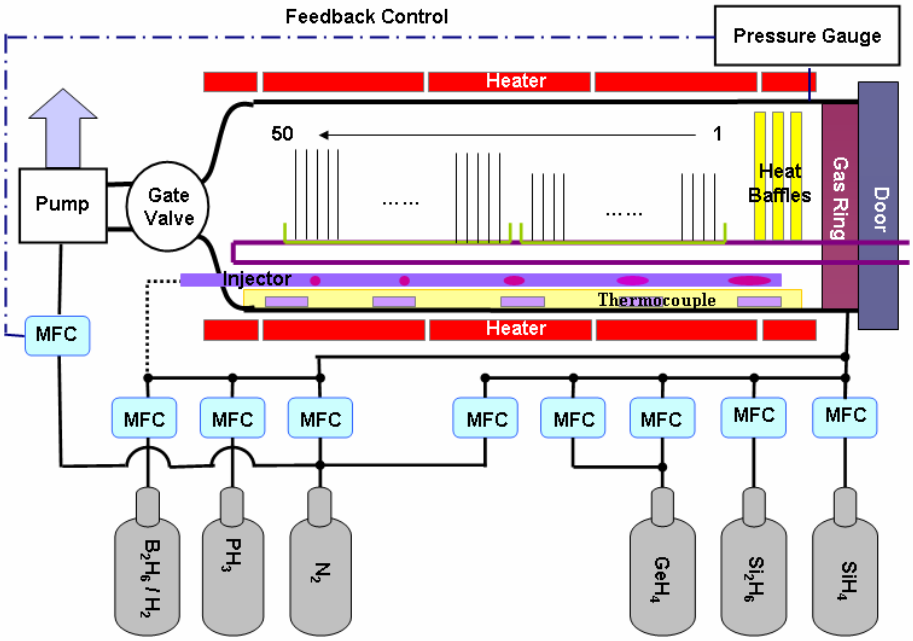


Figure 3.1: Cross section of the LPCVD reactor used to deposit the p+Ge and p+ $Si_{1-x}Ge_x$ films:

- SiH_4 and GeH_4 are fed through the back of the tube, resulting in the fact that wafers placed at back of the furnace have higher Ge content.
- B_2H_6 is fed through the front injector, resulting in the fact that wafers placed at front of the furnace have higher B content.

(Figure is a courtesy of *C. Low*)

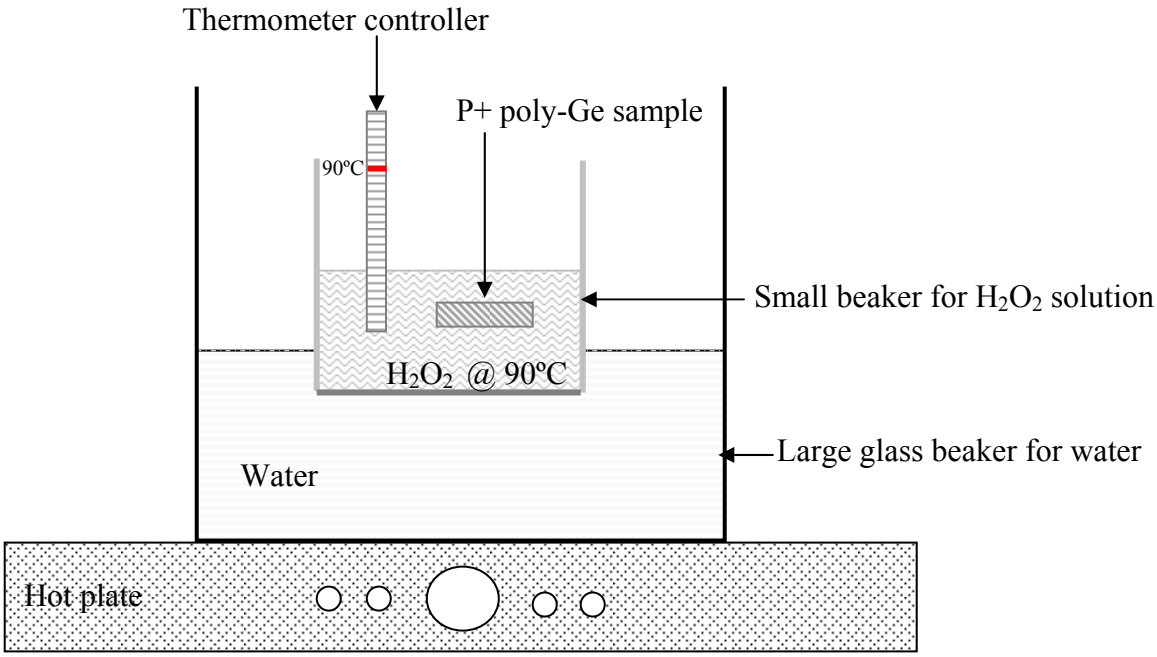


Figure 3.2: Experimental set-up for the characterization of p+ $Si_{1-x}Ge_x$ and p+Ge etch rates in a 90°C heated solution of hydrogen peroxide (H_2O_2) for the study of boron doping effects on the etching properties of the p+ $Si_{1-x}Ge_x$ structural films as well as p+ Ge sacrificial films.

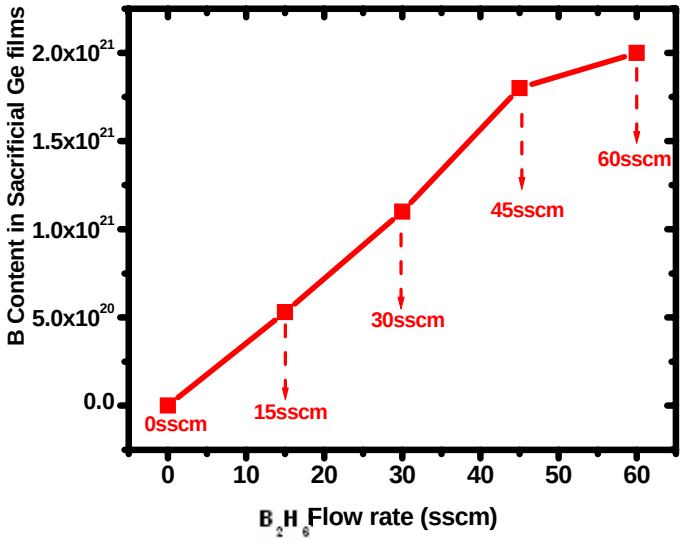
3.2.2. Processing of p+ poly-$Si_{1-x}Ge_x$ structural layer

P-type poly-$Si_{1-x}Ge_x$ films were deposited at 425°C and 400mT in the same LPCVD system onto oxidized Si wafers (p-type, 1ohm/square) coated with ~2.2μm of undoped low temperature oxide (LTO). The purpose of the LTO layer is to insure electrical isolation of the fabricated structures from the silicon substrate. SiH_4 was used as the precursor silicon gas (**Figure 3.1**). The films' resistivity was measured using a four point probe measurement tool. The boron and germanium concentration in the deposited films were determined by SIMS analysis (2.5% accuracy), and varied from $1\times10^{19}cm^{-3}$ to $5\times10^{21}cm^{-3}$ and 61% to 67%, respectively. **Figure 3.3** shows a plot of the boron concentration in the films as a function of the B_2H_6 flow rate for p+ Ge sacrificial layer (**Figure 3.3a**) and for p+ $Si_{1-x}Ge_x$ structural layer (**Figure 3.3b**). In order to determine thin film stress, wafer curvature measurements were made using a Tencor FLX-2320 instrument before and after $Si_{1-x}Ge_x$ deposition (with the backside $Si_{1-x}Ge_x$ film removed). The films were patterned into cantilever-beam test structures (**Figure 3.4**) and then released using a timed etch process in 49% concentrated HF. After wet release process, a critical point dry process was performed using CO_2 in order to alleviate the severe effects of stiction that often occurs in MEMS devices after release. Stiction is defined as the adhesion that takes place when two microstructures come into contact, and it has been intensively studied within the MEMS community [3.14]-[3.17]. It is suggested to be mainly caused by capillary, Van der Waals, electrostatic and chemical forces, all of which are very strong for the size of MEMS devices [3.16]-[3.17]. A Veeco Instruments WYKO interferometer was used to measure the tip deflection of 100μm and 50μm long

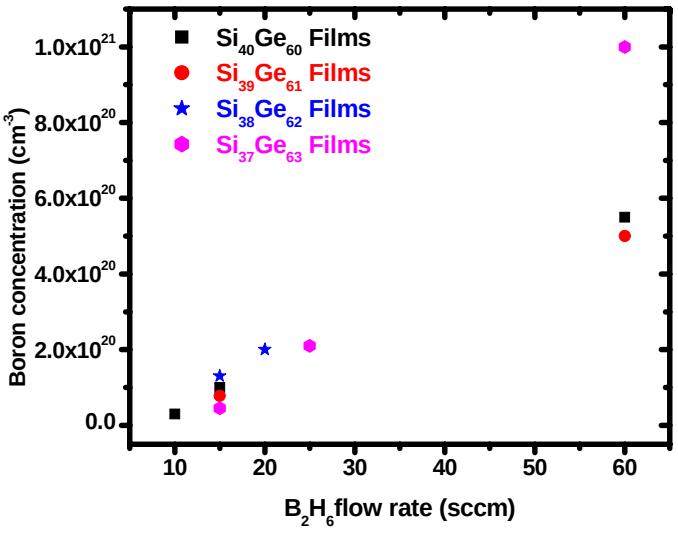
beams to determine the strain gradient. The strain gradient is calculated using linear elastic beam theory resulting in ***equation 3.1***

$$\varepsilon = \frac{1}{\rho} = \frac{2 \times deflection}{Length^2} \qquad (\textbf{\textit{equation 3.1}})$$

The main assumption of this equation is that strain changes linearly through the thickness of the film, so that the film thickness does not affect the strain gradient. For this particular study, this assumption can be justified since the structural p+ $Si_{1-x}Ge_x$ films were deposited relatively thin (0.7μm) in order to reduce the cost. In general, the grain structures of polycrystalline films are not uniform throughout the films' thickness, so that the films' thickness often affects their strain gradient. At the nucleation site, the grains are small and disorganized into small islands of seeds. But as the films become thicker, the grain sizes get bigger and the microstructure of the films becomes more columnar [3.13],[3.18]-[3.19] (**figure 3.5**). A thorough study on the effect of poly p+$Si_{1-x}Ge_x$ film microstructure on strain gradient was recently performed by *C. Low* using BCl_3 as the boron doping gaseous source. These new findings confirmed the observation that thicker p+$Si_{1-x}Ge_x$ films will have lower strain gradient compared to thin p+$Si_{1-x}Ge_x$ films since the film microstructure is more uniform throughout the film in the case of thicker films [3.13].

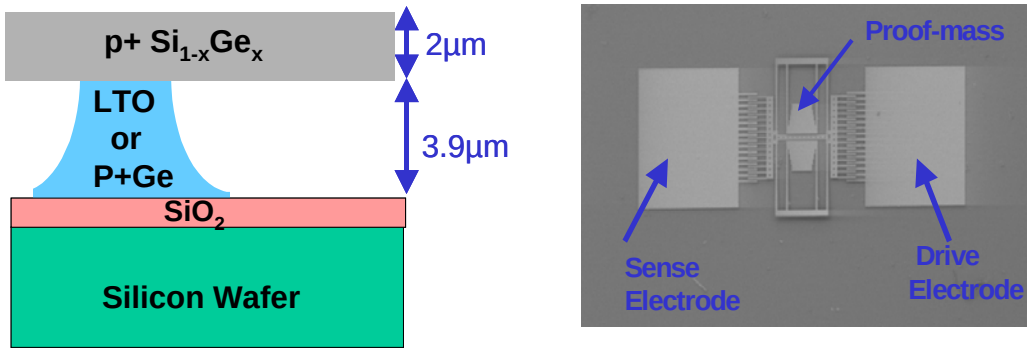


(a)



(b)

Figure 3.3: Boron concentration *vs.* B_2H_6 flow rate for **(a)** sacrificial p+ Ge films deposited by LPCVD at 350°C and 300 mTorr, with GeH_4 flow rate = 170 sccm **(b)** structural poly-$Si_{1-x}Ge_x$ films deposited by LPCVD at 425°C and 400 mTorr, GeH_4 flow rate = 45 sccm, SiH_4 flow rate = 115 sccm.



(a) **(b)**

Figure 3.4: **(a)** Schematic cross-section of cantilever beam used to determine the strain gradient in structural poly-$Si_{1-x}Ge_x$ films. **(b)** SEM micrograph of fabricated comb-drive test structure.

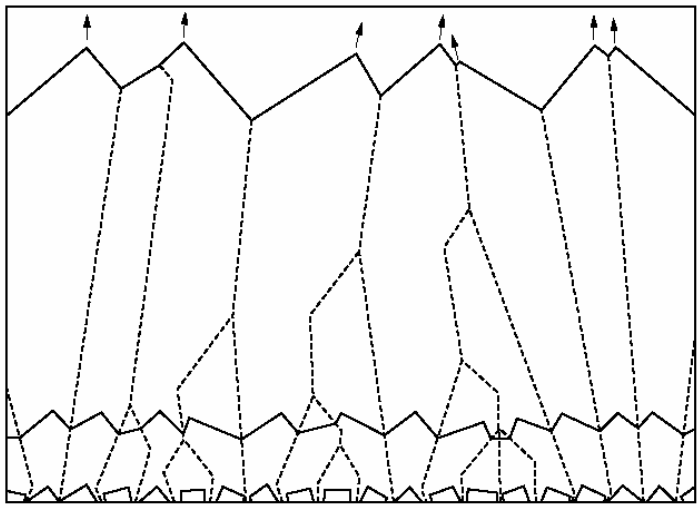


Figure 3.5: Van-der drift construction through thickness, grain size and grain orientation evolution resulting from growth velocity anisotropy during film thickening [3.19].
Note that as the p+ $Si_{1-x}Ge_x$ films become thicker, their microstructure become more columnar and uniform, thus resulting in a lower strain gradient compared to thinner films.

3.3. Results

3.3.1. p+ Ge as a sacrificial material

3.3.1.1. Processing parameters

Poly-Ge can be etched very selectively to Si, $Si_{1-x}Ge_x$, SiO_2 and Si_3N_4 in a heated solution of hydrogen peroxide, and therefore can be used as a sacrificial material instead of oxides, thus eliminating the need to protect CMOS electronics during the MEMS release etch [3.20]-[3.21]. Ideally, a sacrificial material needs to be deposited at a high rate to reduce the cost of the technology, then with minimal surface roughness to allow easy subsequent lithographical steps. Finally, a sacrificial material needs to be rapidly and controllably etched selectively to the structural material. In this chapter, the deposition rate, etch rate (in a 30% H_2O_2 solution maintained at 90°C), and surface roughness of p+ Ge films as a function of diborane (B_2H_6) flow rate have been investigated. **Figure 3.6** shows that the deposition rate increases with B_2H_6 flow rate, saturating at 45 sccm. This is due to the fact boron atoms increase the deposition rate. For the case of polycrystalline silicon films, Kamins explained this increase by the addition of a parallel deposition mechanism to that of undoped films. The normal deposition is attributed to the decomposition of silane on surface silicon atoms, while the additional parallel mechanism is believed to be the decomposition of silane on deposited boron surface atoms which acts as a catalyst. According to this model, the deposition rate of the parallel reaction path should be proportional to the number of surface boron atoms, $N_B^{2/3}$ [3.3].

Figure 3.6 further reveals that the p+ Ge films' etch rate in a 90ºC heated solution of H_2O_2 increases linearly with the B_2H_6 flow rate. This is most likely due to the fact the

B atoms enhances the kinetics reaction that occurs during release of the p+ Ge films. Etching of p+ poly Ge in H_2O_2 results in films that steadily darken and become more "glassy" (exhibiting reflective properties and coloration common to thin oxides) the longer the films are etched [3.22]. It was observed that the grain boundary sites of polycrystalline films etch faster than other sites of the films. **Figure 3.7** presents a cross-sectional profile of p+ sacrificial Ge as peroxide attacks the films starting at the grain boundaries. A possible reason for this phenomenon is that germanium atoms are more readily attacked by peroxide (H_2O_2) at the grain boundaries (or by any wet chemical that etches germanium).

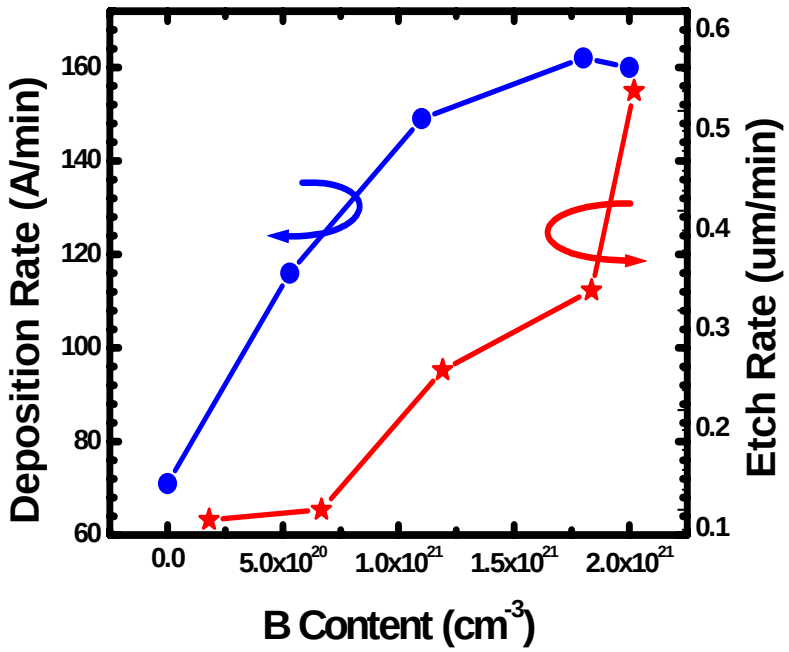
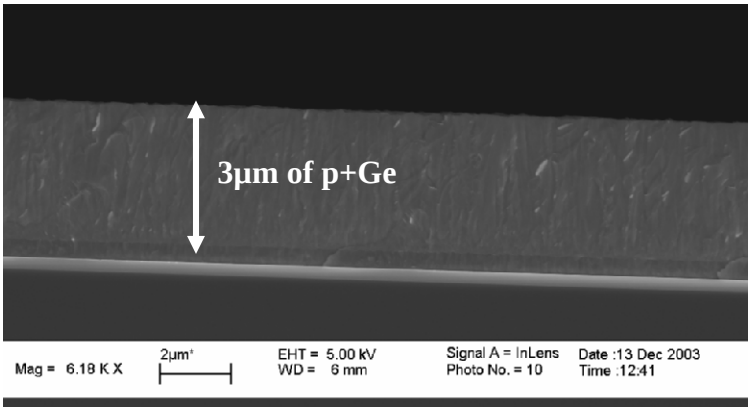
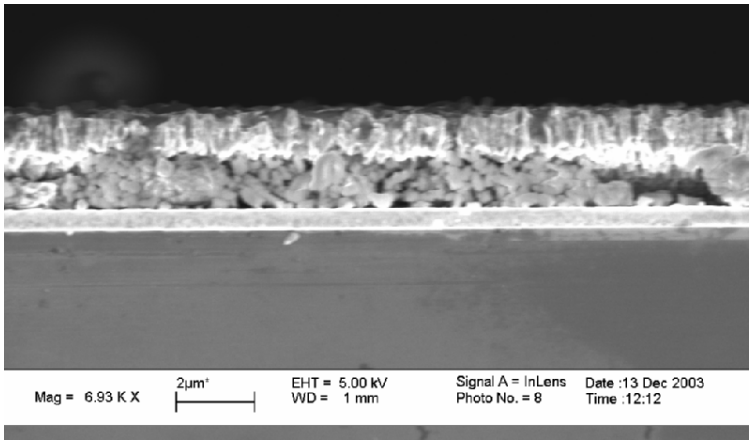


Figure 3.6: Deposition and etch rates for Ge as a function of B_2H_6 flow rate. The Ge films were deposited by LPCVD at 350°C and 30 mTorr, with GeH_4 flow rate = 170 sccm.



(a)



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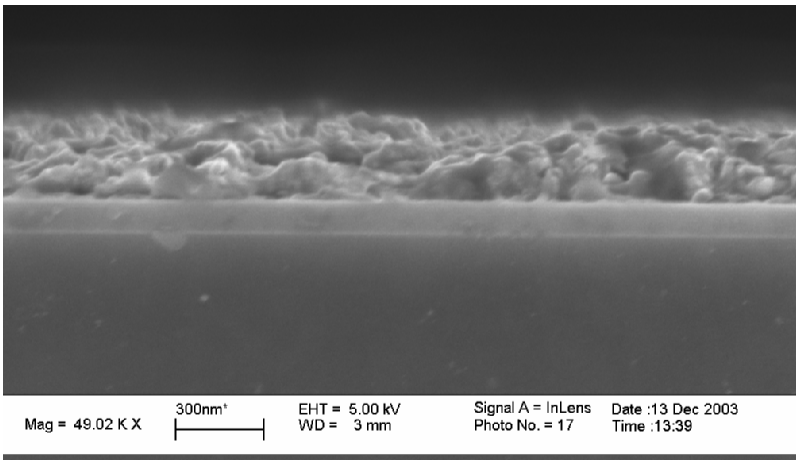


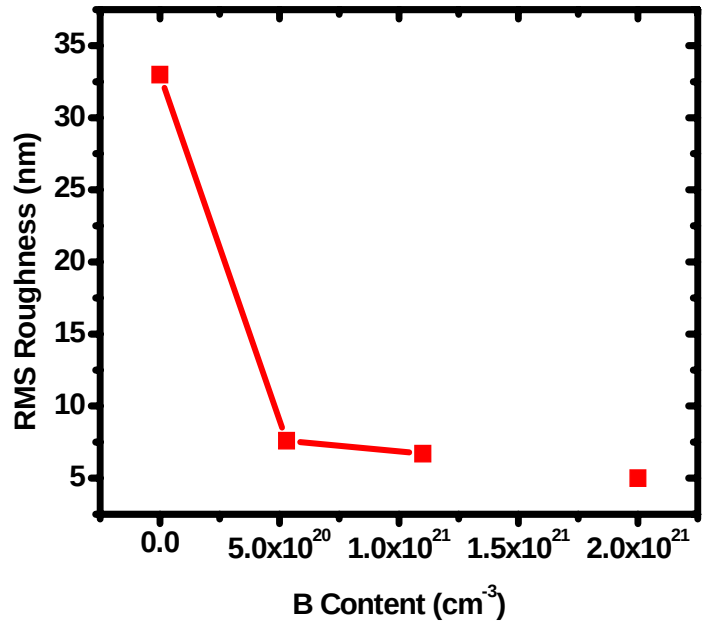
(c)

Figure 3.7: SEM micrograph showing the evolution of polycrystalline sacrificial p+ Ge film as it is being etched in a 90ºC heated solution of H_2O_2.
(a) No etching **(b)** after 15 seconds **(c)** after 45 seconds.

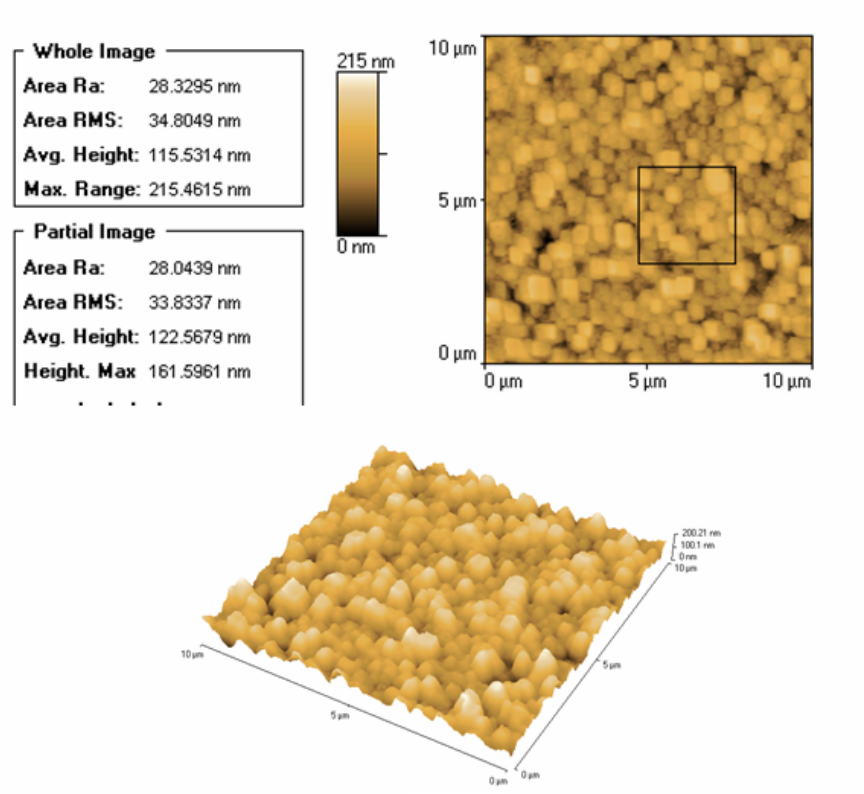
3.3.1.2. Surface Roughness

The RMS surface roughness of the p+ Ge films was characterized with an Atomic Force Microscope (AFM) which uses a RF bias of 500 kHz operating on tapping mode. This mode operates by scanning a tip attached to the end of an oscillating cantilever across the sample surface. The amplitude of oscillation ranges from 20 nm to 100 nm, with the frequency near the resonant peak of the cantilever. The tip lightly taps the surface, altering the oscillatory motion as the scanner moves across the surface. By adjusting the vertical position of the scanner to maintain a constant RMS signal of oscillation, a surface is imaged. The oscillation is measured by a laser positioned by the user to reflect signal into a photodiode detector [3.23].

AFM results indicate that the more heavily boron doped Ge films are smoother (**Figure 3.8a**). This observation is consistent with the higher deposition rate of the heavily boron doped Ge films resulting in a smaller average grain size (see **Figure 3.9** for X-TEM analysis results). Because of the enhancement in deposition rate that accompanies an increase in [B], the atoms adsorbed on the wafer surface have less time to migrate to the lowest energy crystal sites before the next atoms arrive. Clearly, a high level of *in-situ* boron doping is desirable for increasing process throughput, etch rate, and film smoothness of sacrificial Ge films. **Figure 3.8b** presents a close-up topography view of heavily doped Ge films ([B] ~5.3×10^{20} cm^{-3}) deposited at 350°C, revealing a very uniform roughness throughout the surface scanned.



(a)



(b)

Figure 3.8: **(a)** Ge film surface roughness, as a function of B_2H_6 flow rate. The Ge films were deposited by LPCVD at 350°C and 300 mTorr, with GeH_4 flow rate = 170 sccm. **(b)** Close-up image showing surface roughness of films deposited with GeH_4 flow rate = 15 sccm.

3.3.1.3. Film Microstruture

The microstructure of the p+Ge sacrificial films was characterized using transmission electron microscopy (TEM). Cross-sectional TEM specimens were prepared using standard laboratory practices by *TEM Analysis Inc.* [3.24]. TEM micrographs show that the p+ Ge microstructure evolved from polycrystalline to amorphous as the boron doping concentration increases **(Figure 3.9**). Electrical measurements were performed to verify this, and as expected from the TEMs of the polycrystalline films, the films' resistivity drops with increasing [B] (**Figure 3.10**). However, it shows an abrupt increase at ~2×10^{21} cm^{-3} since that deposition condition leads to an amorphous film. Because of the enhancement in deposition rate that accompanies an increase in [B], the atoms adsorbed on the wafer surface have less time to migrate to the lowest energy crystal sites before the next atoms arrive. Thus, as [B] increases, the degree of disorder in the film increases (average grain size decreases – see **Figure 3.9**), until ultimately the film is deposited in amorphous form at very high levels of [B]. The same phenomenon has been reported for the case of p+ polycrystalline silicon film [3.3].

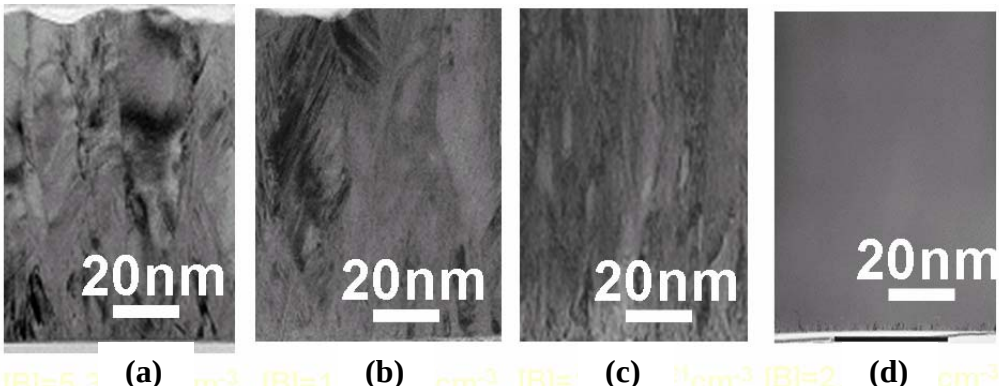


Figure 3.9: X-TEM micrographs of p+ Ge films reported in **Figures 3.6** and **3.8**; (a) B= $5.3x10^{20}cm^{-3}$, (b) B= $1.1x10^{21}cm^{-3}$, (c) B= $1.8x10^{21}cm^{-3}$, (d) B= $6.2x10^{21}cm^{-3}$. Average grain size becomes smaller as [B] increases because of the increase in deposition rate due to increase in [B] content in p+ Ge films (Courtesy of TEM Analysis).

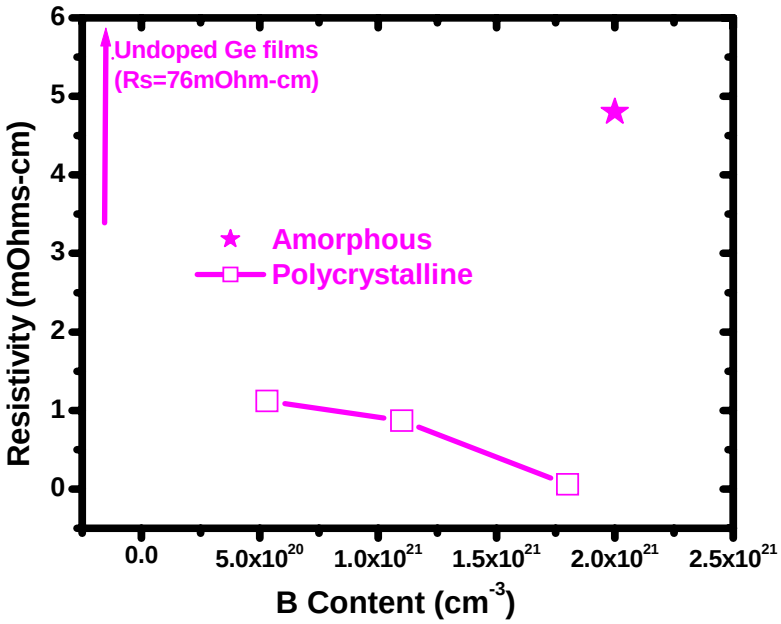


Figure 3.10: Resistivity of p+ Ge films as a function of B concentration. The Ge films were deposited by LPCVD at 350°C and 300 mTorr, with GeH_4 flow rate = 170 sccm.

3.3.2. p+ $Si_{1-x}Ge_x$ structural material

3.3.2.1. Electrical properties

The electrical properties of the p+ $Si_{1-x}Ge_x$ structural films have been studied. In general, the films need to have low resisitivity in order to reduce voltage drop during actuating and/or sensing of the $Si_{1-x}Ge_x$ MEMS devices. Overall, a resistivity $\rho<10m\Omega$ is desired, but specific values would depend on targeted applications.

Using a regression analysis methodology that accounts for all the measured data ($Si_{1-x}Ge_x$ runs provided in **Appendix A**), the best-fitting surface plots for conductivity, residual stress, and strain gradient as a function of B and Ge content were generated.

Since each data point corresponds to a single $Si_{1-x}Ge_x$ deposition run, it was not possible to generate points throughout the regression analysis plots because of the high cost of these runs. The fitting confidence of these plots is 99.5% for conductivity, 89% for residual stress, and 81% for strain gradient.

As expected, the film conductivity of p+ $Si_{1-x}Ge_x$ structural films increases with increasing [B] and [Ge] due to increase in hole mobility and dopant activation (**Figure 3.11**) [3.25]-[3.26]. The etch rate in heated H_2O_2 solution was found to be independent of B content (~2.5nm/min)**.**

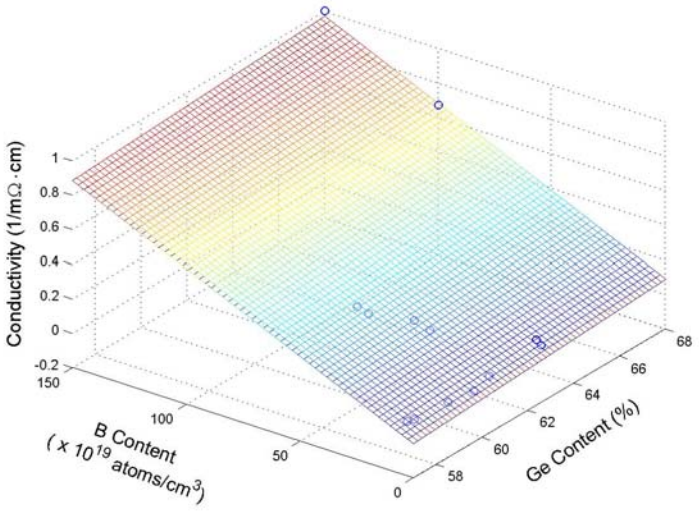


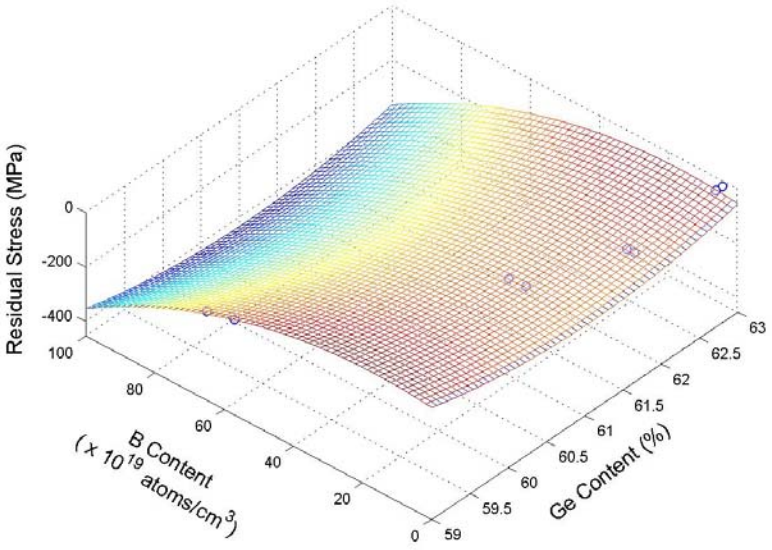
Figure 3.11: Conductivity *versus* boron concentration, for structural poly-$Si_{1-x}Ge_x$ films deposited by LPCVD at 425°C and 400 mTorr, GeH_4 flow rate = 45 sccm, SiH_4 flow rate = 115 sccm.

3.3.2.2. Mechanical properties

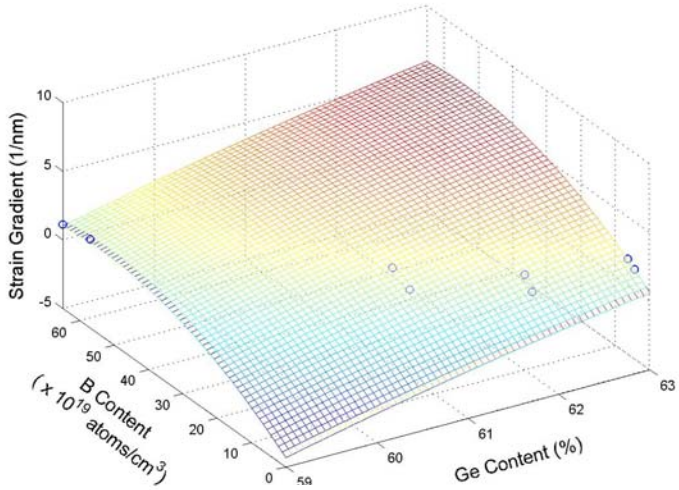
Ideally, a low tensile stress and strain gradient is critical for optimal fabrication of MEMS devices since the film' stress can severely affects the device performance. For instance, a compressive stress would lead to a bad thermal insulation of bolometers and severe strain gradient can produce undesirable deflection in accelerometer devices.

The intrinsic stress reflects the internal structure of a material and is less clearly understood than the thermal stress which often dominates [3.18]. Several phenomena may contribute to the intrinsic stress (σ), making its analysis more complex. Intrinsic stress depends on thickness, deposition rate (locking in defects), deposition temperature, ambient pressure, method of preparation, type of substrate used (lattice mismatch), and incorporation of dopants during growth process. For the case of doped poly-silicon, the atomic or ionic radius of a dopant or substitutional site determines the positive or negative intrinsic stress [3.18]. With boron doped poly-silicon (an atom smaller than silicon), the film is expected to be tensile ($\sigma > 0$), while with phosphorus doping (an atom larger than silicon), the film is expected to be compressive ($\sigma < 0$) [3.18].

For the case of $Si_{1-x}Ge_x$ films studied in this work, the average residual stress decreases (becoming less tensile or more compressive), (**Figure 3.12a**) while the strain gradient decreases considerably, as the boron content increases (**Figure 3.12b**). For $4\times10^{20}cm^{-3}$ boron concentration, the strain gradient is 1.1×10^{-3} μm^{-1}, which corresponds to a vertical deflection of 1.4 μm at the tip of a 50μm-long 2μm-thick cantilever beam. **Figure 3.13** shows SEM images revealing the severe deflection of the p+ poly-$Si_{1-x}Ge_x$ structural films upon release. Two test structures included in this mask set are presented. **Figure 3.13a** presents a circular comb-drive test structure often used for fatigue study of polycrystalline films and **Figure 3.13b** presents cantilever beam test structures used for curvature measurement, which was used to compute the film's strain gradient. Several approaches for reducing the strain gradient have been published elsewhere (and have been summarized in chapter 1 of this thesis). These include the use of a multilayered $Si_{1-x}Ge_x$ films [3.27] pulsed excimer-laser annealing (ELA) [3.28] or flash lamp annealing.

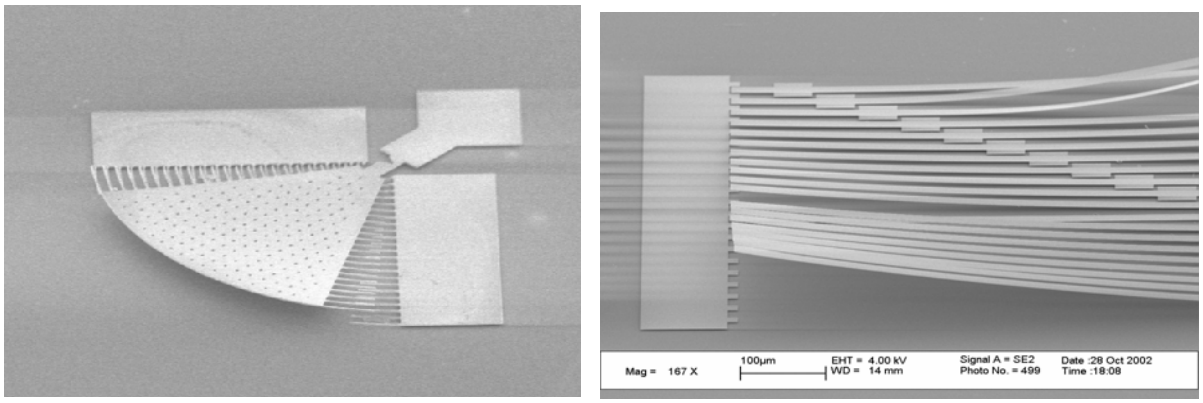


(a)



(b)

Figure 3.12: Regression function analysis plots of **(a)** average residual stress, and **(b)** strain gradient of boron-doped poly-$Si_{1-x}Ge_x$ structural films, as a function of boron content.



(a) **(b)**

Figure 3.13: SEM images showing severe strain gradient in As-deposited of boron doped poly-$Si_{1-x}Ge_x$ structural films **(a)** test structure used for fatigue study **(b)** cantilever beams test structures used for strain gradient characterization.

3.3.2.3. Boron segregation at the grain boundaries

Hall-Effect measurements were performed to compare the dopant activation level in two p+ $Si_{0.37}Ge_{0.63}$ films: Sample A ($[B]_A \cong 4.5\times10^{19}$ cm^{-3}, σ_A = -22 MPa) and Sample B ($[B]_B \cong 9.7\times10^{20}$ cm^{-3}, σ_B = -79 MPa).

The basic physical principle underlying the Hall-Effect is the Lorentz force. When an electron moves along a direction perpendicular to an applied magnetic field, it experiences a force acting normal to both directions and moves in response to this force and the force affected by the internal electric field (**Figure 3.14**). We assume that a constant current *I*, flows along the x-axis from left to right in the presence of a z-directed magnetic field. Electrons subject to the Lorentz force initially drift away from the current line toward the negative y-axis, resulting in an excess surface electrical charge on the side of the sample. This charge results in the Hall voltage V_H, of magnitude equal to *IB/qnd*, where *I* is the current, *B* is the magnetic field, *d* is the sample thickness, and *q* (1.602 x 10^{-19} C) is the elementary charge and *n* the concentration of the majority carriers [3.29].

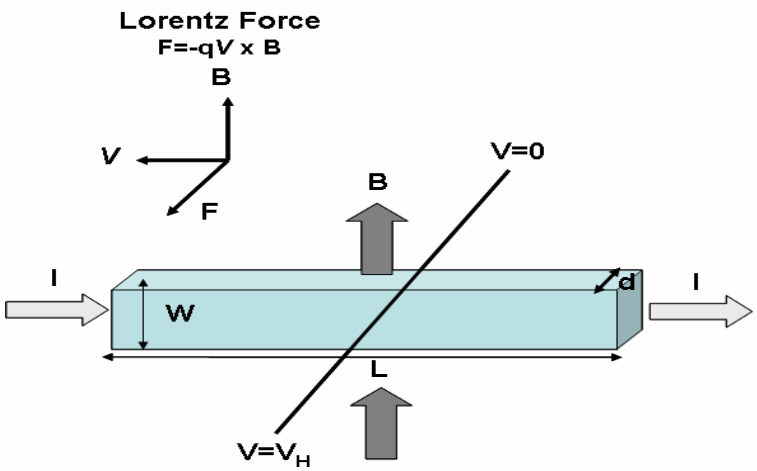
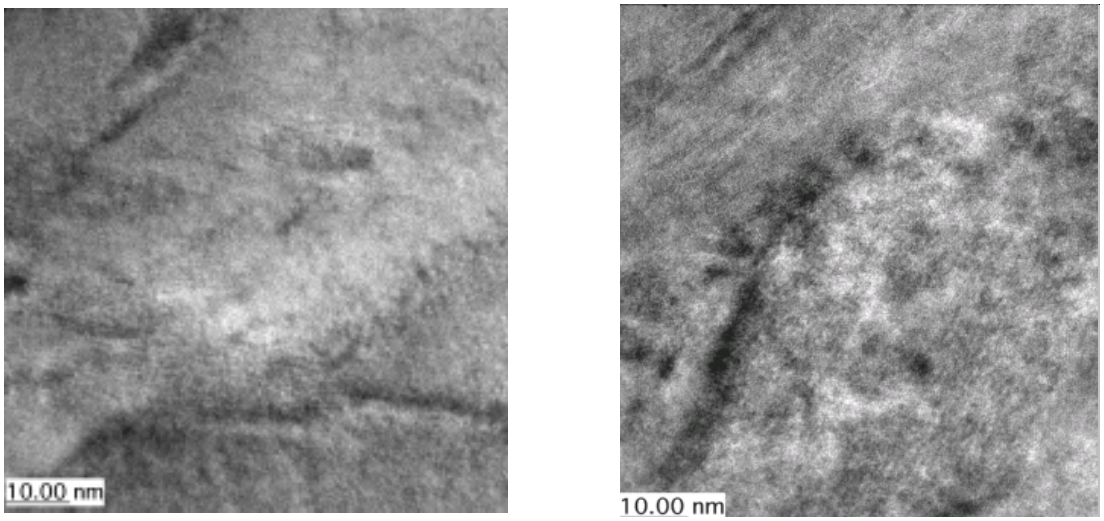


Figure 3.14: Hall-Effect experiment showing a slab of silicon, where and E-field is applied parallel while a B field is applied perpendicular to the sample.

The results from the Hall measurements are summarized in **Table 3.1**, and they indicate that all of the boron dopants are activated in Sample A, whereas they are not in the case of Sample B. Therefore, the observation that the p+ $Si_{1-x}Ge_x$ structural films become more compressive at very high B concentrations is likely due to segregation/clustering of boron atoms (**Figure 3.15**).

Table 3.1: Results from Hall-Effect measurement of dopant activation on Sample A (low compressive residual stress) verse Sample B (high residual stress).

	Sample A	**Sample B**
[B] (cm^{-3})	$4.5x10^{19}$	$9.7x10^{20}$
% dopant activation	100%	55%
Residual stress	-22MPa	-79MPa



(a) **(b)**

Figure 3.15: Transmission Electron Microscopy of **(a)** Sample A and **(b)** Sample B. There is a concentration of texture at the grain boundaries of sample B as compared to Sample A, what would indicate clustering of boron atoms at the grain boundaries.

3.3.2.4. XRD results

Due to the large strain gradient, which causes the released structures to bend up (out of plane), it was not possible to operate the fabricated comb-drive test structures in order to obtain measurements of the mechanical quality factor (Q) for this study. Q values of ~20,000 at 19 kHz resonant frequency have previously been reported for very heavily doped (~[B] > 6×10^{20} cm^{-3}) poly-$Si_{0.38}Ge_{0.62}$ films [3.30]. The Q was found to increase with post-deposition annealing (RTA) temperature**.** To investigate possible causes for this change, a similar annealing process was performed on doped poly-$Si_{0.38}Ge_{0.62}$ films for one minute in N_2 at various temperatures (450^{o}C to 600^{o}C) followed by Hall measurements. Hall measurement results did not indicate a significant increase in dopant activation with annealing, which would suggest that excess (non-ionized) boron atoms remain.

XRD analyses of both as-deposited and furnace annealed p+ $Si_{1-x}Ge_x$ films were also performed using a generalized focusing difractometer with a fixed incident angle (alpha) 7 degree. The XRD step scans of the poly-$Si_{0.38}Ge_{0.62}$ films were each found to exhibit singular peaks corresponding to planes (111), (220) or (110) and (311) characteristics of a material with the diamond-cubic crystal structure. The results show that the as-deposited film has a weak (111) texture, which changes to a strong (110) texture after a rapid thermal annealing treatment (**Figure 3.16)**. At the same time, weak (311) peaks are seen. The diffraction peaks for the annealed films were significantly larger and narrower, indicating a larger average grain size as well. Thus, it seems that the improvement in Q with annealing is attributable to an improved microstructure, rather than a reduction in segregated B dopants atoms. On the other hand, the XRD results do

not indicate a clear correlation between the intensity of each orientation and the annealing temperature.

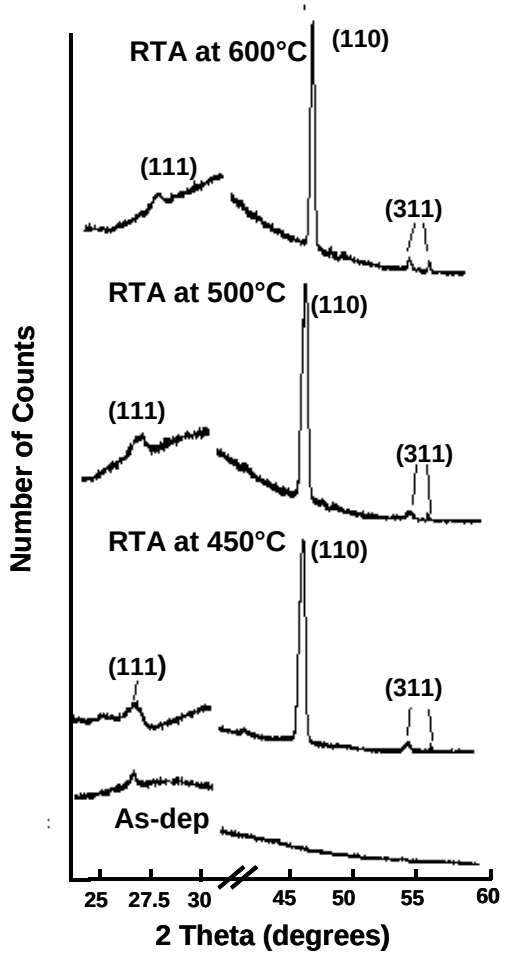


Figure 3.16: XRD results of as-deposited as well as annealed p+ $Si_{1-x}Ge_x$ films at different RTA (Rapid Thermal Annealing) temperatures. RTA was performed in a N_2 ambient.

3.3.3. Codiffusion between p+$Si_{1-x}Ge_x$ and p+Ge

A prior research study has reported a phenomenon of germanium-boron codiffusion in VLSI ultrashallow $Si_{1-x}Ge_x$/Si interface. This study reveals that an excess of vacancies created during the initial structural change causes a rapid Ge-B codifusion in p+ poly-Ge films, as well as drastically affecting the Ge-Si intermixing [3.8].

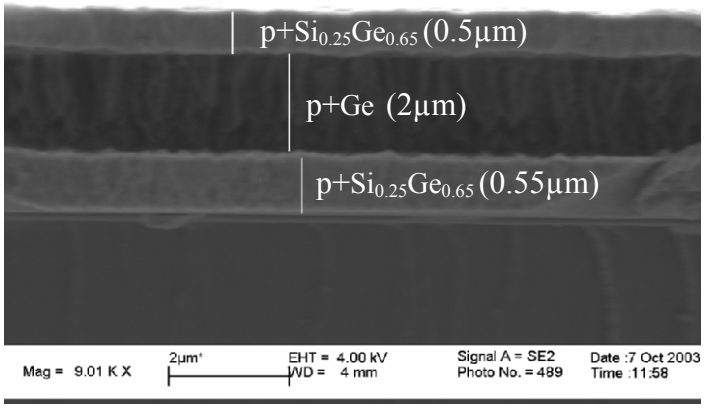
In this work, a short loop experiment was performed to determine how critical is this codiffusion phenomena in the case of high Ge content ([Ge] > 65%) and heavily boron doped ([B] > $7x10^{-19}cm^{-3}$) $Si_{1-x}Ge_x$ films used as the MEMS structural layer.

On two oxidized silicon test wafers, tri-layer films made of p+$Si_{0.25}Ge_{0.65}$/p+Ge/ p+ $Si_{0.25}Ge_{0.65}$ and of p+$Si_{0.25}Ge_{0.65}$/i-Ge/ p+ $Si_{0.25}Ge_{0.65}$ have been deposited using LPCVD at 450ºC for the p+ $Si_{1-x}Ge_x$ films and 350ºC for the p+ Ge films. Cross-sectional SEM schematics revealing the thickness of the tri-layer films is shown in **Figure 3.17**. The tube was opened and vacuum was broken in between the three depositions in order to simulate what happens in the real fabrication process flow of the SiGe micromachined structures, where p+ $Si_{1-x}Ge_x$ is used as the structural layer and p+ Ge the sacrificial layer.

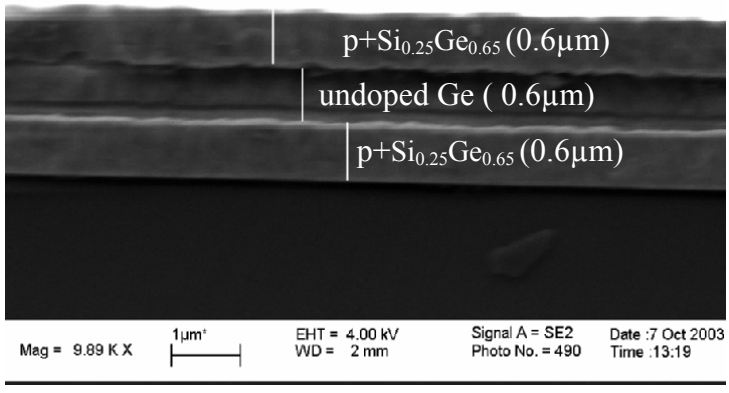
Furnace annealing was performed in a nitrogen ambient at 550ºC for five hours, then Secondary Ion Mass Spectrometry (SIMS) and Spreading Resistance Profiling (SRP) analysis were performed in order to evaluate the total number of dopants, and the total number of activated dopants, respectively. Boron codiffusion at the p+$Si_{1-x}Ge_x$\p+Ge interface was compared to that at the p+$Si_{1-x}Ge_x$\i-Ge interface. This was to evaluate if a doped Ge sacrificial layer is more efficient to alleviate the codiffusion phenomenon as compared to an undoped Ge sacrificial layer.

SIMS results shown in **Figure 3.18** indicate no major change in dopants concentration between as-deposited films and annealed films for both cases. This is most likely due to the fact that the tri-layer was deposited after breaking the tube vacuum, so that a thin native oxide layer present at the interface of the films would act as a barrier for this codiffusion mechanism.

This result indicates that B-Ge codiffusion phenomenon is negligible in SiGe micromachined technology. Therefore, it is still advantageous to dope the Ge sacrificial layer in order to increase the films deposition rate, thus reducing the cost of the technology.



(a)



(b)

Figure 3.17: Schematic SEM cross-sections of the tri-layer films deposited.
(a) Tri-layer made of p+$Si_{0.25}Ge_{0.65}$/p+Ge/ p+ $Si_{0.25}Ge_{0.65}$
(b) Tri-layer made of p+$Si_{0.25}Ge_{0.65}$/i-Ge/ p+ $Si_{0.25}Ge_{0.65}$

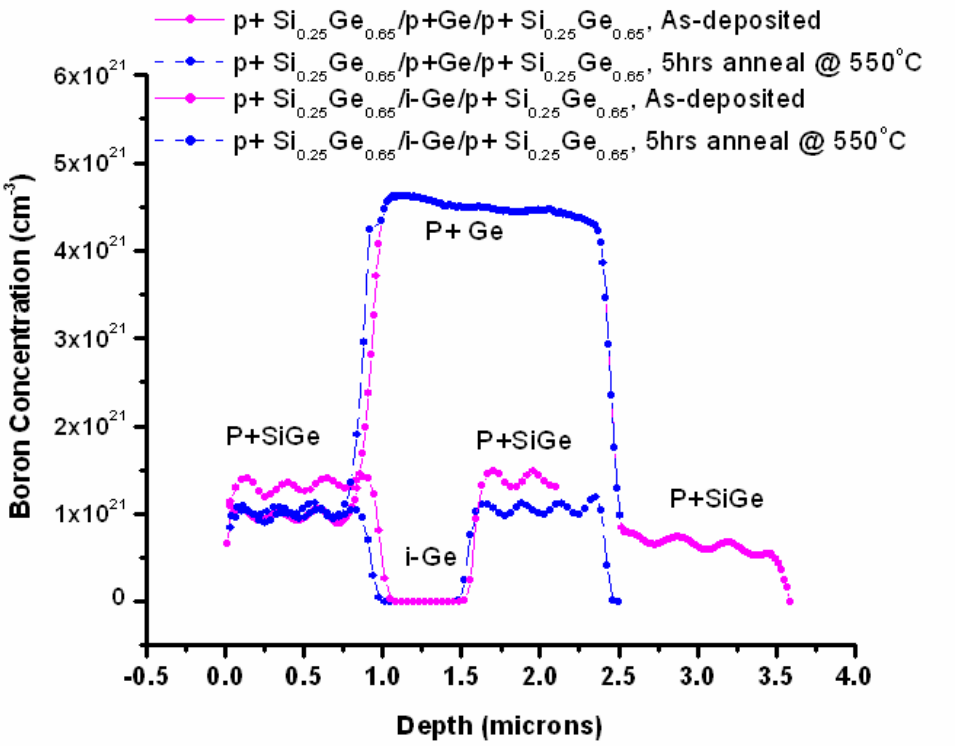


Figure 3.18: Boron concentration verse depth using SIMS analysis (accuracy with 2-3%) For the two tri-layers: p+$Si_{0.25}Ge_{0.65}$/p+Ge/ p+ $Si_{0.25}Ge_{0.65}$ and p+$Si_{0.25}Ge_{0.65}$/i-Ge/ p+ $Si_{0.25}Ge_{0.65,}$ Boron concentration is compared for As-deposited films and annealed films.
Note that the slight shift observed is accounted through the 2.5% accuracy of SIMS analysis.

3.4. Summary

Experimental results show that heavy B doping is beneficial for increasing the deposition and etch rates, as well as for reducing the surface roughness of p+ poly-Ge sacrificial films. However, structural poly-$Si_{1-x}Ge_x$ films become more compressive, and show a slight increase in strain gradient, with increasing B content. Analytical models fit to the experimental data for conductivity, residual stress, and strain gradient have been generated as a guide for co-optimization of B and Ge content. Heavy B doping does not increase the etch rate of poly-$Si_{1-x}Ge_x$ structural films in peroxide, as long as the Ge content is below 65%, so that high etch selectivity can be maintained for a Ge sacrificial material.

XRD results performed in as-deposited and annealed p+$Si_{1-x}Ge_x$ samples show that an improvement in microstructure with annealing temperature would lead to an improvement in Q observed in low frequency comb-drive devices, rather than a reduction in segregated B dopants atoms. And lastly, B-Ge codifusion at the p+$Si_{1-x}Ge_x$/p+Ge interface was found to be negligible compared to that observed in VLSI ultrashallow $Si_{1-x}Ge_x$/Si interface given the fact that a thin layer of oxide is always present at the p+$Si_{1-x}Ge_x$/p+Ge interface to prevent this codiffusion phenomenon.

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Chapter 4

Applications of $Si_{1-x}Ge_x$ MEMS Technology

4.1. Nanogap SiGe RF MEMS filter

4.1.1. Introduction

The wireless communication market continues to require the miniaturization of conventional discrete components in order to decrease the size and power requirements for portable cellular phones. Therefore, an enabling integrated MEMS technology aims to deliver miniature integrated solutions that include filters, switches, oscillators, phase shifters and tunable capacitors for the replacement of discrete components such as quartz crystals.

In recent years, extensive research and significant progress has been made in fabrication techniques and testing of high frequency MEMS resonators for filtering applications [4.1]-[4.4]. A simple model circuit of a resonator is shown in **Figure 4.1** and it is represented by a resistor, inductor and capacitor connected to the substrate by some

feedthrough capacitances. The device is electrostatically driven by a drive voltage V_d, and capacitively sensed through a sense current i_s [4.5]. In the lumped model below, C_{eq} represents the equivalent capacitance of the filter, L_{eq} the equivalent inductance and R_{eq} the motional resistance. In the high frequency domain, the motional resistance R_{eq}, is the most critical component of this lumped model; reducing R_{eq} makes possible the transfer of radio frequencies with low insertion losses [4.6]-[4.7].

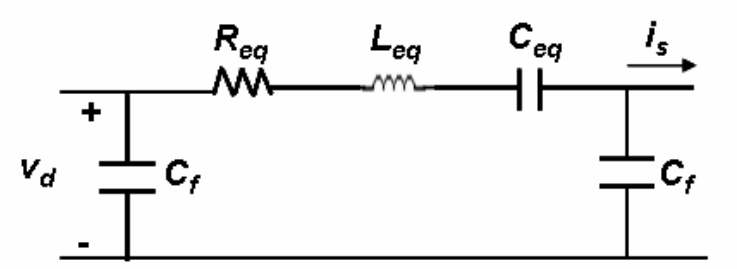


Figure 4.1: A schematic picture for the lumped model of a MEMS filter that includes an equivalent resistance (R_{eq}), capacitance (C_{eq}), inductance (L_{eq}) and some feedthrough capacitances (C_f).

4.1.2. Motivation for Ge blade process

To extend the resonant frequency of micromechanical filters to the Gigahertz range, the gap spacing between the electrodes and the resonator needs to be shrunk in parallel plate electrostatic transducers. Based on theoretical calculations, gap sizes less than 100nm are required in order to reduce the motional resistance R_{eq} to the desired 50Ω range, thus minimizing the device insertion loss. Novel fabrication methodologies have been previously demonstrated to achieve ultra small gaps in the sub-micrometer range. E-

beam lithography and sacrificial side-wall spacer techniques were used to achieve lateral electrode to resonator gaps of 100nm [4.8]-[4.9].

Photoresist (PR) ashing was reported to be a convenient and useful technique to extend the lithography line width limit for sub-100nm and E-beam lithography [4.10]. It is generally used in the semiconductor industry to define nanometer features that are below what can be achieved with conventional optical lithography [4.11]-[4.12].

In this short loop study, SiGe MEMS technology was used along with photoresist ashing technique for the definition of Ge blades to yield nanometer gaps necessary to reduce the motional resistance of electrostatically transduced RF MEMS filters [4.13]-[4.14]. Polycrystalline silicon-germanium films doped with boron replaced poly-silicon as the structural layer, while poly-germanium films were used as the sacrificial layer, rather than silicon dioxide. Electrostatic transducer structures were successfully fabricated with nanometer gaps dimensions ranging from 50nm to 150nm.

4.1.3. Short loop fabrication process details

Starting with a silicon substrate (**Figure 4.2a**), 1μm of silicon dioxide (SiO_2) was deposited in order to electrically isolate the fabricated structures from the substrate (**Figure 4.2b**). Sacrificial in-situ doped p+ poly-Ge was then deposited in a conventional Low Pressure Chemical Vapor Deposition (LPCVD) furnace at 350ºC, using GeH_4 as the gaseous Ge source**,** and B_2H_6 as the dopant gas (**Figure 4.2c**). 2000 angstroms of Low Temperature Oxide (LTO) was deposited to serve as a hard mask (**Figure 4.2d**), followed by photoresist spin-on and optical lithography (**Figure 4.2e**). Several focus-exposure tests were consecutively performed to determine the optimum condition for achieving a

minimal PR line width of 0.5µm. Based on this line width, a proper calibration of the PR ashing rate (using oxygen plasma) was performed both vertically and laterally to push down the minimum line-width dimension to sub-100nm nanometer scale without significantly affecting cross-wafer uniformity. This step was followed by RIE anisotropic etching of sacrificial p+ Ge using Cl_2 and HBr based chemistries (**Figure 4.2f**). The polycrystalline p+$Si_{0.35}Ge_{0.65}$ structural layer was deposited at 450ºC and 400mtorr using SiH_4, GeH_4 and B_2H_6 gases in a LPCVD furnace (**Figure 4.2g**), followed by CMP (chemical mechanical polishing) for film planarization (**Figure 4.2h**). The Ge sacrificial film was removed in a 90ºC heated solution of H_2O_2, followed by a dip in 100:1 diluted solution of hydrofluoric acid to undercut the oxides, creating gaps with dimensions ranging from 50 to 150nm (**Figure 4.3i**).

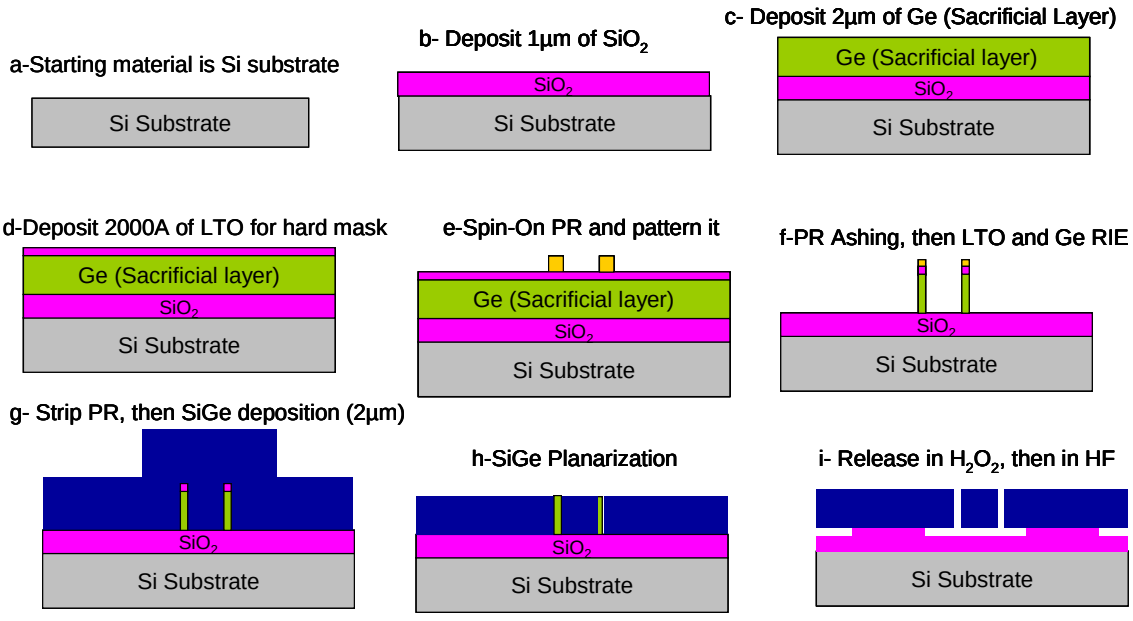
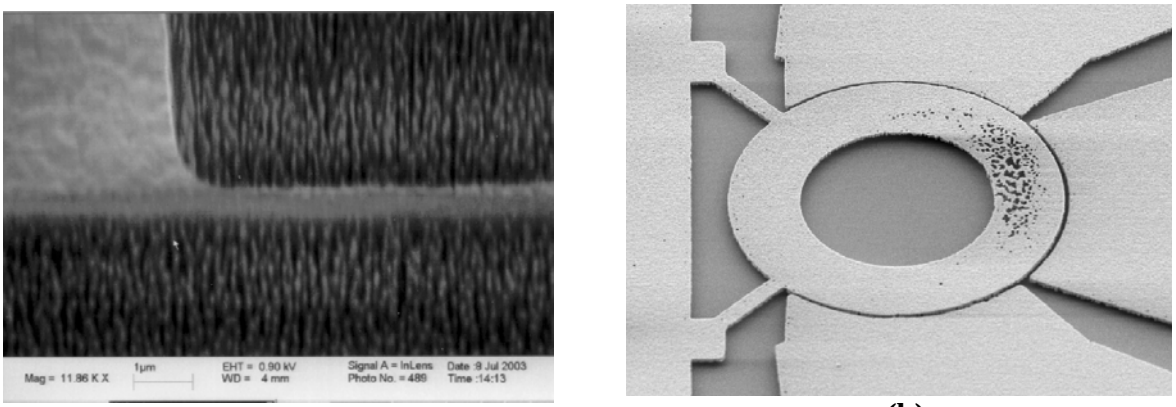


Figure 4.2: Fabrication process flow of RF MEMS filters using Ge ashing technique.

4.1.4. Experimental results

4.1.4.1. Polymer residues after DRIE of p+Ge films

The main challenge encountered in the fabrication process of the SiGe MEMS filters was photoresist redeposition (**Figure 4.3**), which occurred during the stringent deep reactive ion etch process step of p+ Ge layer to achieve 20:1 aspect ratio Ge blades. Photoresist residues were eliminated by dipping the wafers for 1minute into a diluted solution of hydrofluoric acid of 100:1 after the RIE process step.



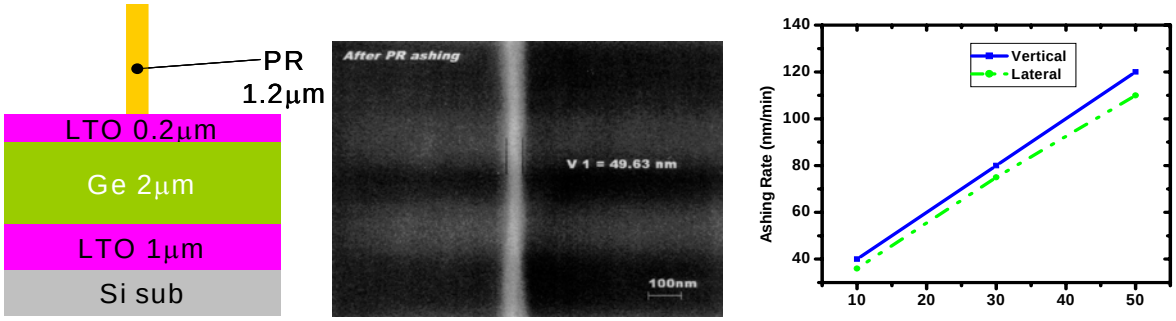
(a) **(b)**

Figure 4.3: **(a)** Closed view of Photoresist residues observed after deep reactive ion etch process of p+ Ge films **(b)** Example of RF MEMS filter device that encountered the photoresist residues problem on the resonating ring mass.

4.1.4.2. Nanometer lateral gaps

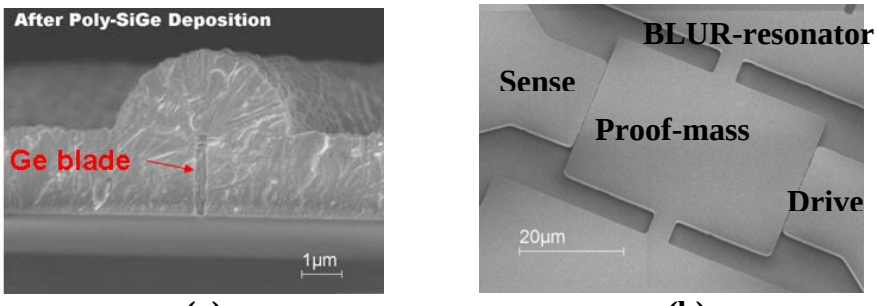
Line widths ranging from 50nm to 150nm were obtained after photoresist ashing (**Figure 4.4a** and **b**). **Figure 4.4c** shows that as the ashing rate is linearly proportional to the ashing power, and that the vertical ashing rate is twice as fast as the lateral ashing rate. LTO was then etched directionally in a standard RIE tool with CF_4 chemistry, followed by the removal of PR. Using oxide as the hard mask, p+ poly-Ge was etched to achieve vertical side-walls with a standard poly-silicon etch procedure.

The fabrication process flow of the RF MEMS filters was further optimized by *Takeuchi et al* [4.14] and *Quevy et al.* [4.15] and the fabricated poly-$Si_{1-x}Ge_x$ electrostatic MEMS filters yielded quality factor $Q \sim 4800$ and radio frequency resonance of 24MHz. **Figure 4.5a** and **b** presents respectively a side view of the Ge blade after $Si_{1-x}Ge_x$ deposition, and a top view of a fabricated working Bulk Longitudinal Resonator.



(a) **(b)** **(c)**

Figure 4.4: **(a)** Cross section of structure prior to resist ashing and **(b)** SEM top view of a PR line obtained after ashing, **(c)** linear relation between ashing rate and ashing power.



(a) **(b)**

Figure 4.5: **(a)** Side-view of Ge blade after $Si_{1-x}Ge_x$ deposition **(b)** Top view of a fabricated working Bulk Longitudinal Resonator.

4.2. SiGe floating inertial sensor system

4.2.1. Introduction

Electrostatic forces are commonly used for actuation of micromachined devices such as inertial sensors, RF MEMS filters and MEMS optical mirrors. However, in all these devices, a mechanical connection exists between the actuated part and the substrate, thus providing a path for mechanical losses through the connecting suspension tethers or through the anchoring points.

For inertial sensor applications such as advanced automotive systems or robotics, vibratory gyroscopes which detect the Coriolis force have been widely studied and commercialized within the MEMS community during the past fifteen years. But these devices often suffer from accuracy, power consumption and performance drift [4.16]-[4.20]. A floating electromechanical system (FLEMS) gyroscope was proposed to improve the performance of conventional vibrating angular rate sensor systems, since it has the ability of achieving higher resolution/accuracy due to the frictionless mechanical pin joints inherent to the device. A FLEMS device is an inertial sensor composed of a charged proof mass electrostatically suspended within an opposite charged base suspension [4.21]-[4.22]. Such a free disk sensor system has many potential applications, such as: (1) accelerometers with online dynamic characteristics tuning, (2) gyroscopes with a spinning disk to measure the precession of the disk induced by the Coriolis force and (3) microfluidic mixers and pumps frictionless bearings for micro-motors. In practice, sensing can be achieved through either electrical (electrostatic sensing) or optical means (light reflection/refraction detection).

The concept of electrostatic levitation for an inertial sensor device has been previously reported using silicon as the structural material, but the dimensions of the device have not been scaled down to the sub-micrometer range to be compatible with VLSI-CMOS based technology [4.23]-[4.24]. In this work, the lateral dimensions of the device have been aggressively scaled to reduce the operating voltages and to facilitate monolithic integration with the sense and drive electronics. Heavily doped p-type poly-$Si_{1-x}Ge_x$ was used for the structural layer as well as the sensing and driving electrode layers to enable modular (Post-CMOS) integration and minimize parasitics in the electronics, and low-temperature-deposited SiO_2 (LTO) films were used as the sacrificial layers.

4.2.2. Benefits

The most attractive feature of an electrostatic FLEMS inertial sensor device is the fact the proof-mass is not structurally linked to the suspension, thus avoiding the usual dominating mechanical losses caused by anchor loss and material damping. Some of the resulting benefits include:

- lower power consumption
- improvement in achievable drift due to the elimination of suspension torques
- reduction of the residual stress effects on the system dynamics achieved from the elimination of the mechanical suspension
- decrease of mechanical wear, fatigue or short-circuiting
- reduction of electric and mechanical parasitics such as electronic noise
- large operating range of temperatures and of accelerations

Additionally, the electrostatic suspension of the FLEMS device provides a high fidelity self-centering system due to the electrostatic forces that are inversely proportional to the square of the gaps between the proof-mass and the suspension electrodes. An acceleration of 45K-g gives approximately 1μN force on a representative $10\mu m^3$ system. Only small charges on the order of femto-Coulombs are needed to comfortably self-center the proof-mass. Thus, in principle, it is possible to operate at very high accelerations without worrying about mechanical stops interfering with operation [4.21].

4.2.3. Experiments details

4.2.3.1. Overview

A CMOS compatible poly-$Si_{1-x}Ge_x$ surface micromachining process flow was developed to enable the fabrication of the FLEMS sensor device. SiGe MEMS technology was used to pave the way for the on-chip monolithic integration of the sensor system with the ASIC electronics for the reduction of parasitics. In the future, vacuum encapsulation using a well established CMOS compatible packaging technology will be needed to reduce air damping effects and to maximize the capacitively induced current that is to be sensed.

To implement the suspended electromechanical sensor system, the sensor has been designed to have at least three degrees of freedom (DOFs), one translational, one tilt, and one rotational. Positional control is achieved in both the axial and radial directions with three sets of actuators: one set on the lower electrode plane, a second set the upper electrode plane, and the last set on the sides of the floating disk.

4.2.3.2. Mask layout design

Based on a design study of the sensing and control scheme for the FLEMS gyroscope, a four-mask fabrication process was developed. The layout of a FLEMS device is shown in **Figure 4.6a**, followed by a view of the entire test chip layout in **Figure 4.6b** which includes FLEMS devices of various sizes and test structures for measurement of stress, strain gradient, resistivity, and Young's modulus.

The first mask defines the base layer or ground-plane layer (**SiGe0**) placed on an insulator layer and is used to form the lower electrodes to control the levitation of the floating mass vertically (z-direction) as well as its tilt radial excursion. The bottom electrode located in the center will inject an AC signal that other electrodes will use to sense gap changes as the disk moves.

The second mask (**SiGe1**) is used to define the structural layer (proof-mass) as well as the side electrodes. The side electrodes are anchored on an insulating layer (LTO) and are used to control the motion of the floating mass laterally (x-y direction). Based on such a scheme, the active conductive layer of the gyroscope sensor will be composed of **SiGe1** (defining the levitated disk) separated from the other conductive layers by two vertical gaps. It is critical to point out that a low-strain-gradient poly $Si_{1-x}Ge_x$ structural film is required to minimize the out-of-plane curvature of the released proof-mass, which would result in a degraded capacitive coupling to the side electrodes. Approaches to achieving low strain gradient poly-$Si_{1-x}Ge_x$ films investigated in this study are discussed in section 4.2.3.5.

A third (dark field) mask (**Anchor**) is used to define the regions where the top electrodes will be anchored, thus preventing the electrodes from being completely released along with the levitated disk during the final release etch step in hydrofluoric acid. Finally, the fourth mask (**SiGe2**) is used to define the top electrodes to control the vertical levitation, the tilt and the angular motion along with the bottom electrodes.

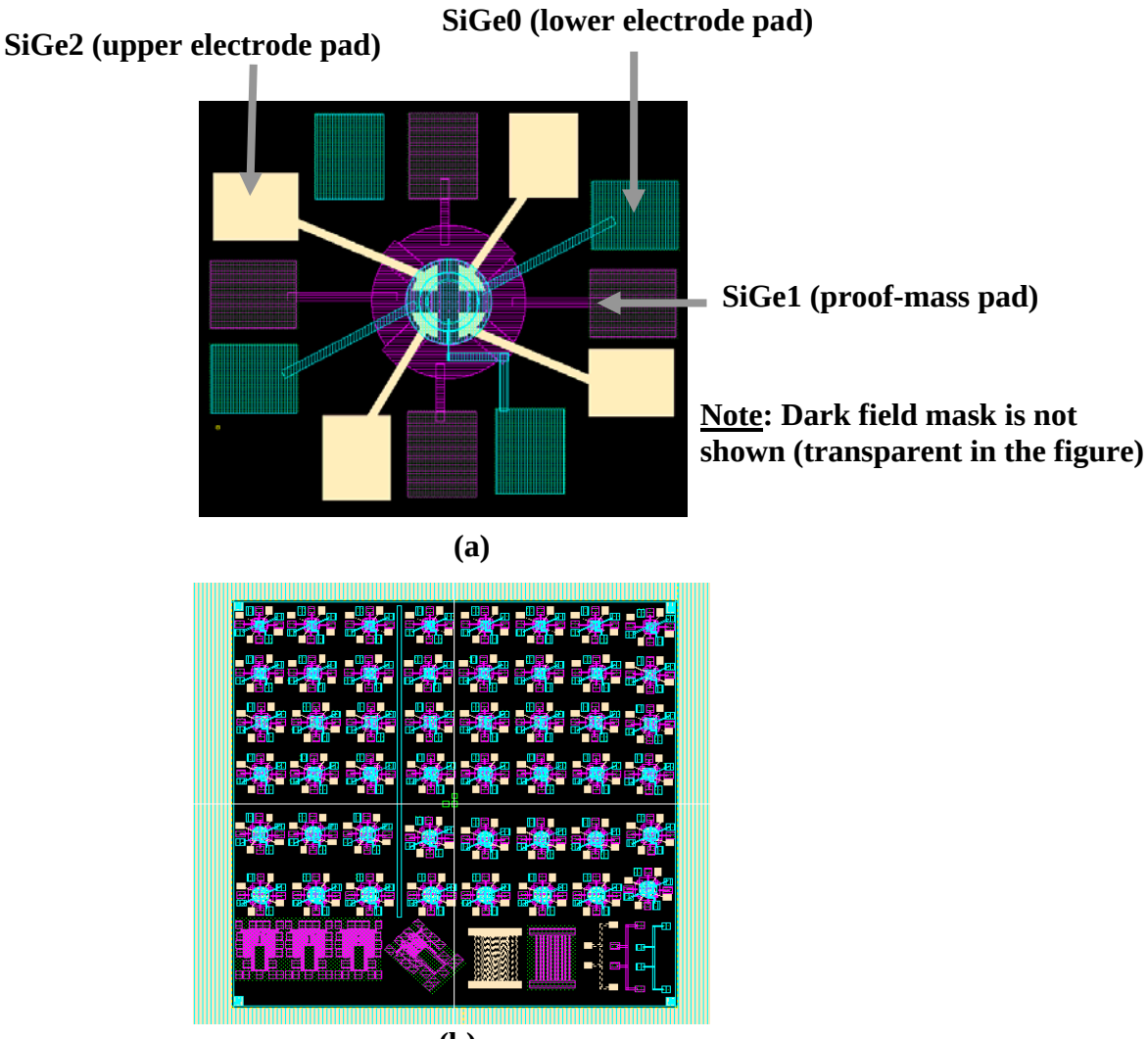


Figure 4.6: **(a)** FLEMS sensor layout **(b)** View of test die containing devices of various sizes and test structures (for measurement of stress, strain gradient, resistivity, and Young's Modulus).

4.2.3.3. Design considerations

In general, in order to achieve high precision and accuracy in the measurement of angular rate acceleration (or Coriolis acceleration), a micromachined gyroscope device needs to have a large angular momentum, *i.e.* a large system mass and/or a sizeable device is required [4.18]-[4.22],[4.25]-[4.26]. Also, minimal lateral gap dimensions (often in the nanometer-scale range) are needed in order to achieve sufficiently high capacitively induced current for electrostatic actuation and/or sensing.

Keeping these two design constraints in mind, the central design of the FLEMS sensor device uses a 100μm disk radius. The dimensions were chosen to avoid the severe effect of a strain gradient that is a hurdle for larger sized devices. The minimum line width achievable with the i-line projection lithography stepper in the UC Berkeley Microfabrication Laboratory is ~0.6 μm, thus it was chosen for the minimal lateral gap dimension in of the FLEMS device in order to achieve optimal capacitive sensing. An array of devices with radii varying from 100 μm to 200 μm (in 20 μm increment) and lateral gad dimension varying from 0.6 μm to 1 μm was included in the final layout (see **Figure 4.6b** and **Table 4.1**). Finally, three lower electrodes, four side electrodes and four upper electrodes were adopted to achieve control over the maximum number of degrees of freedom.

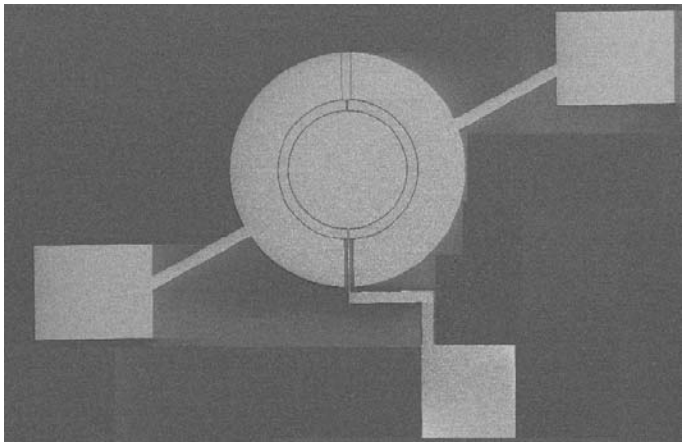
Table 4.1: Summary of the array of FLEMS devices designed in the mask layout (Note that all the dimensions are in micrometers).

Disk_radius	Radius of top electrode	Radius of center electrode	Inner radius of ring electrode	Outer radius of ring electrode
100	60	50	70	100
120	80	60	80	120
140	100	70	90	140
160	120	80	100	160
180	140	90	110	180
200	160	100	120	200

4.2.3.4. Device fabrication process

The fabrication process flow of the FLEMS sensor follows a conventional multi-layer surface-micromachining process with one ground plane layer, two structural layers and two sacrificial layers. The fabrication procedure starts with a conductive p-type silicon wafer starting substrate coated with 1μm-thick Low Temperature Oxide (LTO) and 0.2μm-thick silicon nitride which serves to protect the LTO from being etched during the structural layer release etch in hydrofluoric acid vapor.

An electrically conductive polycrystalline $Si_{1-x}Ge_x$ film (heavily doped with boron) is then deposited and patterned to form the ground plane or lower electrodes. The deposition parameters as well as a scanning electron micrograph of the lower electrodes are shown in **Figure 4.7**. The thickness of this layer was measured to be 0.7μm, and its resistivity was measured to be 5mΩ-cm, and the RMS surface roughness was ~200Angstroms. It is important to note that a high surface roughness would be necessary to prevent the floating disk from getting stuck down on the lower electrodes during the release wet etch process. **Figure 4.8a** shows a schematic cross-section of the device after definition of the first poly-$Si_{1-x}Ge_x$ layer.



Deposition process parameters of poly-SiGe0 layer:

T_{dep} = 425°C
Pressure = 600 mTorr
SiH_4 flow rate = 120 sccm
GeH_4 flow rate = 45 sccm
BCl_3 flow rate = 12 sccm

Figure 4.7: SEM micrograph of patterned 1st poly-Si_xGe_{1-x} layer, defining the lower electrodes.

After the definition of the lower electrodes, 2μm of LTO is deposited at 400°C, followed by chemical mechanical polishing (CMP) to planarize the surface of the LTO (**Figure 4.8b**). The purpose of this CMP step is twofold: first, it reduces the topography of the surface to ease subsequent lithography steps; second, it allows the formation of a uniformly thick vertical gap between the lower electrode and the proof mass. A short-loop CMP study was performed by *Dae-Won Ha* (**Figure 4.9**) [4.27], and these results were optimized for use in the FLEMS sensor fabrication process.

The most critical step in the fabrication process flow is to deposit of the structural poly-$Si_{1-x}Ge_x$ film (4μm targeted thickness) with low residual stress and low strain gradient for the levitated disk and side electrodes. Using a low strain gradient recipe, the structural layer was deposited (process conditions provided in **Table 4.2**). The deposition rate turned out to lower than expected. Using a Dektak surface profilometer, the film thickness was found to be 3.6μm. To determine the residual stress, wafer curvature measurements were made using a Tencor FLX-2320 instrument before and after the poly-$Si_{1-x}Ge_x$ deposition (with the backside $Si_{1-x}Ge_x$ film removed). The film was patterned into cantilever-beam test structures and then released using a timed etch in a concentrated (49%) solution of hydrofluoric acid (HF). Then, a Veeco Instruments WYKO interferometer was used to measure the tip deflection of 100μm long beams to determine the strain gradient. The measured stress was -51MPa, and the measured strain gradient was $1x10^{-4}\mu m^{-1}$, which is unacceptably high for the floating gyroscope application. Given the thermal budget constraint for post-CMOS integration of MEMS devices reported in [4.28], a furnace annealing step was performed at 400°C for 4 hours in an attempt to reduce the out-of-plane deflection of the film [4.29]; this resulted in a

reduction of the film strain gradient from $1x10^{-4}\mu m^{-1}$ to $5x10^{-5}\mu m^{-1}$. Increasing the annealing time did not show anymore improvement. A design of experiments (DOE) described in Section 4.2.3.5 was performed to determine the optimal process conditions to further reduce the poly-$Si_{1-x}Ge_x$ film strain gradient to the desired value of $1x10^{-5}\ \mu m^{-1}$. This experiment optimized the deposition of an additional (highly compressive) upper layer of poly-$Si_{1-x}Ge_x$ to cancel out the bending-up stress gradient [4.30]-[4.31].

Continuing the fabrication procedure, standard lithography and DRIE etch process were performed to pattern the proof-mass layer (**SiGe1**) to achieve critical lateral gap dimensions of 0.6μm (**Figure 4.8c**). Then a 2μm-thick LTO film was deposited and planarized using CMP (for the same reasons mentioned above), leaving 1μm of LTO over the structural poly-$Si_{1-x}Ge_x$ to define the upper vertical gap separating the disk from the upper electrodes (**Figure 4.8d**). Next, a 100nm-thick layer low temperature SiN layer was deposited at 400°C and patterned using a dark-field mask to define the anchoring points for the upper electrodes (**Figure 4.8e**). This step is necessary to ensure that the top electrodes are not completely released during the final wet etch process. The final deposition step is used for the formation of the upper poly-$Si_{1-x}Ge_x$ electrodes (**SiGe2**), for axial and radial control of the FLEMS device. It is critical that this final conductive layer also has low residual stress and low strain gradient in order to avoid severe out-of-plane deflection that could compromise actuation using the upper electrodes. This layer was finally patterned to define the upper electrodes (**Figure 4.8f**) and a timed etch process in HF vapor was used to release the disk (**Figure 4.8g**).

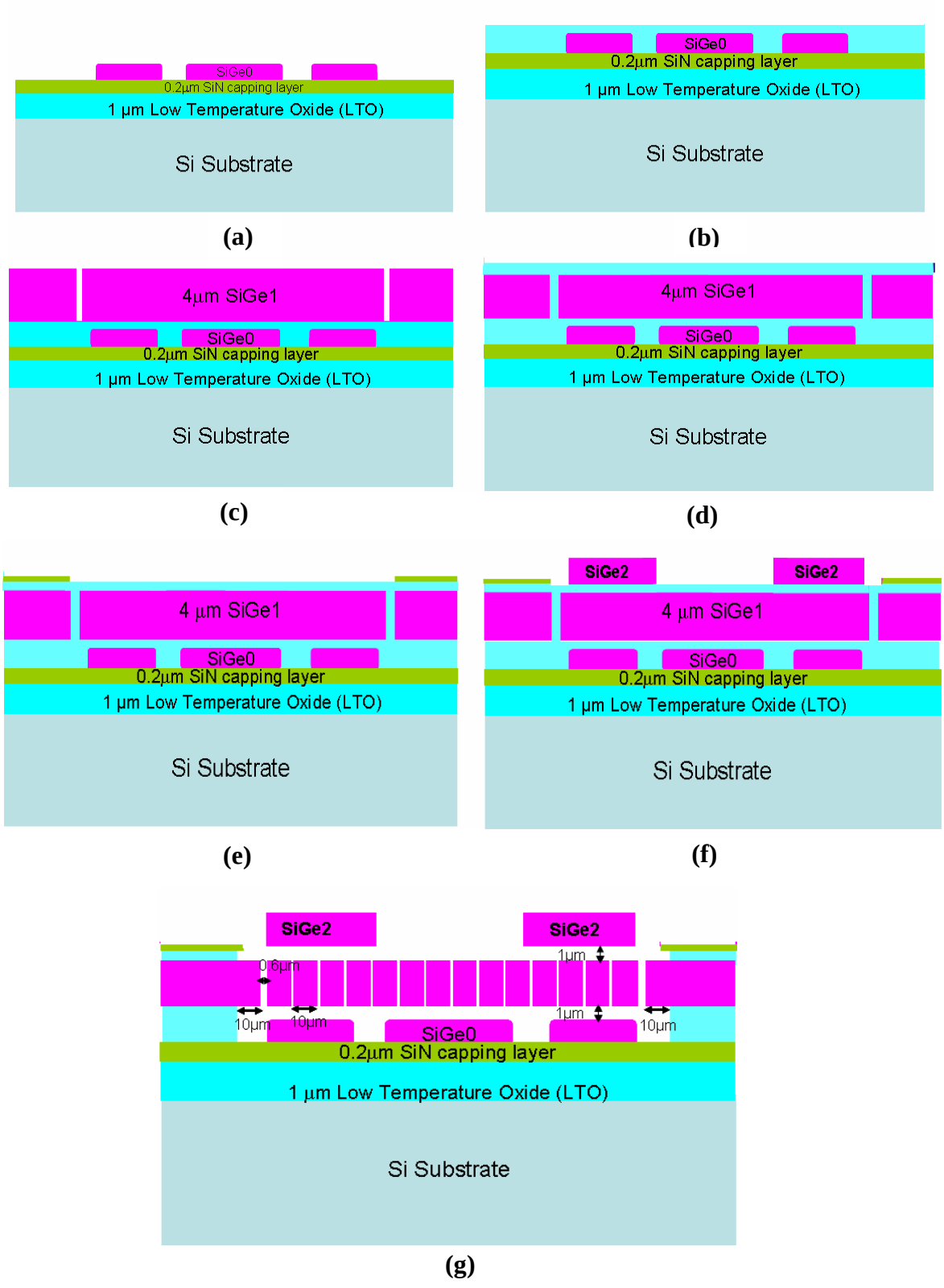


Figure 4.8: Cross sectional schematics (not drawn to scale) to illustrate the FLEMS device fabrication process. Etch holes in levitated mass are not shown in **(a)-(f)** for simplicity.

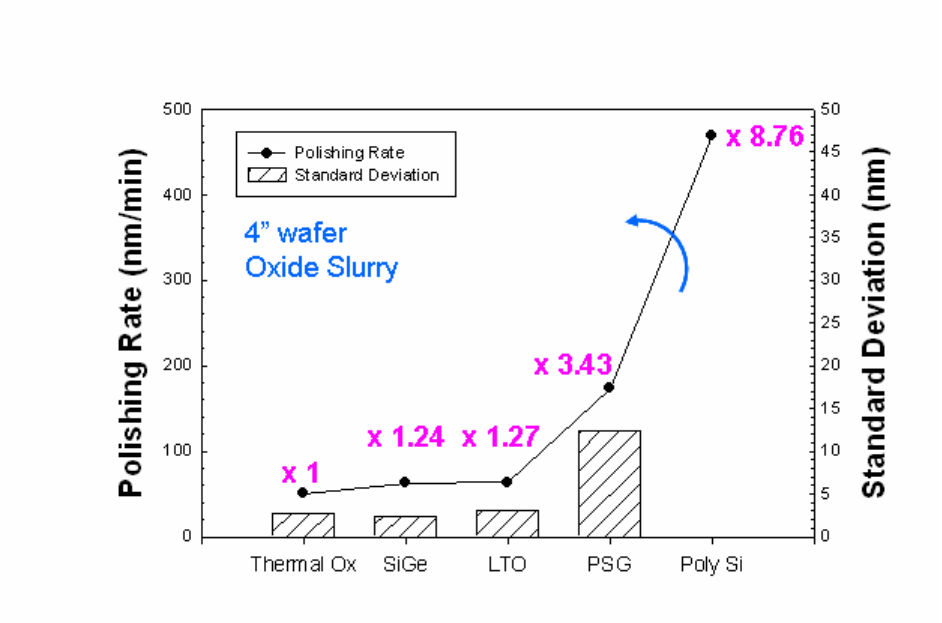


Figure 4.9: CMP polishing rate of various materials used in semiconductor/MEMS processing [4.27].

Table 4.2: Deposition process parameters of SiGe0 (ground plane layer) and SiGe1 (proof-mass levitated layer).

Lower SiGe layer for the definition of ground plane								
Pressure (mTorr)	Temp. (deg C)	SiH4 (sccm)	GeH4 (sccm)	BCl3 (sccm)	Dep rate (A/min)	Thickness (um)	Stress (MPa)	Resistivity (mOhm-cm)
600	425	120	45	12	62	0.7	N/A	5
Middle SiGe layer for the definition of levitated disk								
Pressure (mTorr)	Temp. (deg C)	SiH4 (sccm)	GeH4 (sccm)	BCl3 (sccm)	Dep rate (A/min)	Thickness (um)	Stress (Mpa)	Resistivity (mOhm-cm)
600	410	105	70	12	60	3.6	-51	1.2

4.2.3.5. Structural layer process module development

Deposition process development is necessary to attain $Si_{1-x}Ge_x$ films with low residual stress and low strain gradient at CMOS compatible temperatures (<450°C). As reported earlier, a single 4μm-thick p+ $Si_{0.4}Ge_{0.6}$ layer deposited at 410°C was found to have a strain gradient of $1x10^{-4}$ μm^{-1}. This strain gradient implies a vertical tip deflection of 0.5μm for a 100μm-long cantilever, what is unacceptable for the FLEMS sensor

application (100 μm disk radius). Therefore, the use of a bilayer structural film was investigated to reduce the strain gradient to an acceptable level (1 to $2x10^{-5}$ μm^{-1}). The top layer is required to be more compressive than the bottom layer in order to create a bending-down moment that cancels the bending-up moment generally seen in low-temperature deposited p+ $Si_{1-x}Ge_x$ films [4.30]-[4.31]. Higher compressive stress in the top layer can be achieved by reducing the Ge content [4.32]-[4.33] or by reducing the deposition temperature while keeping the other process parameters constant. The design of experiment parameters are presented in **Table 4.3** along with the electrical and mechanical properties of the $Si_{1-x}Ge_x$ films achieved during this short loop study. From this table, it is clear that as the GeH_4 flow rate is reduced on the top $Si_{1-x}Ge_x$ layer, the film becomes more compressive so that the bi-layer strain gradient is reduced. At a certain point, the strain gradient becomes negative, thus causing a bend-down curvature of the cantilever beams upon release.

Table 4.3: Design of Experiment Matrix for development of a bi-layer deposition procedure to achieve a low strain gradient p+$Si_{1-x}Ge_x$ structural layer.

Bottom SiGe layer of bilayer process (less compressive)										
Temp. (deg C)	SiH4 (sccm)	GeH4 (sccm)	BCl3 (sccm)	Dep rate (A/min)	Thickness(um)	Final Thickness	Stress (MPa)	Resistivity (mOhm-cm)	Deflection (um)	Strain Gradient (um^-1)
425	105	70	12	91	3.3		-51	5.1	2.2	4.40E-04
Top SiGe layer of bilayer process (more compressive)										
Temp. (deg C)	SiH4 (sccm)	GeH4 (sccm)	BCl3 (sccm)	Dep rate (A/min)	Top layer Thickness	Bilayer Thickness	Stress (Mpa)	Resistivity (mOhm-cm)	Deflection	Strain Gradient 100um beam
410	105	70	12	60	0.48	3.78	-159	6.2	2.2	4.40E-04
410	115	60	12	55	0.55	3.83	-161	3.4	1.1	2.20E-04
410	125	50	12	52	0.5	3.8	-215	3.4	0.2	4.00E-05
410	130	45	12	44	0.93	3.92	-295	3.2	0.1	2.00E-05
410	135	40	12	40	1.06	3.9	-300	3.7	-0.3	-6.00E-05

Assuming the first order approximation of the strain gradient to be linear (which is the best fitting function for the experimental data points), a plot of the effect of SiH_4/GeH_4 ratio on the p+ $Si_{1-x}Ge_x$ strain gradient was generated (see **Figure 4.11**). From this plot, one can extrapolate the point where the strain gradient is zero using

straightforward mathematical computation. The SiH_4/GeH_4 ratio that would yield the least positive strain gradient is 2.5. Experimental data shown on **Table 4.3** closely matches the predicted value extracted from **Figure 4.10.**

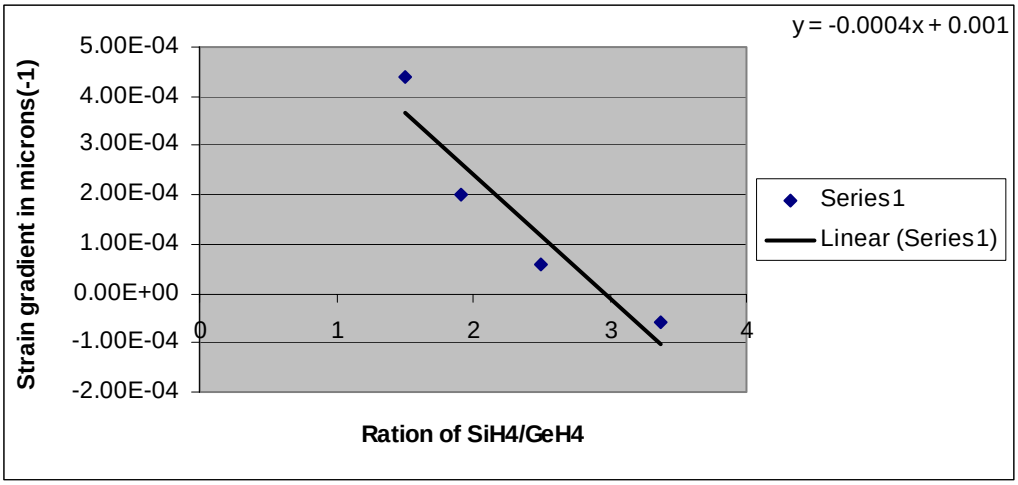


Figure 4.10: Linear approximation plot of the effect of SiH_4/GeH_4 ratio on the p+ $Si_{1-x}Ge_x$ strain gradient (data are taken from the design of experiment matrix to achieve low strain gradient films using bi-layer procedure for stress gradient cancelation).

After film deposition, the Bosch RIE process was used to etch the p+ $Si_{1-x}Ge_x$ films in the new reactive ion etcher system installed for 6" wafers. The Bosch process uses different cycles with a combination of SF_6 gas as the main etching gas and C_4F_8 for the deposition of a passivation layer on the side walls for protection. The plasma is inductively coupled at an RF of 13.56 MHz via a matching unit and coil assembly. Directional energy control is provided by a 400 kHz biasing of the cathode with a separate power supply. The etch rate for silicon film was reported to about 3μm/min (see **Table 4.4)**, but it was found to be lower for p+ $Si_{1-x}Ge_x$ (~1μm/min). This is likely due to a major difference in the density of the devices on the layout.

Table 4.4: Bosch RIE recipe for Si, Ge and $Si_{1-x}Ge_x$ to achieve high aspect ratio side walls (Courtesy of *M. Wasilik*, UC Berkeley Microlab Centura Operational Manual).

Deep Si 1A	Passivation	Etch
SF6, sccm	0	250
C4F8, sccm	300	0
time, sec	8	6
coil, watts	1200	1200
bias, watts	-	10
pulsing	-	CW
pressure, mT	100	40
cycles	500	
Recipe Type	TMGM	
Typical Use	deep silicon high AR etch	
TYPICAL RESULTS		
Etch Rate, mic/min	3.0	
% Non-Uniformity	15%	
Si:SPR220 Selectivity	75:1	
profile	90° ± 1°	

The cantilever-beam test structures were released in a concentrated solution of hydrofluoric acid followed by a critical-point dry process to prevent stiction. The best run resulted in a tip deflection of 0.1µm for a 100µm-long cantilever beam, corresponding to a strain gradient of $2x10^{-5}$µm (**Figure 4.11a**). The second best run showed out of plane positive deflection of 0.2µm in a 100µm cantilever beam, what corresponds to a strain gradient equal to $4x10^{-5}$µm (**Figure 4.11b**). And the third best run showed out of plane negative deflection of 0.3µm in a 100µm cantilever beam (films bending-down), which corresponds to a strain gradient equal to $-6x10^{-5}$µm (**Figure 4.11c**).

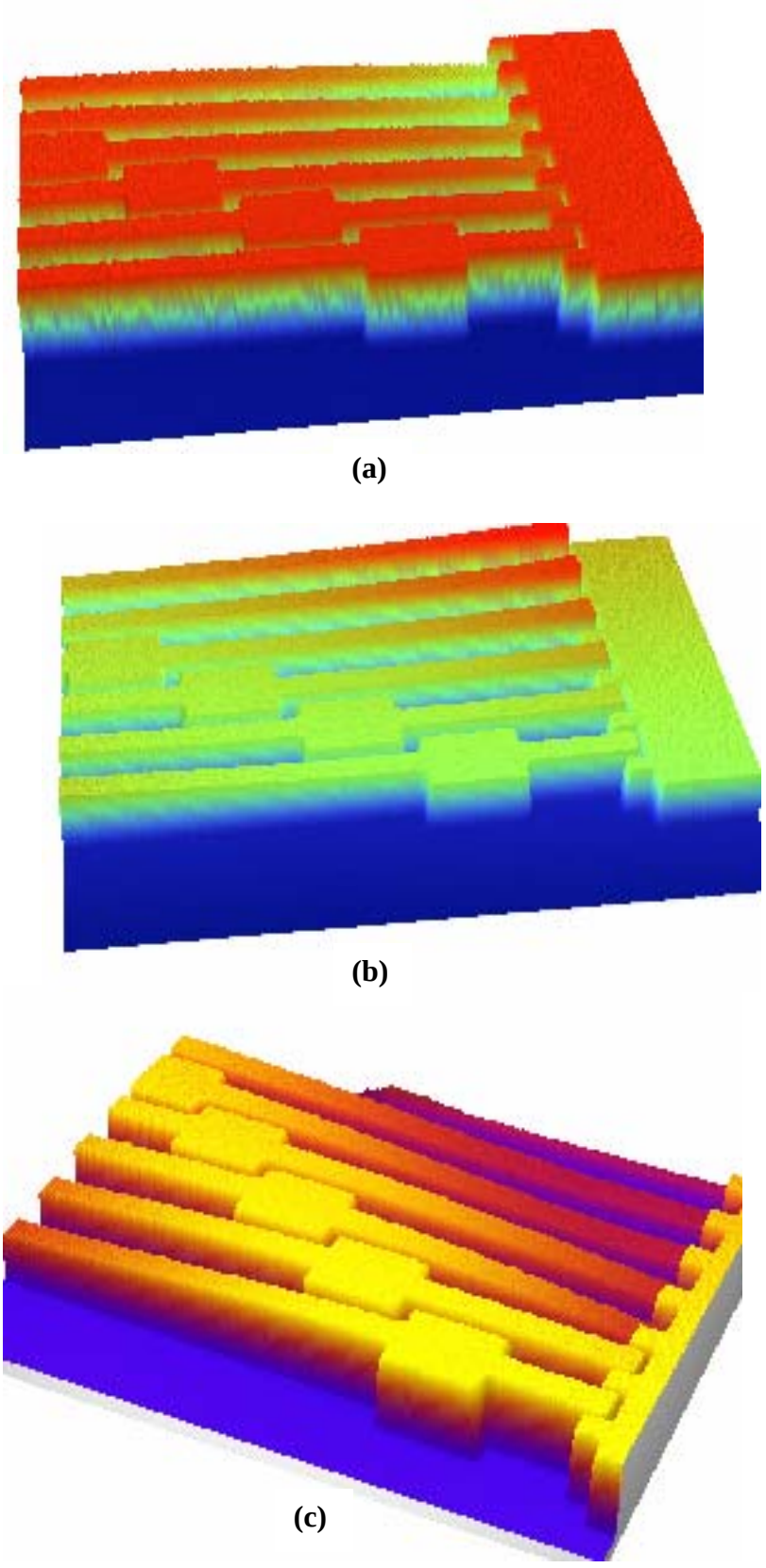


Figure 4.11: Interferometry images of p+ $Si_{1-x}Ge_x$ 100µm-long cantilever beams
(a) flat films corresponding to a deflection of 0.1µm
(b) slightly positive strain gradient corresponding to a deflection of 0.2µm
(c) slightly negative strain gradient corresponding to a deflection of -0.3µm.

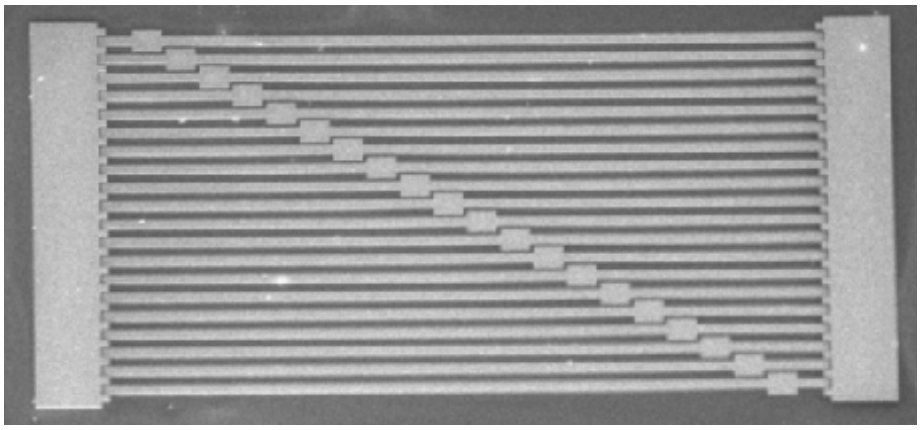


Figure 4.12: Images of released p+ poly-$Si_{1-x}Ge_x$ cantilever beams.
(a) using a Veeco Instrument WYKO interferometer **(b)** plan-view scanning electron micrograph. The beams are comprised of bilayer $Si_{1-x}Ge_x$ films:

- The bottom $Si_{1-x}Ge_x$ layer was deposited at 425°C and 600 mTorr, with GeH_4 flow rate = 70 sccm, SiH_4 flow rate = 105 sccm and BCL_3 flow rate = 12 sccm, σ=-51MPa
- The top $Si_{1-x}Ge_x$ layer was deposited at 410°C and 600 mTorr, with GeH_4 flow rate = 45 sccm, SiH_4 flow rate = 130 sccm and BCL_3 flow rate = 12 sccm, σ=-295MPa

Out-of-plane tip deflection is 0.1μm for a 100μm-long beam.

4.2.3.6. Definition of disk layer using bi-layer p+$Si_{1-x}Ge_x$ film

After the deposition of the 4μm-thick p+$Si_{1-x}Ge_x$ structural layer, the underlying patterns were no longer visible due to the thick and rough structural $Si_{1-x}Ge_x$ film. Therefore, a blanket lithography step was used to remove the structural layer from an entire column of dies to reveal the underlying alignment marks. **Figure 4.13a** shows a SEM top view of the fabricated proof mass disk with the side electrodes. And **Figure 4.13b** shows a SEM top view of the fabricated bottom electrodes, proof mass and side electrodes.

Initially chlorine and bromine chemistries were used to etch the structural layer. The roughness of the 4μm $Si_{1-x}Ge_x$ films was so high (> 400 Angstroms) and results into a

sloped resist, which caused the RIE procedure to yield an undesirable angled lateral gap (**Figure 4.14).** Using the Bosch RIE process, a straighter lateral gap was achieved. **Figure 4.15** shows a cross section of the fabricated proof-mass with the side electrodes (**Figure 4.15a**), a zoom-in interferometry image of the 0.6µm lateral gap (**Figure 4.15b**) and a SEM top view of a 0.8µm lateral gap (**Figure 4.15c**).

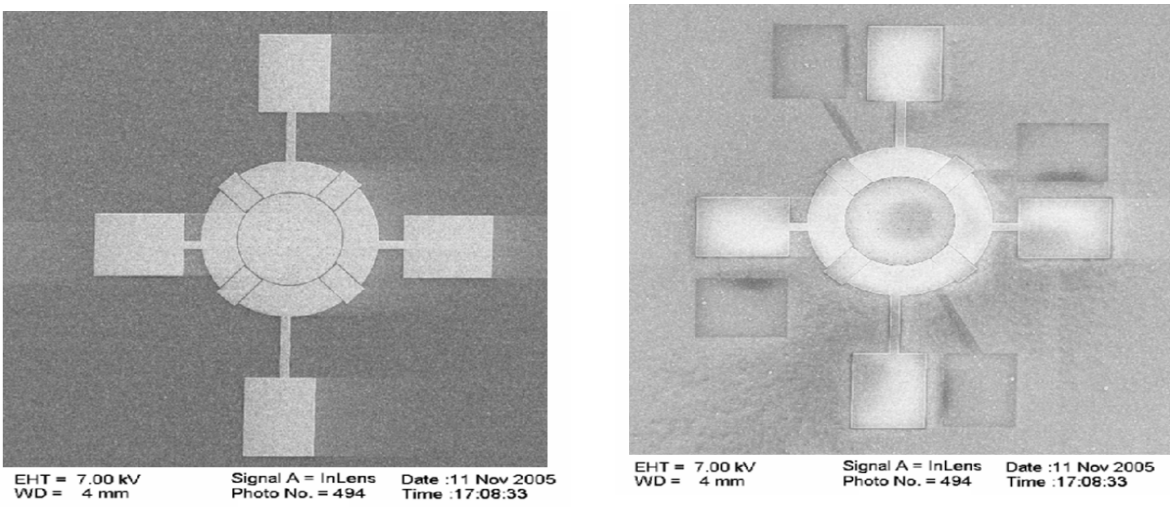


Figure 4.13: (a) plan-view SEM image of patterned p+ $Si_{1-x}Ge_x$ proof-mass disk and side electrodes **(b)** image showing proof-mass disk layer as well as the lower electrodes.

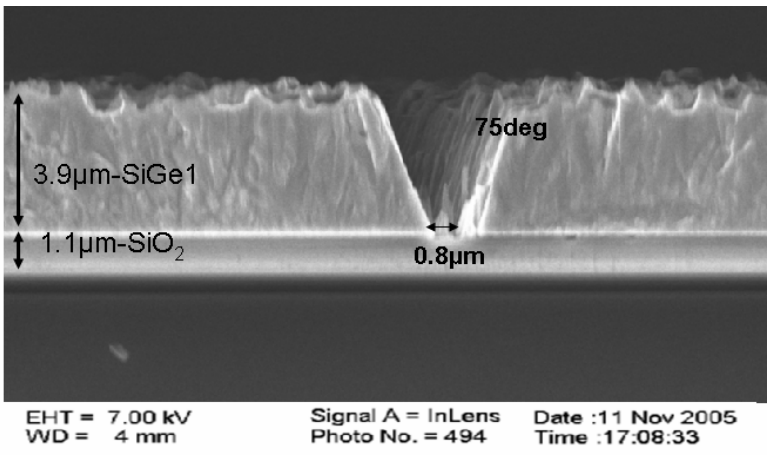
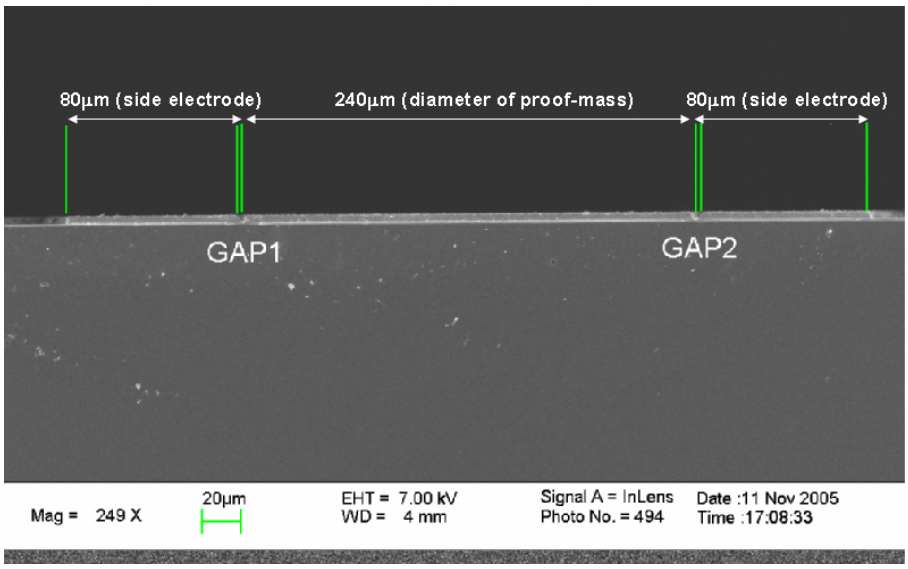
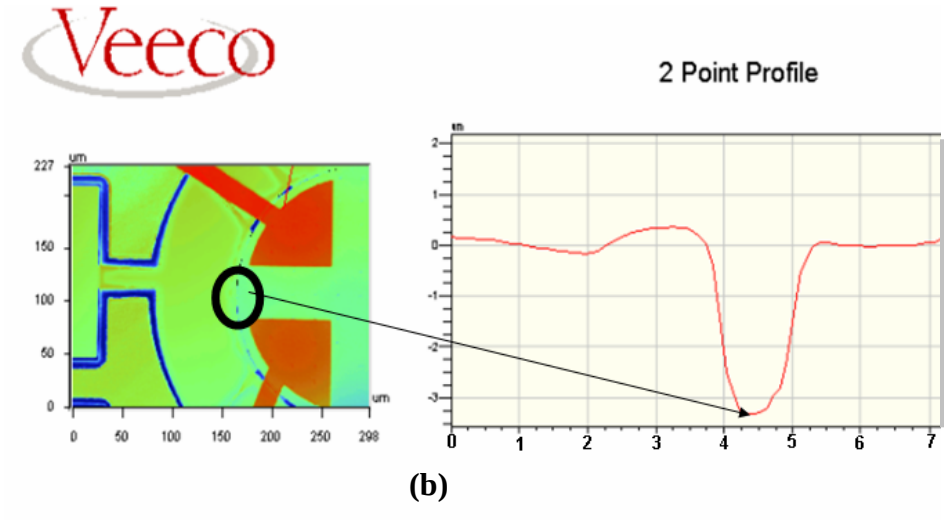


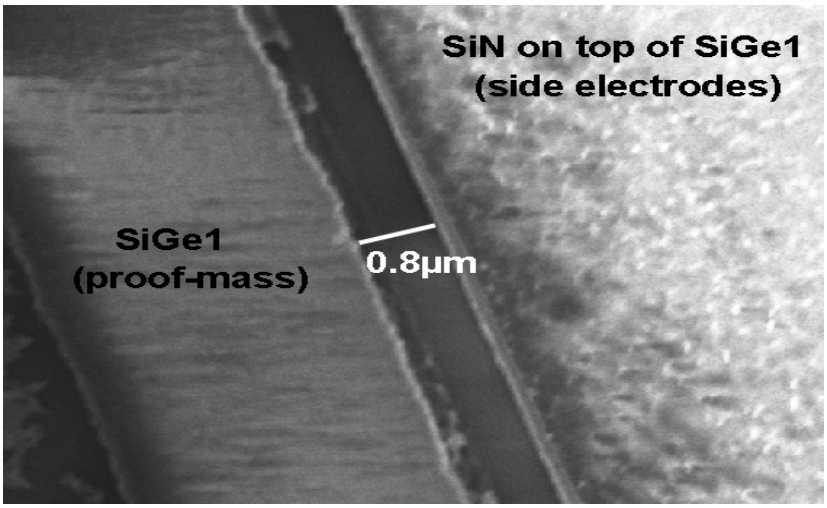
Figure 4.14: 75ºC angled lateral gap achieved when using chlorine based chemistry to etch 4µm bi-layer p+ $Si_{1-x}Ge_x$ used for the definition of the proof-mass disk layer**.**



(a)



(b)



(c)

Figure 4.15: **(a)** SEM cross section of the proof-mass and side electrodes, **(b)** zoomed-in interferometry image of a 0.6µm lateral gap and **(c)** SEM plan view image of a 0.8µm lateral gap.

Next, 2µm of LTO is deposited as a sacrificial layer to define the second vertical gap, then chemical mechanical polishing (CMP) was used to planarize the sacrificial layer, thus reducing the topography of the surface so that the two last subsequent lithography steps are easy to process. A low strain gradient bi-layer of p+ $Si_{1-x}Ge_x$ film was deposited and patterned for the definition of the top electrodes after the definition of the SiN anchoring regions (**Figure 4.16**). Images of the FLEMS devices were taken using both SEM and a high-magnification optical microscope after the complete fabrication process flow (**Figure 4.17**).

A cross-sectional SEM image of a non-released FLEMS device that shows the thicknesses of the various layers is presented in **Figure 4.18**. The uppermost LTO layer (for the definition of the second vertical gap) turned out to thinner than expected (~200nm). This unexpectedly thin LTO film is most likely due to the CMP process which was found to be non-uniform across a wafer.

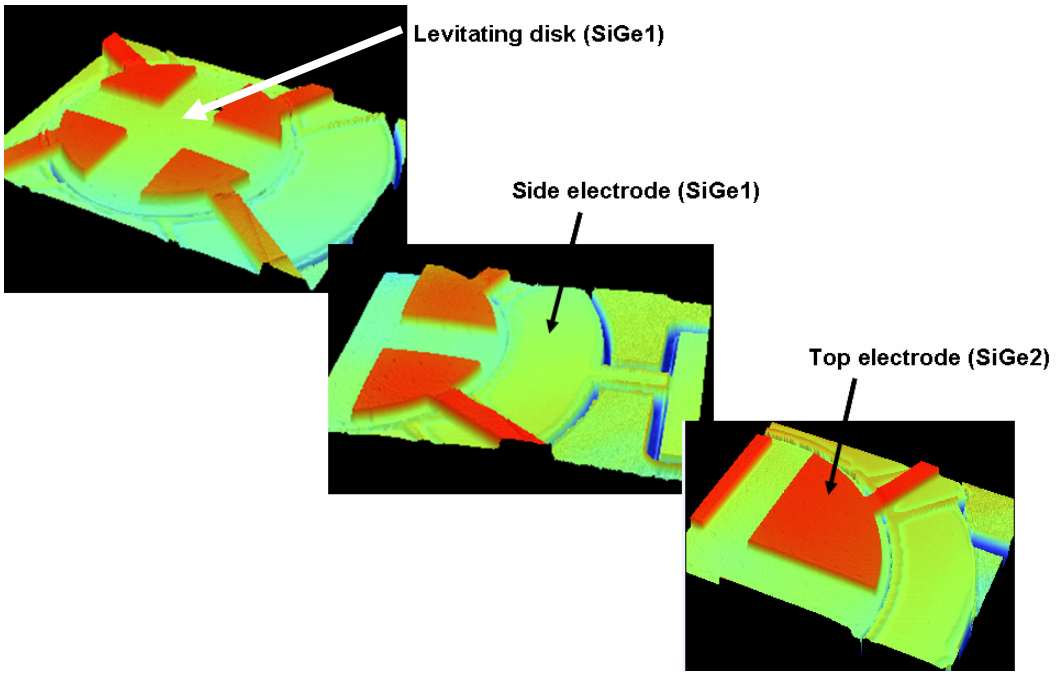


Figure 4.16: Interferometry images of p+ $Si_{1-x}Ge_x$ top electrodes taken using a Veeco WYKO interferometer showing flat p+ $Si_{1-x}Ge_x$ films. Stress cancellation methodology that uses a bilayer deposition procedure was performed for the definition of the top electrodes.

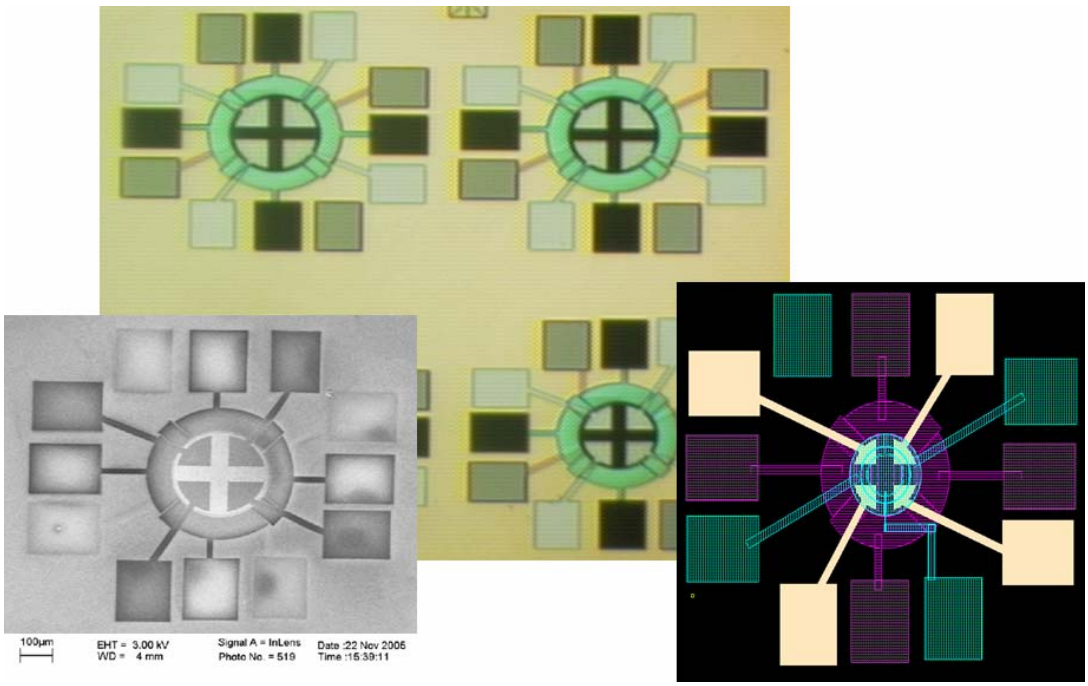


Figure 4.17: FLEMS devices after complete fabrication process flow (microscopy, SEM and layout insert images are shown).

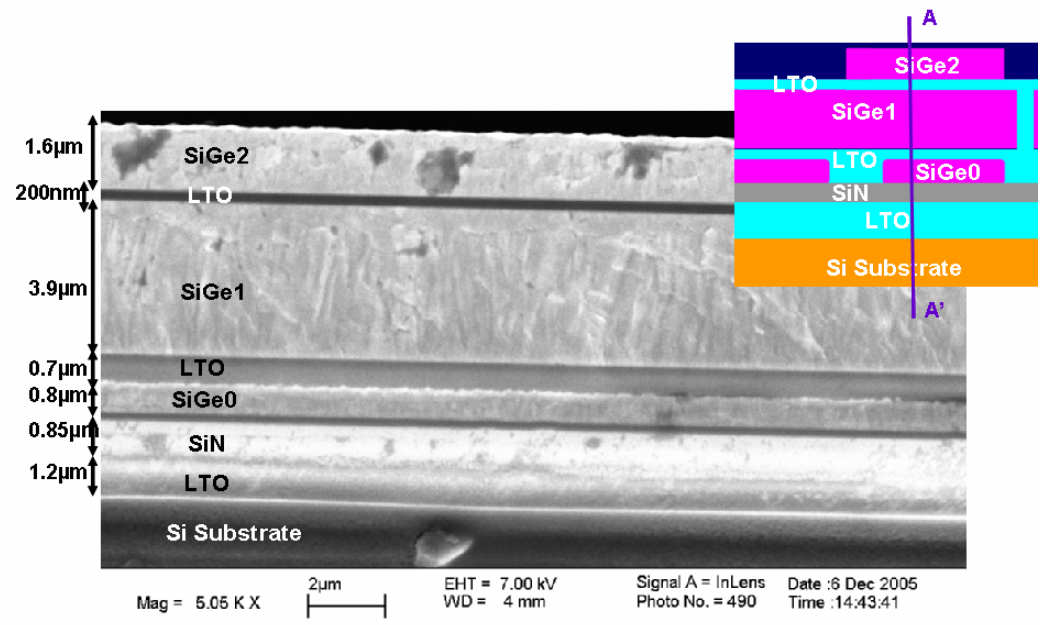


Figure 4.18: SEM cross section of the FLEMS device after complete fabrication process flow (A-A' view). Final cross section closely agrees well with the expected cross section inserted.

4.2.3.7. Release process module development

Release of the devices was performed using HF vapor. Since the HF vapor tool was new in the UC Berkeley Microfabrication Laboratory, the HF vapor release process module was characterized through a short loop experiment study. It was found that at 40^{o}C, HF vapor etches 15μm of LTO in 30 minutes while it etches 20μm of thermal oxide in 55 minutes. A microscope image of a FLEMS release device showing the HF etching edge contour after complete release of devices is shown in **Figure 4.19.** Several destructive tests were performed in order to investigate complete release of the disk and to see whether stiction after release was an issue:

- **Figure 4.20a** shows an example of an optimally released device that did not suffer any stiction problem. After the top electrodes were broken off using a microprobe tip, the disk was pushed off its rest location and no sacrificial LTO remained underneath the disk.
- **Figure 4.20b** shows a die where the disk was stuck to the top electrodes, after pushing off the top electrodes; this indicates a stiction issue. 50% of the devices released in this study turned out to have a stiction problem between the top electrodes and the free disk. Perfluorodecyltrichlorosilane (FDTS) and octadecyltrichlorosilane (OTS) based self-assembled monolayers (SAMs) anti-stiction coatings tried on some dies to correct this stiction issue, but with no apparent success.

Electrical measurements for short and open circuit were performed on wafers that did not show this stiction issue, followed by electrostatic sensing and control of the FLEMS sensor device.

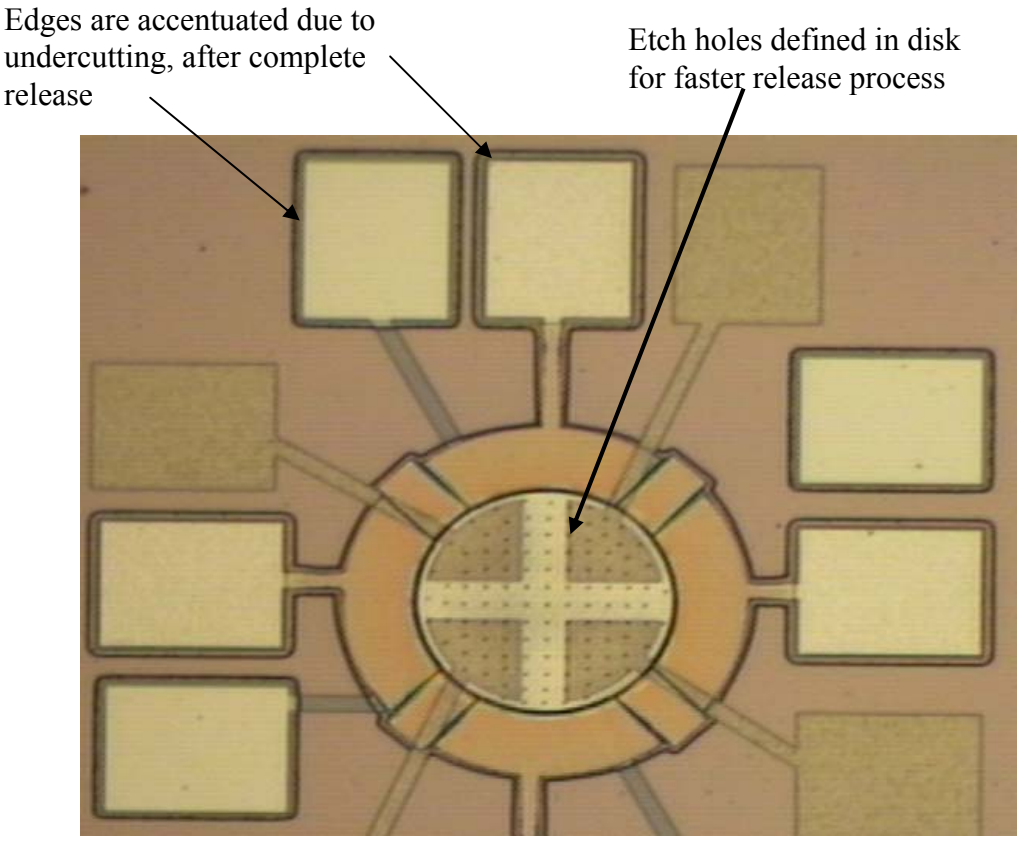
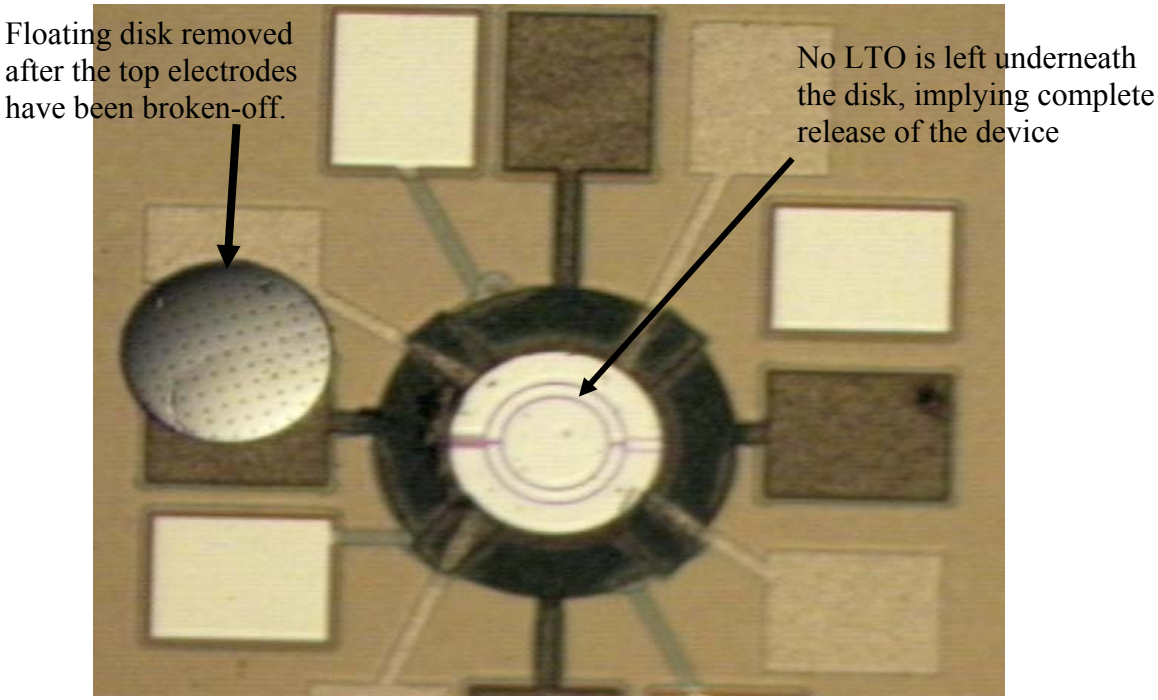
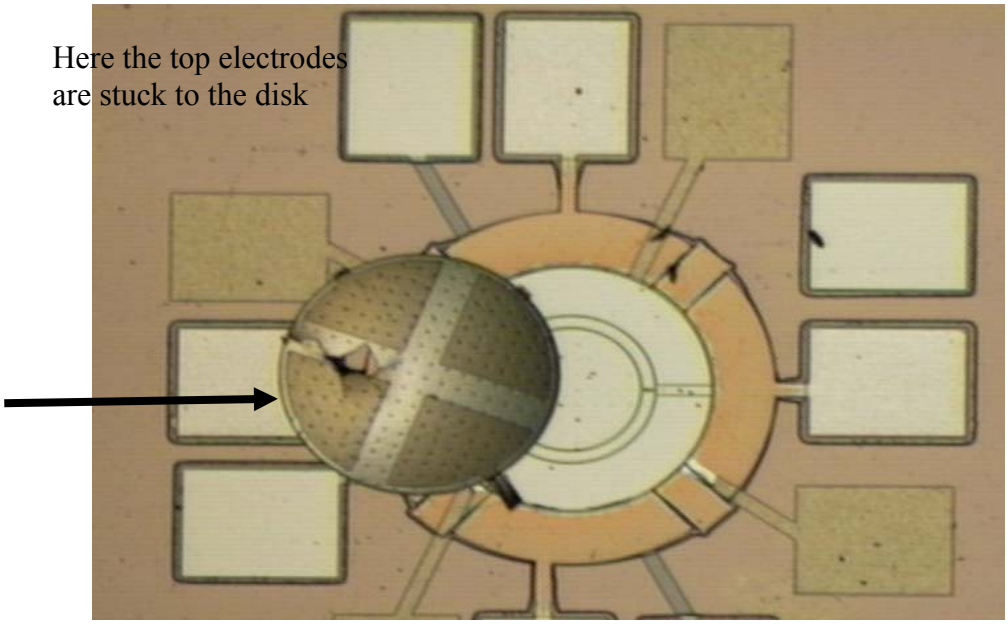


Figure 4.19: FLEMS device revealing HF etching contour after complete release in 40^{o}C HF vapor.



(a)



(b)

Figure 4.20: (a) Example of an optimal released device that does not have stiction issue **(b)** Example of released device with potential stiction issue between the top electrodes and the proof-mass disk.

4.2.4. Electrical Measurement

4.2.4.1. Theory of electrostatic lift-off

Simulations of an electrostically levitated disk along with the tuning of a controller have been previously developed by *A. Kominek* and *D. Garmire* (work not published). The results of these simulations reveal that it is possible to control the position of the disk by controlling the applied voltages on the different electrodes.

Electrostatic forces are used for the sensing and the actuation of the FLEMS sensor devices. Initially, the disk is assumed to be at rest on the bottom electrodes. Stiction and gravitational forces keep it there. In order to lift up the disk, an electrostatic voltage is to be applied on the top electrodes. This voltage induces a charge on the disk, which will be injected through the grounded bottom electrodes as long as there is a contact. Due to the potential difference between the top electrodes and the disk, the electrostatic force pulls the disk up. When the gravitational force and the stiction force are overcome by the electrostatic force, the disk lifts up. Before lift-off, the induction from the top electrodes forces the charges to be transferred to the bottom electrodes. After lift-off, there is a net charge on the disk. This net charge was computed using Finite Element Modeling (FEM) to be ~ 8.3×10^{-14} Coulombs [4.34].

It is important to note that a reduced damping was assumed in the simulation work. This condition occurs when the device is in vacuum. Simulations with higher damping and longer sampling times were not successful. Therefore ultimately, vacuum encapsulation will be needed to reduce the air damping effects on the system, thus achieving an optimal electrostatic levitation mechanism.

4.2.4.2. Sensing of the disk

As a demonstration of the sensing mechanism of the disk, a relatively high AC frequency (f~500 kHz) voltage signal is sent through the bottom (lower) electrodes. Due to this voltage, currents are induced to the side and upper electrodes of the FLEMS sensor. These currents are sent through an integrator Op-Amp (Operational Amplifier), then amplified through a voltage Op-Amp. A RMS-DC converter that incorporates a low-noise phase lock loop converts the sinusoidal signal into a linear output. The linear signal is fed through a MATLAB Simulink code that calculates the differential capacitance, which is a function of the position and rotation of the disk. The same Simulink program provides a control loop code for the electrostatic control of the system after levitation.

A schematic of the electronics circuitry used for the sensing and control of the FLEMS sensor is shown in **Figure 4.21**. Differential voltages ranging from 0 to 40Volts were swept between the upper and lower electrodes during five different runs. **Figure 4.22** presents the electrical signals that have been generated during the sensing testing with no feedback control included. The results show that during the first run, the disk initially lifts-off at a bias ~ 25.65V, and then becomes unstable until the differential voltage is removed. This instability is due to the fact that when the disk is lifted-off, it remains at the center position as long as the net charge on the system is zero. If the applied voltage keeps on increasing, the disk would eventually touch the upper electrodes. And as a result, it will get discharged so that it will fall back on the lower electrodes to get charged-up again. This trend will continue till the voltage is turned off. However during subsequent runs, the differential capacitance is observed to be almost constant, translating into a null displacement of the disk. This could be attributed to the

stiction phenomenon that would occur after the disk returns to its resting state on the lower electrodes (once the applied voltage is removed). It is important to note that the slight change in capacitance observed before complete lift-off as well as for subsequent runs would indicate a minor deformation of the disk as the applied bias increases.

Given the dimensions of the FLEMS sensor device, theoretical computations show that the voltage required for lift-off would provide a charge enough to supply 8000*g* acceleration at 10V. Also assuming a standard differential circuit sensitivity of 1aF $/\sqrt{Hz}$, the position of the disk can be sensed with a resolution of about 0.01Å $/\sqrt{Hz}$, what is comparable (and even better) to what is achieved with most common manufactured accelerometers sensors.

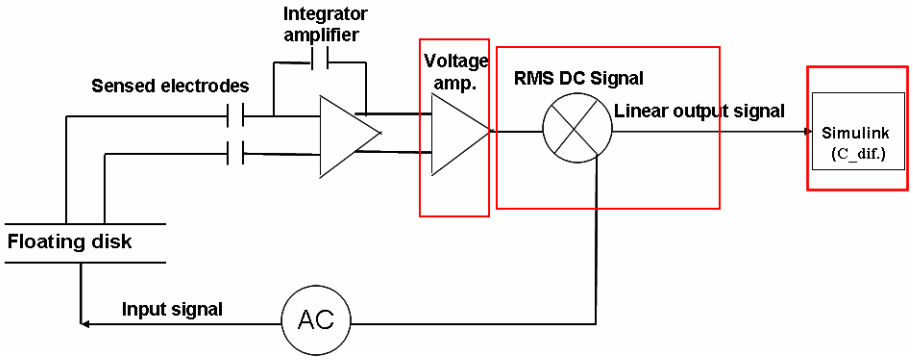


Figure 4.21: Schematic of the electronics apparatus used for the sensing and electrostatic control of the FLEMS disk.

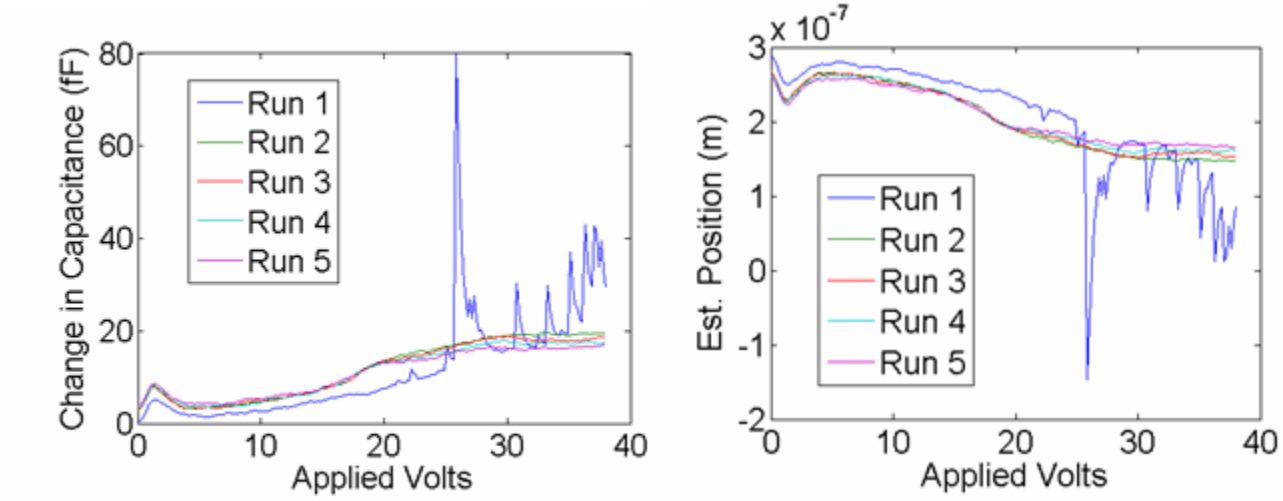


Figure 4.22: **(a)** Change in Capacitance vs Voltage **(b)** Estimated lift position vs Voltage (Courtesy of *D. Garmire*).

4.3. Summary

The first part of this chapter presents a novel fabrication technique using Ge blades to define nanometer lateral gaps in the processing of SiGe electrostatic RF MEMS filter devices. Photoresist ashing was demonstrated to be a suitable, reliable and simple procedure for the formation of lateral nanometer gaps. SiGe resonators structures were successfully fabricated with gap dimensions ranging from 50nm to 150nm.

The second part of this chapter suggests a novel device design and fabrication procedure of CMOS compatible FLEMS (Floating ElectroMechanical System) sensor devices using poly-$Si_{1-x}Ge_x$ surface micromachining technology. For this purpose, a design of experiment was performed using $Si_{1-x}Ge_x$ bilayer stress cancellation methodology for the reduction of the strain gradient on the free proof-mass disk. Strain gradient ~$2x10^{-5}$μm corresponding to a tip deflection of 0.1μm for a 100μm-long cantilever beam was attained. Lateral gap ~ 0.6 μm in a 4μm-thick $Si_{1-x}Ge_x$ layer was defined to allow easy sensing of the capacitively induced current. The fabrication process of the FLEMS devices was successfully completed after the definition of low strain gradient p+ $Si_{1-x}Ge_x$ disk and upper electrodes. The release module in HF vapor was characterized and optimized, and it was found that 15μm of LTO etched in 30 minutes in HF vapor at a temperature of 40ºC.

As a demonstration of the sensing aspect of the system, a feedback control loop that inputs a sinusoidal wave function, and outputs a linear function through a RMS DC Signal converter was designed. Electrical responses showed a vertical displacement motion of the disk between the lower electrodes and upper electrodes, with the disk

released at a bias ~ 25.65 Volts. This reveals that the disk is indeed free to move in place, and can be used as a MEMS acceleration sensor system with an estimated resolution sensitivity of 0.01 Å / $\sqrt{Hz}$ (assuming a standard differential circuit sensitivity ~ 1aF / $\sqrt{Hz}$). Ideally, any acceleration could be sensed with such a system given the fact that the major loss mechanisms due to anchor and suspension losses are eliminated. However in practice, the achievable acceleration would be limited by the amount of charge (thus voltage) required in order to trigger levitation, and how precise the resulting differential capacitance can be resolved. Further optimization will be necessary in order to demonstrate angular acceleration sensing mechanisms for potential gyroscope applications. Also, the real-time control feedback of the system after lift-off is yet to be demonstrated in order to prove optimal electrostatic levitation.

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Chapter 5

RF MEMS Switches using Standard "Back-End-Of-Line" Materials

5.1. Background

5.1.1. MEMS technology using standard "back-end-of-line" materials

A second approach for post-CMOS integration of MEMS with ICs is to use back-end-of-line (BEOL) materials such as aluminum [5.1]-[5.4] or copper [5.5] that are already available in the integrated circuitry to fabricate the MEMS devices.

Using the aluminum interconnects present in most standard CMOS processes as moving layers, *Fedder et al.* succesfully fabricated MEMS accelerometers by surface micromachining technology and deep reactive ion etching (**Figure 5.1**) [5.1]. In their work, the multilayered composite structural layer was made of polycrystalline silicon and aluminum metal lines. To define the MEMS structures, they used three RIE etch processes which include: backside etch of structural silicon film, front side etch of dielectric materials and front side release-etch of silicon. The main benefit of this

technology is that "Post-CMOS" integration of MEMS on ASICs is made possible without any additional materials.

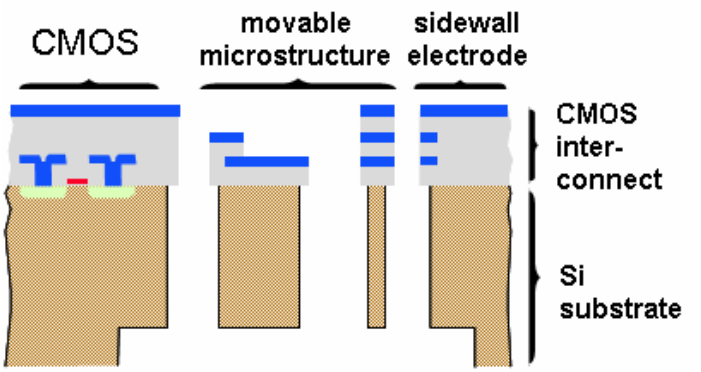


Figure 5.1: A post-CMOS micromachined lateral accelerometer fabricated using aluminum based interconnects [5.1].

During recent years, copper has been intensively researched within the IC industry as a good candidate material for the replacement of aluminum in back-end technology for the 25nm (and below) technology node. This is mainly due to its low resistivity (1.2μΩ-cm) as well as its lower vulnerability to electromigration (the movement of individual atoms through a wire), caused by high electric currents, which creates voids and ultimately breaks wires [5.6]-[5.8].

Similar to SiGe MEMS technology, using copper-based MEMS technology to create free standing micromachined devices presents several challenges, mainly due to the severe strain gradient inherent in the multilayered copper structures. This is caused by the fact that the transition from aluminum to copper for integrated circuit interconnections, rather than being a simple replacement of one metal with another, requires migration from blanket metal deposition to a dual damascene process with several barrier layers. The two types of barrier films most widely used in copper

interconnects are: a liner on the side and bottom of the damascene features and a cap on top of the damascene features. The reason for these barrier layers are to prevent copper and oxygen diffusion as well as to promote a good adhesion between copper and the interlayer dielectric (ILD) [5.9]. Also, copper, unlike aluminum, easily oxidizes and must be encapsulated to prevent corrosion during subsequent process steps [5.10]-[5.12]. Thus, the resulting micromachined structures often have a complicated multilayer cross-section and film stresses must be considered during fabrication in order to avoid large strain gradients that will result in severe deformation of the beams, which compromises the reliability of the RF MEMS structures [5.13]-[5.14].

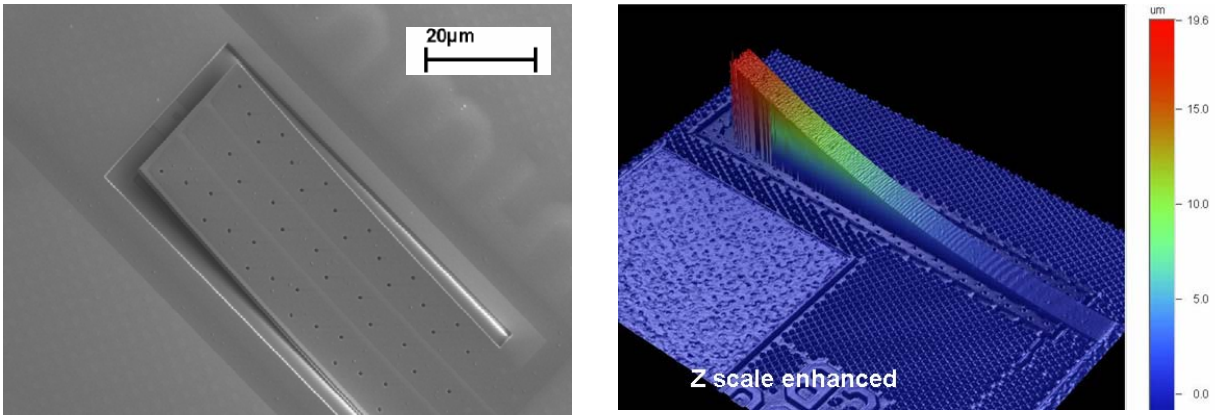
5.1.2. Overview

An analytical model to predict the curvature of a five layers released MEMS cantilever beam structure made of standard back-end-of-line (BEOL) materials (SiN/Cu/TaN-Ta/SiN) was developed [5.13]. The MEMS cantilever beams were fabricated along with RF MEMS switches using a low temperature ($T<400^{o}C$) copper-based CMOS interconnect manufacturing technology [5.14]. For all copper-based MEMS devices reported, a highly compressive TaN/Ta adhesion layer/barrier was used in conjunction with the copper layer. These films cause severe deformation in released MEMS cantilever beams as illustrated in **Figure 5.2**. Both Physical Vapor Deposition (PVD) and Atomic Layer Deposition (ALD) were used to deposit the TaN layer in the BEOL film stack. Elemental analysis was performed in order to characterize the residual stress of individual film used in the analytical model. Interferometry measurements show deformations that agree within 20% of the predictions of the theoretical model developed.

The model can be used to characterize the curvature of multilayer cantilever beams fabricated with low stress liner, as well as for device engineering design and process optimization.

In addition, the effects of annealing on devices to 400^{o}C was investigated and compared to measured beam deflection. Reducing the adverse effects of deflection of multilayered MEMS cantilever switches would imply meeting design goals for a lower actuation voltage, improved switch performance and manufacturing yield following subsequent packaging [5.15].

The ultimate goal of this study was to develop a better understanding of strain gradient effects present in multilayered copper-based back-end MEMS process for the reduction of the severe deflection in copper-based composite MEMS cantilever switches.



(a) **(b)**

Figure 5.2: **(a)** SEM of released copper-based cantilever beam showing significant deformation due to an overall compressive stress. **(b)** Interferometry image of same device with enhanced Z-scale.

5.2. Previous studies on multilayer modeling

Composite beam structures have been widely used in microelectronics, optics, several RF/inertial MEMS applications and numerous other engineering fields. Therefore, it is very crucial to accurately characterize as well as predict their elastic deformation for the design of high performance devices. Calculations of stress and/or curvature in multilayer structures have been published by several authors, yet the results are usually complex and are based on particular boundaries conditions specific to their targeted application [5.16]-[5.26].

Stoney was the first to develop an expression of the residual stress for a single thin film grown or deposited on a thick substrate (see ***Equation 5.1***) [5.26]:

$$\sigma_f = \frac{1}{6}\frac{E_s}{(1-\nu_s)}\frac{t_s^{\,2}}{t_f}\frac{1}{\rho} \qquad (\textbf{\textit{Equation 5.1}})$$

where σ_f is the film stress, E_s and ν_s are respectively the Young's modulus and the Poisson's ratio of the substrate (note that $E_s/(1-\nu_s)$ represents the bi-axial Young's modulus), t_s and t_f are the thickness of the substrate and the film respectively, and ρ is the radius of curvature of the wafer. Several theoretical models of thin films mechanical' stress were constructed later on as they applied to more than one film [5.27]-[5.32].

5.3. Development of theoretical model

5.3.1. Overview

The multilayer beam model used in this work consists of five layers *i*, where the subscript *i* refers to the layer number and is ranged from 1 to 5 (with 1 representing the layer immediately adjacent to the substrate). Each layer is characterized by its thckness t_i, Young's modulus E_i, Poisson ratio ν_i and residual stress σ_i. The residual stress is a product of both film processing deposition methodology and material properties. Therefore each film's respective stress value was evaluated based on the extended Stoney's equation, from wafer curvature measurements performed using a Tencor FLX-2320 instrument. **Figure 5.3** presents the approach used in this work for modeling the copper-based multilayered cantilever beams followed by a cross-section of the composite beam modeled.

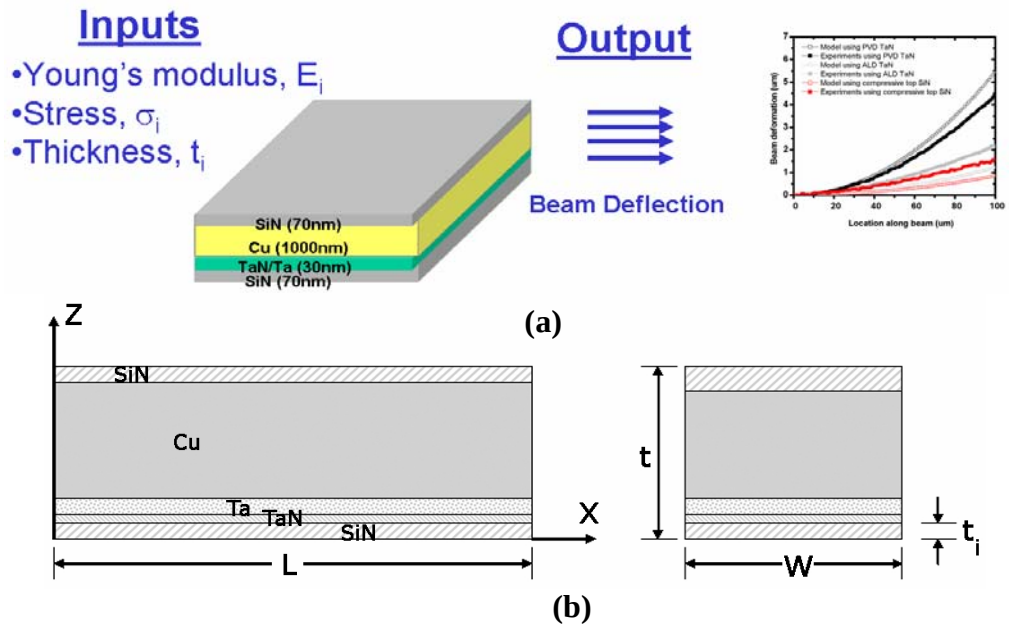


Figure 5.3: **(a)** Schematic description of the analytical approach used to derive the copper-based multilayered model. **(b)** Cross section of multilayer copper-based MEMS cantilever beam (not drawn to scale).

5.3.2. Modeling

Given the fact that the multilayer beam is anchored at one end of the substrate and free at the other end, beam theory for elastic deformation was applied. Some assumptions were necessary for the development of the model:

- Small deformation was assumed to be true
- The interface between the layers are continuous and do not slip with respect to one another
- The shear stresses in the layers are assumed to be negligible (this assumption justified since $t << L$)
- Every layer is defined as a rectangular solid with uniform length (L) and width (W), but with various films thicknesses (t_i)

The longitudinal strains of composite beams can be determined from the same basic axioms used for finding the strains in uniform beams fabricated with a single material [5.16]-[5.17]. The strain distribution can be decomposed into a uniform component (ε_o) and a bending component ($\kappa.t$) [5.2]-[5.6], and varies linearly along the surface of the beam according to ***Equation 5.2***:

$$\varepsilon_i = -\kappa z + \varepsilon_o \qquad (\textbf{\textit{Equation 5.2}})$$

In this equation, κ is the curvature and z the distance from the neutral axis. From Hooke's law, the thermal strains of each film can be related to the normal stress by ***Equation 5.3***:

$$\sigma_i = E_i\left[\varepsilon_i - \alpha_i \Delta T\right]$$

$$\sigma_i = E_i\left[(-\kappa z + \varepsilon_o) - \alpha_i \Delta T\right] \qquad (\textbf{\textit{Equation 5.3}})$$

It is important to note that $\alpha_i \Delta T$ is the strain due to different coefficient of thermal

expansion. Also for a plate-like-beam structure, the biaxial modulus $\left[E_i \middle/ (1-\nu_i) \right]$ is used instead of the normal modulus, E_i.

Due to different materials thermal mismatch, the composite beam will deform even without any external loading. There are no external forces applied to the system, therefore the only forces considered are internal due to bending strains and stress. When the thickness of the films is much less than the thickness of the substrate, the solution for elastic beam deformation can be simplified. To meet static equilibrium after released of the multilayer beam, both the bending forces and moment with respect to a bending axis need to be zero:

$$\sum F_i = 0 \Rightarrow \int_0^{t_i} E_i \left[(-\kappa z + \varepsilon_o) - \sigma \Delta T \right] dz = 0$$

$$\sum M_i = 0 \Rightarrow \int_0^{t_i} E_i \left[(-\kappa z + \varepsilon_o) - \sigma \Delta T \right] z dz = 0 \qquad (\textbf{\textit{Equation 5.4}})$$

The unknown parameters ε_o and κ are found solving the following linear equations:

$$\frac{-\kappa}{2} \sum_{i=1}^{N} E_i \left[t_i^{\,2} - t_{i-1}^{\,2} \right] + \varepsilon_o \sum_{i=1}^{N} E_i \left[t_i - t_{i-1} \right] - \sum_{i=1}^{N} E_i \alpha \Delta T \left[t_i - t_{i-1} \right] = 0 \qquad (\textbf{\textit{Equation 5.5}})$$

$$\frac{-\kappa}{3} \sum_{i=1}^{N} E_i \left[t_i^{\,3} - t_{i-1}^{\,3} \right] + \frac{\varepsilon_o}{2} \sum_{i=1}^{N} E_i \left[t_i^{\,2} - t_{i-1}^{\,2} \right] - \frac{1}{2} \sum_{i=1}^{N} E_i \alpha \Delta T \left[t_i^{\,2} - t_{i-1}^{\,2} \right] = 0 \qquad (\textbf{\textit{Equation 5.6}})$$

Equations 5.5 and **5.6** provide two equations with two unknowns, κ and ε_o, allowing an easy solution for the curvature κ using a numerical methodology. A MATLAB script was used for the computation of *D*, the multiplayer beam deflection: $D = \frac{\kappa}{2} L^2$ (***equation 5.7***)

where κ is the curvature of bending, *L* the distance to the fixed end of the beam.

5.4. Experimental details

5.4.1. Fabrication of test structures

Along with RF MEMS switches, multilayer cantilever beams test structures of thin films that are commonly found in the interconnect levels of CMOS and BICMOS IC's have been fabricated by researchers at IBM Watson Research center (**Figure 5.4)**. The fabrication process of these MEMS devices was previously reported in [5.5] and [5.14] followed by a more detailed analysis of RF MEMS switches [5.33]. All of the dielectric films have been produced using PECVD with a maximum temperature of 400^{o}C, and all the metals are deposited using sputter deposition or a combination of sputter and an electroplating. Metallization of copper interconnect involves the deposition of a copper barrier layer (commonly referred as the liner) and a seed layer followed by electroplating of copper. Currently, physical vapor deposition (PVD) techniques are most widely used to deposit both the barrier and the seed layers. In this study, the barrier layer (liner) was constituted of a bilayer film made of Tantalum Nitride (TaN) and Tantalum (Ta). ALD films are inherently conformal and uniform, allowing ultrathin films to be deposited with a low tensile stress. Initial stress measurements show that TaN deposited by PVD has a high compressive stress close to -3GPa, which led to a significant curl-up of the multilayer beam after release (**Figure 5.3**). Some of the wafers had ALD TaN replacing PVD TaN on the multilayer film stack, to remedy the overall compressive stress of the beams. A Veeco instrument WYKO interferometer was used to measure the tip deflection of 250μm long and 20μm wide cantilever beams, thus determining their radius of curvature.

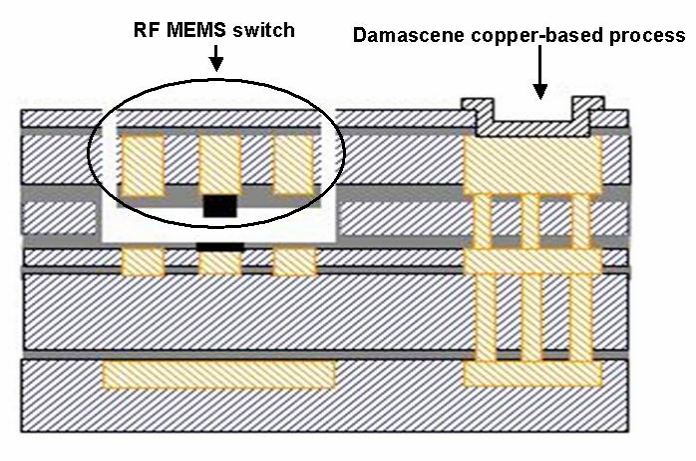


Figure 5.4: Schematic of copper interconnect structures used to fabricate RF MEMS devices (switches and resonators) using conventional back-end-of-line (BEOL) materials.

5.4.2. Residual stress characterization

Residual stresses occurred due to non-uniform processing conditions and material properties such as temperature, coefficient of thermal expansion, chemical/nucleation shrinkage/growth that remain in the structure after processing [5.34]. The residual stresses are composed of intrinsic stresses and extrinsic stresses. The different causes of intrinsic stress are: grain growth process, microstructure, grain size, orientation, misfits/substitutional or intersticial impurities and phase transformation. Common sources for extrinsic stresses are differential material properties such as coefficient of thermal expansion and processing conditions. All of the residual stresses besides the extrinsic stresses formed during the device fabrication processes are categorized as intrinsic stresses [5.34]. Stress measurements performed exactly at the deposition temperature would enable the determination of pure intrinsic stress components separately. However, *in-situ* measurement of stresses for various layers of a thin film is

not an easy task. In this work, thin films of SiN, Cu, TaN and Ta were deposited on (100) Silicon wafer in order to mimic the film stack in the regular copper-based multilayer MEMS cantilever switches (**Figure 5.3**). In these wafers, the TaN film was deposited using both Physical Vapor Deposition and Atomic Layer Deposition. Wafer curvature measurements were made using a Tencor Flexus-2320 instrument that scans the wafer surface on its backside. Four measurements were taken in x and y direction, both in the front side and backside of the wafer to get better measurement accuracy. The average residual stress values are reported in **Table 5.1**. In order to extract individual stress level in the complete film stack, Stoney's equation (***equation 5.1***) was used.

Table 5.1: Material properties of thin films used in the MEMS multilayered beam. Young's modulus and Poisson ratio data were obtained from the literature. Thickness and stress values are experimental data.

	SiN	Cu	Ta	TaN
Thickness(nm)	70	1000	20	10
Young's Modulus (GPa)	184	110	186	240
Stress(MPa)	-170	70	-2200	-2200
Poisson's Ratio	0.245	0.34	0.34	0.35

5.5. Results and Discussion

5.5.1. Theory compared to experiments

Deflection profile measurements of 100μm long, 40μm wide composite MEMS beams show deformations that are within 20% of that predicted by the analytical model. For cantilever beams fabricated with PVD TaN, the average deformation found from experimental measurement was 4.7μm, while that given by the analytical model was 5.2 μm. For similar dimension cantilever beams fabricated with ALD TaN, the deformation was measured to be 2.1μm, an improvement of almost 50% over the devices fabricated with PVD TaN. Even more dramatic improvement (60% reduction in deformation) was achieved when using a slightly compressive top SiN layer (**Figure 5.5**).

The 20% divergence between the experimental and the analytical results is most likely due to non-ideal factors such as the copper relaxation phenomena (discussed in section 5.5.3) that cannot easily be incorporated into a mathematic model. Moreover, some experimental errors come from the estimation of Young's modulus (Young's modulus was taken in the literature for all simulations), and stress measurements can exacerbate the model fitting accuracy. In general, the stresses in released structures are generated by the radius of curvature of the devices due to the positive bending moment of the films, while stresses in blanket films are caused by their confinement of the substrate [5.25]. Since it was not possible to accurately extract effective residual stress of each film directly from the released cantilever beam structures, this study assumed that the effective residual stress of the BEOL films does not vary after release. A short loop experiment was performed to verify this assumption. Single layers of PECVD SiN,

PECVD TaN, ALD TaN and Cu were cycled from room temperature to 400^{o}C and there was no significant change in the residual stress of these films.

5.5.2. Thermal cycling of cantilever beams

RF MEMS switches are very sensitive to humidity and contaminants (gases or organic compounds), that could degrade of the device performance [5.35]-[5.37]. Therefore, by shielding RF MEMS devices against moisture and other contaminants, many common failure mechanisms, including an increase in insertion loss as well as contact resistance, can be eliminated. Different packaging technologies have been developed by several research groups. One of the most common packaging techniques is the usage of a capping (protective coating) layer of dielectric material for the encapsulation of MEMS devices in a hermetic environment [5.39]. The deposition of this dielectric layer needs to be conformal for a good coverage of the MEMS devices as well as the exposition of the electrical wires. In addition, this deposition needs to be CMOS compatible to avoid damaging the electronics underneath the MEMS structures.

The MEMS cantilever beams fabricated using back-end-of-line materials were cycled to 400^{o}C for 2 minutes in a N_2 environment. This was to investigate the effects of subsequent temperature cycles on released MEMS devices, such as during the deposition of the final dielectric layer for packaging purpose. After one annealing cycle, the beam deformation had increased by 40% for composite beams fabricated with PVD TaN and 37% for similar beams fabricated with ALD TaN ***(*Figure 5.6)**. Such an uncontrollable increase of the beam deformation is undesirable, since it will compromise the MEMS devices' packaging. The direct implication of this result is the fact that the increase in

beam deformation during packaging should be taken into account during the design and fabrication of the RF MEMS switches, in order to offer a reliable and robust copper-based MEMS technology.

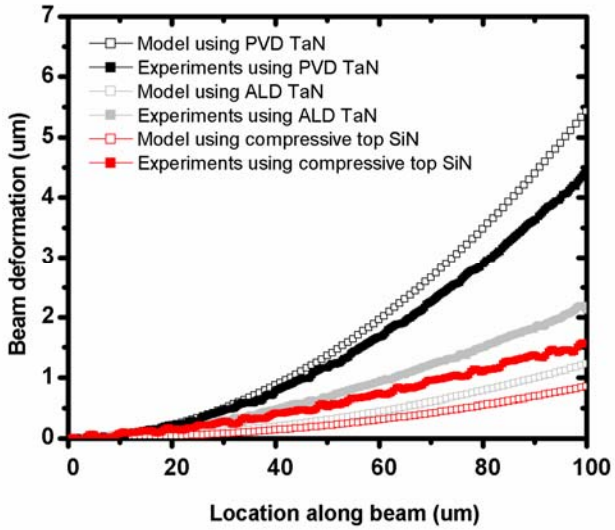


Figure 5.5: Comparison of measured and modeled deformation of composite copper-based MEMS beams fabricated using PVD or ALD TaN liner material, and PVD liner material with compressive top SiN layer. The analytical model shows a similar trend as the experimental data (reduction in beam curvature when ALD TaN is used instead of PVD TaN, as well as when compressive top SiN is used). Model accuracy is within 20%.

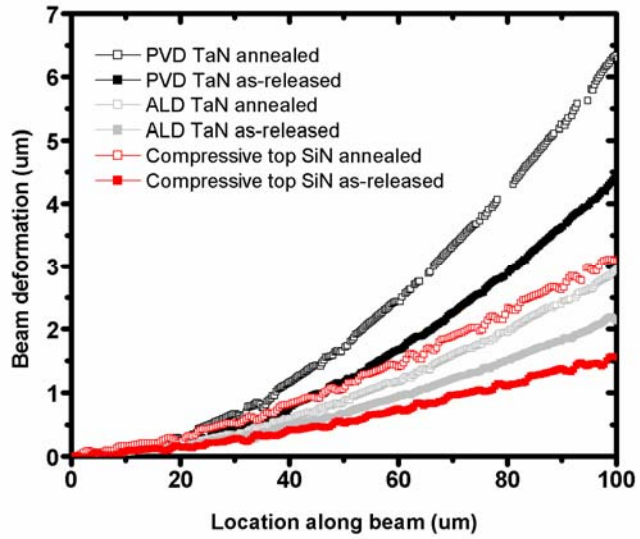


Figure 5.6: Measured increase in deformation of composite copper-based MEMS beam (reported in **Figure 5.5)** for as-released and annealed devices. Annealing was performed at 400^{o}C for 2 minutes in a N_2 ambient to mimic the deposition of a final dielectric layer used for packaging. The overall beam deformation increased by 35 – 40% following annealing.

5.5.3. Copper hysteretic behavior

5.5.3.1. Thermal cycling of the test structures

In thin film materials, the residual stress after cooling and heating generally depends on the coefficient of thermal expansion, the dimension, and the presence or absence of capping layer [5.38]-[5.39]. Copper is a very fascinating material in terms of its elastic properties. Several authors have examined the evolution and relaxation of its residual stress in an attempt to elucidate its behavior during thermal cycling [5.40]-[5.41]. In order to assert how such a complex behavior affects the multilayer beam curvature, the copper stress was plotted for different temperatures. The results are reported in **Figure 5.7** and show that during the first cycle to 400^{o}C, the stress in copper changes from a low tensile value to a compressive regime, with plastic deformation occurring around 225^{o}C, which causes a permanent increase in cantilever beam deformation. However, as the temperature returns to room temperature, the stress of copper returns to a higher tensile value than it initially was because of its high coefficient of thermal expansion. No further relaxation follows the first anneal cycle, and the stress behavior remains constant with subsequent thermal cycling. Experimental evidence from *Thouless et al.* suggests that the slope of the cooling portion of copper relation plot at low temperature indicates when dislocation-glide dominated mechanisms are important [5.41]. New results revealing that the presence of a capping layer on the surface of a film can have substantial effect on relaxing rates, possibly suppressing mechanisms associated with diffusion and dislocation climb and leaving a mechanism associated with exponential stress dependence such as dislocation glide are also presented [5.41]. Therefore, it is clear that during the deposition of the final dielectric layer, copper goes through a hysteretic behavior which includes

grain growth, film relaxation and dislocation climb. Unfortunately, this phenomenon that would greatly affect the residual stress of the copper film cannot be easily introduced into an analytical model.

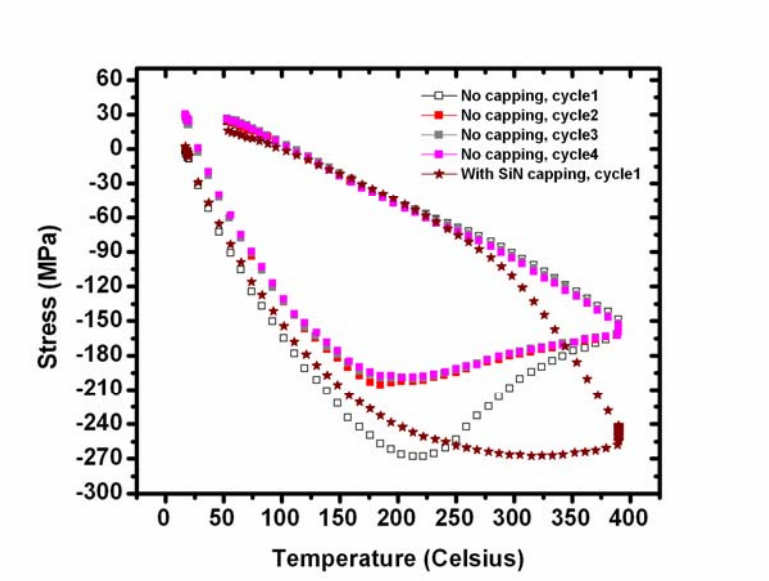


Figure 5.7: Measured hysteretic stress behavior in SiN/TaN/Ta/Cu. As the temperature is increased from room temperature to 400°C, copper relaxes and yields around 225°C. Upon cooling the copper film returns back to tensile stress.

5.5.3.2. Discussion

By changing copper stress from 0MPa to a high tensile stress (~200MPa) in the analytical model, it is possible to explain the adverse increase in beam deformation after annealing reported in section 5.5.2. Upon deposition of the final dielectric layer (SiN and SiO_2) at 400°C, it is evident that copper goes into a more compressive state (**Figure 5.7**). **Figure 5.8** was generated from the analytical model. In the model, as the copper layer becomes less tensile and more compressive, the multilayer beam has a higher deformation, which confirms what was seen experimentally in **Figure 5.6**. Also a

slightly thicker copper layer dramatically reduces the composite beam deformation since more tensile stress is being added to the beam to further compensate for the overall compressive stress of the liner.

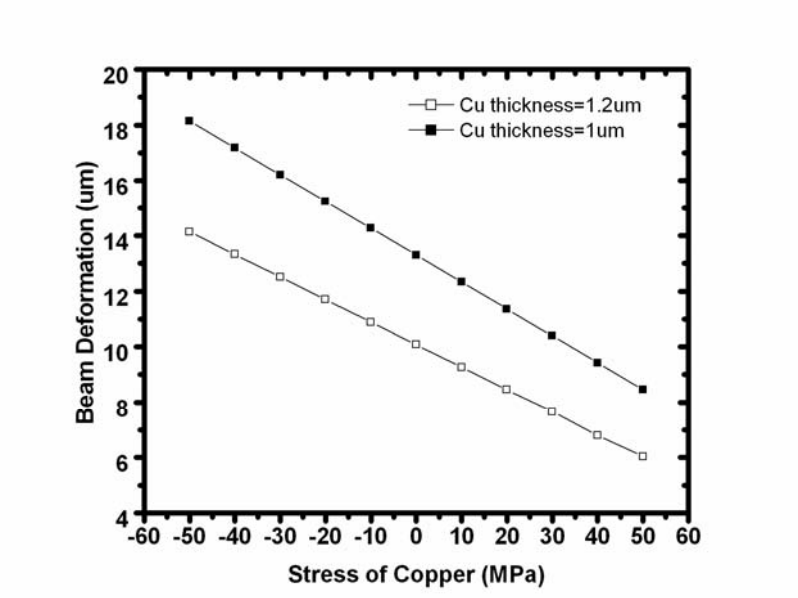


Figure 5.8: Model of composite copper-based MEMS beam deformation as a function of copper stress for copper thickness =1.0μm and 1.2μm. A slightly thicker copper film shows less deformation.

5.6. Optimization

In this section, the theoretical model developed was used for further process optimization and to evaluate design trade-offs in the fabrication of high performance copper-based composite MEMS cantilever beams switches. From the experiments, it is clear that the severe stress gradient of the beams is caused by the high compressive stress of the liner (TaN/Ta). To alleviate this, the liner thickness was reduced to half of the standard thickness used in common "back end" IC line (~50A for TaN and 100A for Ta). **Figure 5.9** shows that as the liner thickness is reduced, the multilayer beam deformation profile increases unless the copper thickness is slightly increased. This is likely due to the fact that adding a tensile layer (copper), would help to alleviate the high compression of the liner, leading to less deformation of the composite beam.

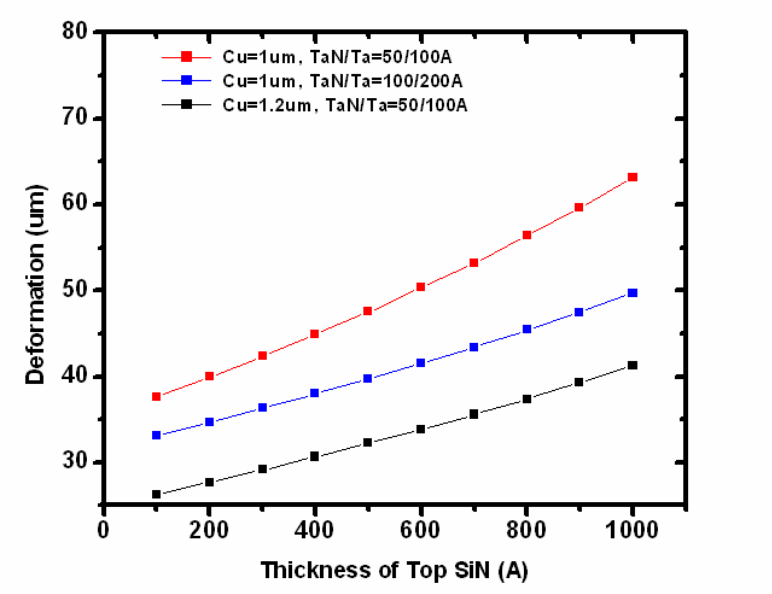


Figure 5.9: Model of composite copper-based MEMS beam deflection as a function of SiN thickness for copper thickness =1.0μm and 1.2μm, and liner thickness =100A/200A or 50A/100A.

5.7. Summary

An estimate of the deformation for multilayer beam structures made of five layers materials used in “back end of line” materials has been developed. The curvature was derived based on elastic beam theory for bending moment due to internal strains/stress only. The analytical model matched the experiments within 20% and was used to predict the deformation of copper based composite beams when several process and design parameters were modified. This study also indicates that ALD TaN films can effectively reduce the overall deformation in released copper-based IC compatible MEMS structures, and that understanding the copper stress relaxation behavior is essential to designing MEMS devices tolerant to 400ºC temperature packaging.

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Chapter 6

Conclusions

6.1. Summary of contributions

Part of this work falls into the continuation of *A. Franke's* foundational study of LPCVD p+$Si_{1-x}Ge_x$ structural layer and LPCVD p+Ge sacrificial films for integrated MEMS technology applications [6.1]. In this current contribution, several aspects of SiGe MEMS technology as well as copper-based MEMS technology have been further explored in order to attain a robust, reliable and low cost "Post-CMOS" modularly integrated MEMS technology.

6.1.1. Interconnects between p+SiGe MEMS and Al-CMOS

The non-MOS clean SiGe LPCVD furnace (Tystar 20) was installed right at the beginning of this work; this has allowed the deposition of $Si_{1-x}Ge_x$ films directly on top of metals to reduce parasitic capacitances and resistances. Without any pre-cleaning treatment, the specific contact resistivity was found to exceed $10^{-5}\Omega$-cm^2, which is too high for forming low-resistance contacts between SiGe MEMS devices and underlying

CMOS circuitry. For fixed Ge content, a higher deposition temperature (450ºC) yields lower contact resistance. A plasma pre-cleaning treatment prior to $Si_{1-x}Ge_x$ deposition substantially improves the contact resistivity, with Ar plasma being more effective than He plasma for this purpose. An *in-situ* pre-cleaning treatment (exposure to pure GeH_4) prior to p+ poly-$Si_{0.35}Ge_{0.65}$ deposition was found to be helpful for reducing ρ_c. The most dramatic improvement in contact resistivity is achieved by capping the metal with a thin Ni layer, so that an intermediary germanosilicide layer is formed between the metal and the $Si_{1-x}Ge_x$ film during the $Si_{1-x}Ge_x$ deposition procedure. This yields a very low contact resistivity of $10^{-7}\Omega$-cm^2, which is suitable for forming low-resistance contacts between the MEMS and CMOS. The results of this study reveal that it is possible to achieve specific contact resistivity in the acceptable range of $10^{-6}\Omega$-cm^2 (and even lower), which is needed for modularly integrated MEMS devices (**Chapter 2**) [6.2].

6.1.2. Boron doping effect on structural SiGe MEMS technology

An extensive study on *in-situ* boron doping effect on the chemical, electrical, and mechanical properties of poly-Ge sacrificial layer as well as poly-$Si_{1x}Ge_x$ structural films was performed and results have been presented in **Chapter 3** [6.3]. For LPCVD p+Ge sacrificial films, *in-situ* B doping is beneficial for improving the deposition and etch rate, as well as the surface smoothness. However, structural poly-$Si_{1-x}Ge_x$ films become more compressive, and show a slight increase in strain gradient, with increasing B content above $5x10^{-20}cm^{-3}$. Analytical models fit to the experimental data for conductivity, residual stress, and strain gradient have been generated as a guide for co-optimization of

B and Ge content. Finally heavy B doping does not increase the etch rate of poly-$Si_{1-x}Ge_x$ structural films in heated H_2O_2 solution, as long as the Ge content is below 65%, so that high etch selectivity can be maintained for p+Ge sacrificial material. XRD results performed in as-deposited and annealed p+$Si_{1-x}Ge_x$ samples show that an improvement in microstructure with annealing temperature appears to lead to an improvement in Q observed in low frequency comb-drive devices, rather than a reduction in segregated B dopant atoms.

6.1.3. SiGe MEMS applications

Two micromachined systems using $Si_{1-x}Ge_x$ MEMS technology have been presented in **Chapter 4**. First, a process flow (commonly called "Ge blade" process) that uses p+ germanium ashing technique to define nanometer lateral gaps, necessary for the reduction of the motional resistance in electrostatic MEMS resonators has been demonstrated. Lateral gap dimension between the proof-mass and the sense and drive electrodes ranging from 40nm to 100nm have been achieved [6.4]. Secondly, a SiGe levitating MEMS inertial sensor system was proposed to reduce the anchor loss mechanism in inertial sensor applications. For this purpose, a freely moving disk enclosed by drive and sense electrodes using p+ $Si_{1-x}Ge_x$ films as the structural layer and LTO as the sacrificial layer was successfully fabricated using a multilayered SiGe surface micromachining process [6.5]. The sensor system is comprised of a disk-shaped proof mass that is to be electrostatically suspended between sense and drive electrodes located above, below, and at the sides of the disk. An attractive feature of this design is that the proof mass is not structurally linked via a suspension, so that mechanical losses

associated with anchors are eliminated. As a demonstration of the sensing aspect of the system, a feedback control loop that inputs a sinusoidal wave function and outputs a linear function through a RMC-DC converter was designed for the sensing mechanism of the device. Electrical responses showed a vertical displacement motion of the disk between the lower electrodes and upper electrodes, with the disk released at a bias ~ 25.65 Volts. These results are promising and indicate that the disk is indeed free to move in place, and can be used as a MEMS acceleration sensor system with an estimated resolution sensitivity of 0.01 Å / $\sqrt{Hz}$ (assuming a standard differential circuit sensitivity ~ 1aF / $\sqrt{Hz}$).

6.1.4. Multilayer modeling of copper-based MEMS structures

Stress gradient issues associated with building MEMS devices using conventional back-end-of-line (BEOL) materials and layers compatible with IC interconnects technology have been addressed in **Chapter 5** [6.6]. Stresses inherent in these layers are of little significance for integrated circuits, but when creating released structures, strain gradients become critical for optimum device operation. For copper-based MEMS structures, it was found that the highly compressive TaN/Ta adhesion and barrier layer caused deflection of the MEMS structures. A closed-form solution of elastic beam deformation suitable for multilayer cantilever beams fabricated along with copper-based MEMS structures has been derived and used to assess copper effects on the reliability properties of these RF MEMS switches structures. Reducing the adverse effects of deformation of multi-layered MEMS cantilever switches would imply meeting design

goals for a lower actuation voltage, improved switch performance and manufacturing yield following subsequent packaging steps.

6.2. Recommendations for future work

6.2.1. Reliability of $Si_{1-x}Ge_x$ MEMS technology

Since poly-SiGe MEMS technology is fairly recent compared to the more mature poly-silicon MEMS technology, there has not been much work on the reliability of SiGe micromachined structures. Therefore, the unknown reliability of SiGe MEMS devices could limit their incorporation into commercial products.

It is clear that the long-term stability of MEMS devices can only be insured with greater knowledge of the basic properties and failure mechanisms of the materials employed in MEMS designs [6.7]. There are numerous properties that need to be measured for each MEMS material, including elastic modules, yield strength, fracture toughness, fatigue resistance, corrosion resistance, creep behavior, and residual stress. Still, there is very limited data available on the properties and long-term performance of these $Si_{1-x}Ge_x$ MEMS alloys, including fatigue-induced fracture, crack propagation, corrosion resistance, fracture toughness and creep resistance.

For fatigue-induced fracture testing, it is necessary to stress a targeted device at relatively high frequencies until fracture occurs. This is made possible by using a notched cantilever beam that is in turn attached to a large perforated plate which serves as the resonant mass (**Figure 6.1**). The mass and beam are electrostatically forced to resonate and the resulting motion is measured capacitively. On the opposite side of the mass, are interdigitated fingers for electrostatic actuation. The stress-life fatigue behavior of

polycrystalline silicon films deposited through the MUMPS foundry process has been investigated by *C. Muhlstein* using the same structure [6.8]. One of the main result from this work reasons that crack growth that caused fatigue-induced fracture occurs due to environmentally assisted cracking in the amorphous SiO_2 layer. In the case of poly-$Si_{1-x}Ge_x$ MEMS films, GeOx is not as stable as SiO_2 [6.9]; therefore it is expected that the crack propagation mechanism observed with the thin native oxide layer of poly-Si MUMPS film would be negligible at the GeOx interface, so that fatigue-induced fracture would occur at larger load stress or through a different mechanism. Therefore, it will certainly be worthwhile to do a systematic study of fatigue behavior in $Si_{1-x}Ge_x$ structural films in order to compare their stress-life behavior to their poly-Si counterparts.

Other reliability tests should aim to understand how SiGe MEMS devices fail when submitted to extreme thermal or/and load conditions, with the ultimate goal to assert how these failures will occur in real life applications and provide recommendations as of how to remedy or design around them. Such test includes: thermal shock test, drop test, temperature cycling test, operation and non-operational test, vibration test. Detailed description of these tests has been provided by the ASTM Standards [6.10].

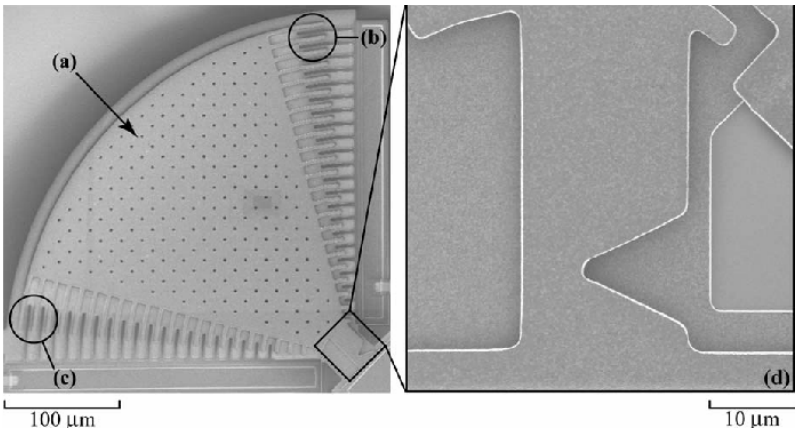

Figure 6.1: SEM of a fatigue life characterization test structure
(a) Proof-mass, **(b)** Comb-drive actuator, **(c)** Capacitive displacement sensor and **(d)** notched cantilever specimen are shown.

6.2.2. Thermal budget of the $Si_{1-x}Ge_x$ Structural Layer

Technological innovation has accomplished remarkable progress in the semiconductor industry and CMOS scaling into the nanometer regime. For instance, the state of the art CMOS technology makes used of copper damascene interconnects technology for the reduction of the interconnects resistance as well as the eradication of the electromigration problem often encountered with back-end-process that uses Al interconnects. Moreover, high k materials are now required as MOS structures are getting into the nanometer range because the conventional SiO_2 has become too thin (~2nm) to minimize the tunneling current as well as the out-diffusion of boron from the gate. Finally, novel low k materials will be needed to reduce the RC delay in modern IC electronics by either lowering the interconnect wire resistance, or by reducing the capacitance of the ILD (Inter-level Dielectrics). Many of these non-conventional low-k and/or high-k VLSI materials may require "Post-CMOS" processing with thermal budget lower than 400ºC for the monolithic integration of MEMS structures with the state-of-art VLSI-CMOS electronics.

In this work, all the $Si_{1-x}Ge_x$ structural films were deposited at temperatures greater than 400ºC in order to insure the attainment of polycrystalline films structures. However in the future, it would be critical to investigate $Si_{1-x}Ge_x$ structural layer deposition conditions at temperature below 400ºC (and even 350ºC) to meet the stringent thermal requirement of the state-of-the-art VLSI-CMOS technology for the achievement of a robust modularly integrated technology portable to all IC platforms. The approach

adopted by the SiGe research group at IMEC is to use a PECVD process to deposit the poly-$Si_{1-x}Ge_x$ structural films at temperatures below 370ºC [6.11].

To realize a LPCVD polycrystalline SiGe MEMS technology well below 400ºC, further optimization of deposition parameters such as pressure, doping and gas flow rates as well as source gases need to be performed. This will allow using the latest technology the IC industry has to offer and placing the MEMS directly on top of it, instead of worrying about thermal budget compatibility every time the electronics industry updates its processes.

6.2.3. Packaging of SiGe MEMS technology using porous $Ge/Si_{1-x}Ge_x$

The early focus on the development of MEMS has been on device design. Now that MEMS are being commercialized at an increasing rate, the focus is on delivering a robust and cost-sensitive product. Therefore, packaging has become a major way to differentiate between products. Moreover, the cost of undertaking this activity is receiving greater attention by manufacturers; typically, the cost of packaging can vary from 33% to 45% of the products' total cost [6.7]. To date, most of the packaging technologies require high thermal budgets, which is unacceptable for a "Post-CMOS" compatible modular integration technology. The idea of vacuum encapsulation of $Si_{1-x}Ge_x$ integrated MEMS structures was initially investigated by *Jong-Woo Shin* (former visiting scholar from *Samsung Inc.* at BSAC). It entails the usage of a poly- $Si_{1-x}Ge_x$ shell which allows release of the MEMS structures through a porous window [6.12]. The advantage of such a technology over others include: low temperature process (using $Si_{1-x}Ge_x$ MEMS technology), minimization of release time (which is important for the case of nano-gap

resonators), and the non-penetration of the deposited sealing material inside the package. Electrochemical etching of $Si_{1-x}Ge_x$ film was investigated, and porous membrane was formed in both HF and HCl based electrolytes. However, process integration of porous membranes and poly-$Si_{1-x}Ge_x$ MEMS devices still needs to be explored and optimized.

6.2.4. Electrostatic levitation of $Si_{1-x}Ge_x$ MEMS sensor system

One of the main hurdles encountered during the fabrication of the SiGe FLEMS inertial sensor devices was stiction between the upper electrodes and the disk. To prevent this stiction problem, an additional mask set consisting of dimples could have been designed and used after the CMP procedure of the second sacrificial LTO layer in order to create dimples on the top electrodes that would act as stoppers. Further investigations on novel anti-stiction coatings are also worthwhile investigating.

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Appendix A
Process Parameters

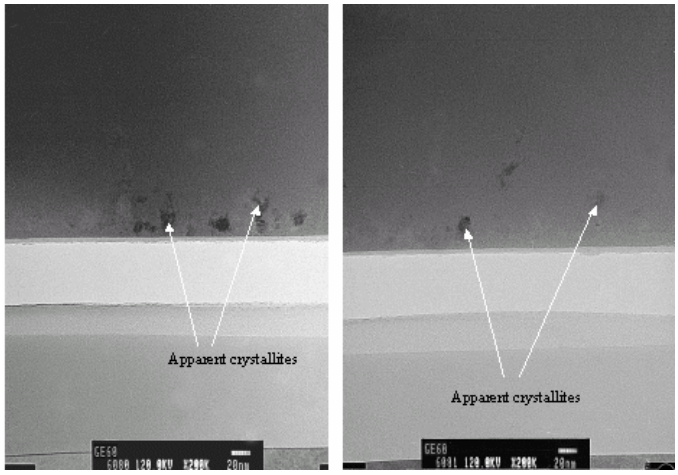
A1: Processing parameters of all $Si_{1-x}Ge_x$ films deposited using B_2H_6 doping source in chapter 2&3

Date	Temp (ºC)	Press (mTorr)	SiH4 (sccm)	GeH4 (sccm)	B2H6 (sccm)	Ge (%)	[B] (cm^{-3})
9/16/2003	425	600	100	60	60	77	1.00E+21
9/16/2003	425	400	0	180	60	100	5.00E+21
9/16/2003	425	400	100	60	60	63	1.00E+21
9/17 /2003	425	400	100	60	60	63	1.00E+21
9/17/2003	425	400	0	180	0	100	5.00E+21
9/17/2003	425	400	100	60	60	63	1.00E+21
10/14/2003	425	400	100	45	60	68	6.00E+20
9/14/2003	425	400	0	170	60	100	5.00E+21
9/14/2003	425	400	100	45	60	68	6.00E+20
11/20/2003	425	400	125	35	10	60	3.60E+19
11/20/2003	425	400	120	40	15	60	1.00E+20
11/20/2003	425	400	115	45	20	63	1.30E+20
11/20/2003	425	400	110	50	25	65	1.90E+20
12/11/2003	425	400	115	45	15	59	8.40E+19
12/11/2003	425	400	115	45	60	62	4.50E+20
1/12/2004	425	400	115	45	60	60	5.70E+20
1/15/2004	425	400	100	60	60	66	8.00E+20
1/29/2004	425	400	120	40	15	57	6.50E+19

A2: TEM cross section and deposition conditions of p+Ge amorphous layer

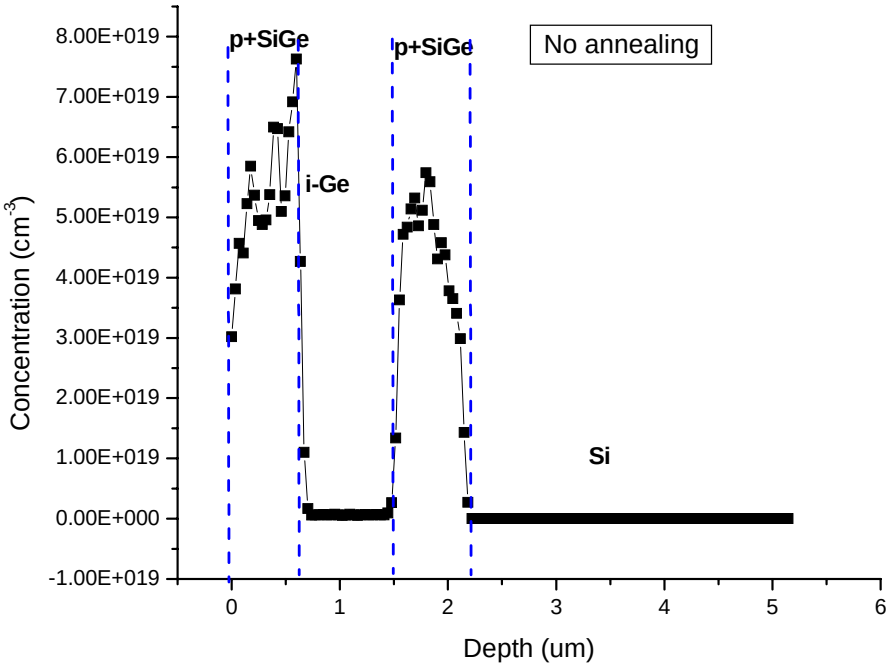
Recipe for α-Ge:

P=300mtorr
T=350°C
SiH4=0sscm
GeH4=170sscm
B2H6=60sscm
R=0.6mΩ-cm

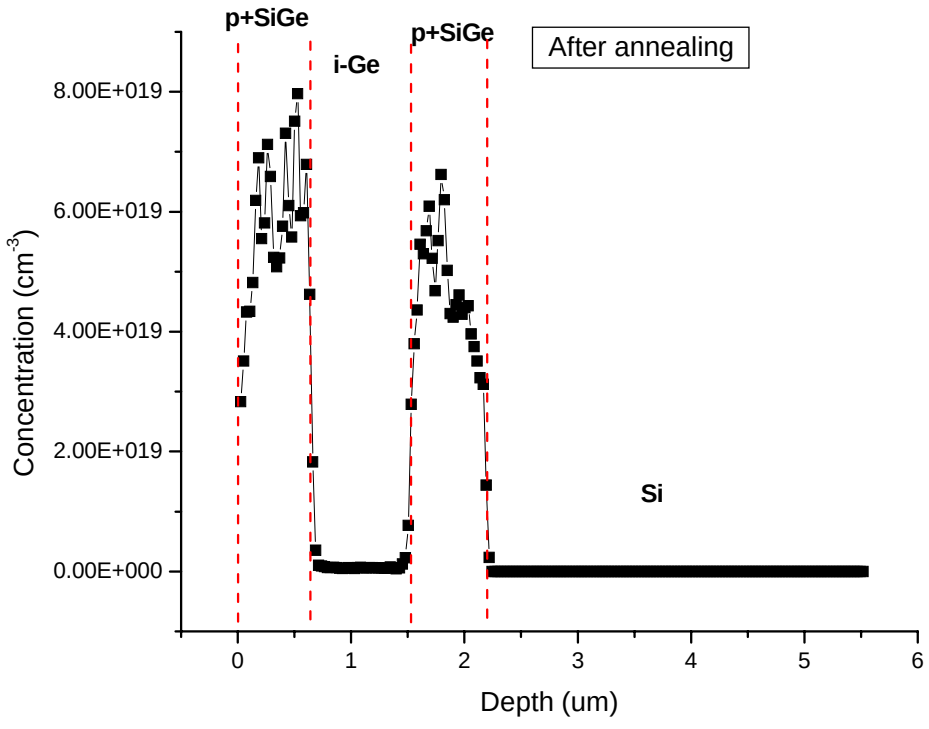


Appendix B
Spreading Resistance Profile (SRP) Results of Boron Content

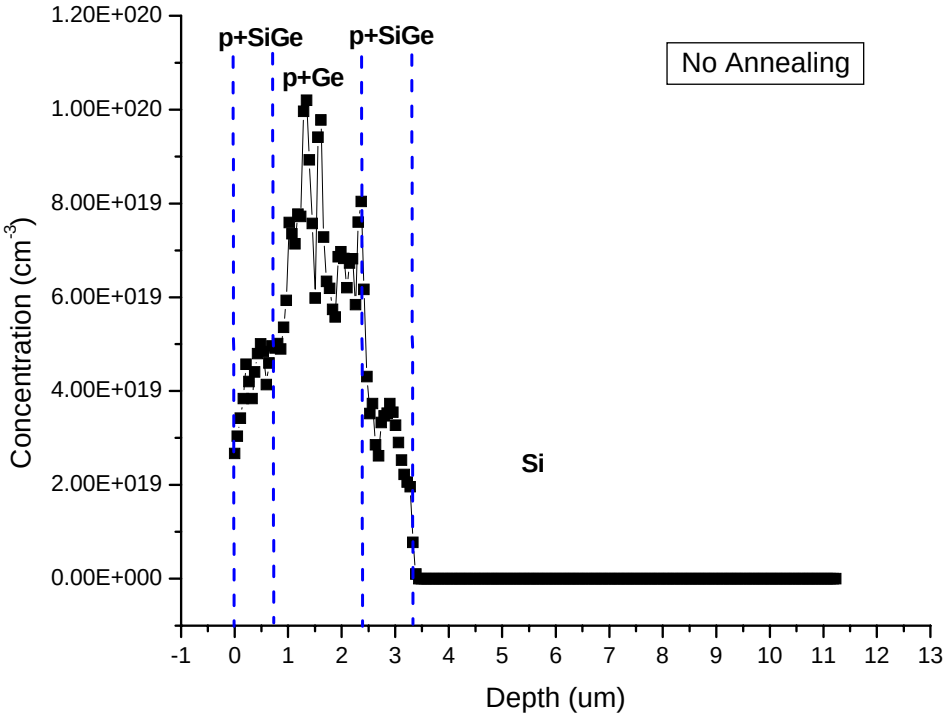
B1: SRP of $p+Si_{1-x}Ge_x$/i-Ge/$p+Si_{1-x}Ge_x$ tri-layer

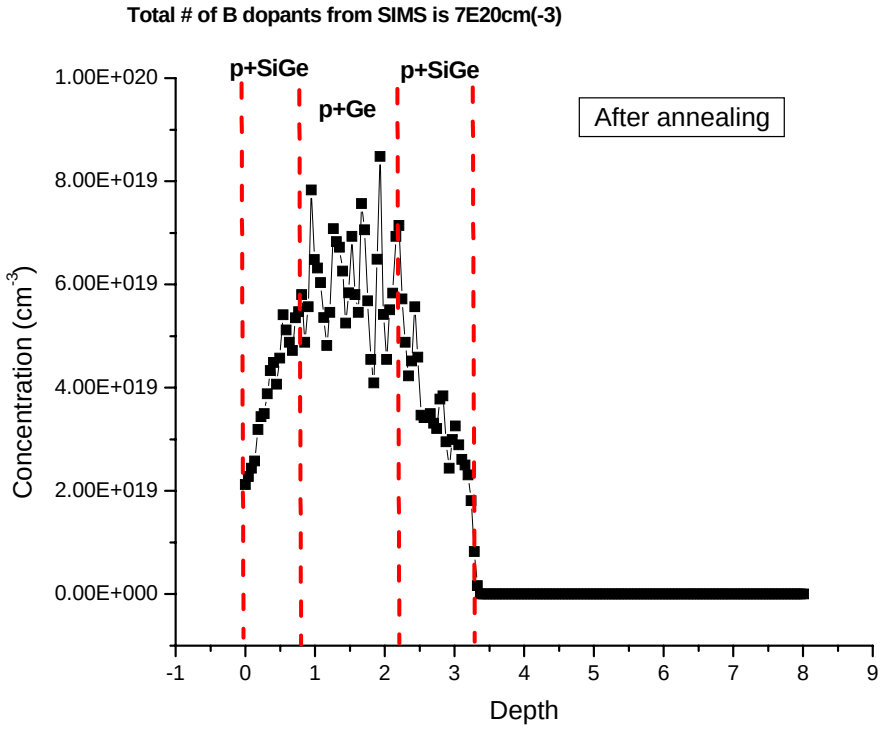


Total # of B dopants from SIMS is 1E21cm(-3)



B2: SRP of $p+Si_{1-x}Ge_x/p+Ge/p+Si_{1-x}Ge_x$ tri-layer





Appendix C
FLEMS Fabrication Details

C1: Detailed Fabrication Process Flow of the FLEMS Devices

The process flow and modules described below are specific to the University of California Berkeley (UCB) Microfabrication Laboratory. Although the equipment names and recipes listed are unique to UCB, the processing parameters and equipment are general.

Step	Process	Conditions	Equipments	Comments
	Bare Wafers	6" p-type prime wafers		
0	**LABELING**			
0.1	Label		Dimaond Pencil	
0.2	DI Rinse	3 Cycle DI Water Rinse	sink6	
0.3	HF Cleaning	10:1 HF 5min	sink6	
1	**Deposition of LTO**			
1.0	Deposition of LTO	Standard undoped LTO, T=450C, fixed SiH4 and 02	Tystar12	Receipe=12SULTOA, Dep rate=150A/min
1.1	Measurement		NanoDUV	2microns
2	**Deposition of SiN**			
2.0	Deposition of SiN	T=750C, P=140mtorr,DCS=100sccm, NH3=25sccm, Dep. Rate=1100A/min	Tystar17	Receipe=17SNSTDA
2.1	Meausrement		NanoDUV	200nm
3	**Deposition of ground plane (SiGe0)**			
3.1	Piranha cleaning	120C 10min, 3 cycle DI water rinse	sink 8 & sink 6	
3.2	Native Oxide removal	HF Dip	sink 6	
3.3	Seed layer	T=425C, P=600mtorr, SiH6=100, time=10min	tystar20	
3.4	SiGe0 deposition	T=425C, P=600mtorr, BCL3/SiH4/GeH4=12/120/45sccm	tystar20	0.7microns
4	**Definition of bottom electrodes (SiGe0)**			
4.1	HMDS and PR	I-Line PR, 90C soft bake	svgcoat6	receipe: HMDS-1, OIR 897 10i (I line)
4.2	Expose	Exposure=2.2sec, Focus=0	Gcaws6	
4.3	Post exp. bake and develop	90C 1min	svgdev6	receipes: bake - 3; developer OPD 4262
4.4	Hard bake	140C 1min with UV	uvbake	recipe: U
4.5	SiGe etch	Coil=1500W, Biais=30W, P=75mtorr, HBR=125sccm, CL2=75sccm, Pulsing CW	Centura-DPS	Receipe:variable, Etch rate=0.8um/min
4.6	Measurement		asiq	step height=0.7microns
5	**Low Temperature Oxide Sacrificial 1**			
5.1	Di water rinse	3 Cycle DI Water Rinse	sink 8 & sink 6	
5.2	Native Oxide removal	HF Dip	sink 6	
5.3	LTO deposition	Standard undoped LTO, T=450C, fixed SiH4 and 02	Tystar12	Receipe=12SULTOA, Dep rate=150A/min
5.4	Thickness measurement		nanoduv	2microns
5.5	CMP	DF=9Psi, Table/Chuck=33/15rpm, BP=1psi, Slurry=100ml/min, CMP rate=225nm/min	CMP tool	
5.6	Post cleaning	Di Rinse, SVC14-90C	sink5-sink8	

Step	Process	Conditions	Equipments	Comments
6	**Deposition of proof-mass layer (SiGe1)**			
6.1	Metal organic cleaning	SVC14-90C 15min, 3 cycle DI water rinse	Manual bath	
6.2	SiGe1 depo. (Bottom layer)	T=425C, P=600mtorr, BCL3/SiH4/GeH4=12/105/70sccm	tystar20	Dep rate=90A/min
6.3	SiGe1 depo. (Top layer)	T=410C, P=600mtorr, BCL3/SiH4/GeH4=12/130/45sccm	tystar20	Dep rate=60A/min
7	**Definition of proof-mass layer (SiGe1)**			
7.1	HMDS and PR	I-Line PR, 90C soft bake	svgcoat6	receipe: HMDS-1, OIR 897 10i (I line)
7.2	Expose	Exposure=3.35sec, Focus=-4	Gcaws6	
7.3	Post exp. bake and develop	90C 1min	svgdev6	receipes: bake - 3; developer OPD 4262
7.4	Hard bake	120C for 16 hours	Oven	
7.5	SiGe etch	Coil=1200W, Biais=10W, P=40mtorr, SF6=250sccm, C4F8=300sccm, Pulsing CW	Centura-DPS	Receipe:Si-Deep 1A, Etch rate=1.3um/min
7.6	Measurement		asiq	step height=4.1microns
8	**Low Temperature Oxide Sacrificial 2**			
8.1	Di water rinse	3 Cycle DI Water Rinse	sink 8 & sink 6	
8.2	Native Oxide removal	HF Dip	sink 6	
8.3	LTO deposition	Standard undoped LTO, T=450C, fixed SiH4 and 02	Tystar12	Receipe=12SULTOA, Dep rate=150A/min
8.4	Thickness measurement		nanoduv	2microns
8.5	CMP	DF=9Psi, Table/Chuck=33/15rpm, BP=1psi, Slurry=100ml/min, CMP rate=225nm/min	CMP tool	
8.6	Post cleaning	Di Rinse, SVC14-90C	sink5-sink8	
8.7	Thickness measurement		asiq	1.2micron
9	**Deposition on anchor layer (SiN)**			
9.1	Metal organic cleaning	SVC14-90C 15min, 3 cycle DI water rinse	Manual bath	
9.2	Native Oxide removal	HF Dip	sink 6	
9.3	PECVD SiN	T=350C, P=0.9torr, RF=25W, NH3=200sccm, SiH4=40sccm, Ar=200sccm	Oxford PECVD tool	
9.4	Thickness measurement	SiN (Monitor wafer)	nanoduv	3000A
10	**Definition of anchor layer (Anchor)**			
10.1	HMDS and PR	I-Line PR, 90C soft bake	svgcoat6	receipe: HMDS-1, OIR 897 10i (I line)
10.2	Expose	Exposure=2.6sec, Focus=-3	Gcaws6	
10.3	Post exp. bake and develop	90C 1min	svgdev6	receipes: bake - 3; developer OPD 4262
10.4	Hard bake	140C 1min with UV	uvbake	recipe: U
10.5	SiN etch	Power=450W, P=50mtorr, CF4=20sccm, CHF3=15sccm, O2=8sccm, Ar=110sccm	Centura MXP	Receipe:MXP=Nitride, Etch rate=2600A/min
10.6	Measurement		asiq	3000A
11	**Deposition of top electrodes layer (SiGe2)**			
11.1	Metal organic cleaning	120C 10min, 3 cycle DI water rinse	sink5-sink8	
11.2	Native Oxide removal	HF Dip	sink 6	
	SiGe2 depo. (Bottom layer)	T=425C, P=600mtorr, BCL3/SiH4/GeH4=12/105/70sccm	tystar20	Dep rate=90A/min
11.3	SiGe2depo. (Top layer)	T=410C, P=600mtorr, BCL3/SiH4/GeH4=12/130/45sccm	tystar20	Dep rate=60A/min
12	**Definition of top electrodes layer (SiGe2)**			
12.1	HMDS and PR	I-Line PR, 90C soft bake	svgcoat6	receipe: HMDS-1, OIR 897 10i (I line)
12.2	Expose	Exposure=2.6sec, Focus=-2	Gcaws6	
12.3	Post exp. bake and develop	90C-1min	svgdev6	receipes: bake - 3; developer OPD 4262
12.4	Hard bake	120C for 12 hours	Oven	
12.5	SiGe etch	Coil=1500W, Biais=30W, P=75mtorr, HBR=125sccm, CL2=75sccm, Pulsing CW	Centura-DPS	Receipe:variable, Etch rate=0.8um/min
12.6	Measurement		asiq	step height=1.6microns
13	**Release Module**			
13.1	Release	T=40C, Etch rate=30microns for 50minutes	Hf Vapor	
13.2	Check for complete release		Probe station	Move disk around to check for complete release
14	**Testing**			
14.1	Short/Open	Testing for short and open between electrodes	Probe station	No short was observed
14.2	Sensing/Control	Use electronics setup to sensing/controlling of the disk	Sensing electronics	Sensing was succesfully achieved

Appendix D
Program

D1: MATLAB code of copper-based multilayer beam model

```
clear all
close all
% Constants/Material Properties (1:SiN, 2:Cu, 3:TaN, 4:Ta, 5:SiN)
% Material properties for SiN bottom layer
E1_p= 184E9; % Pa
S1_p= -173E6; % Pa
t1=0.07E-6; % m
v1=0.24; % non dimensional
a1=1.6;

%E1_p= 70E9; % Pa
%S1_p= -10E6; % Pa
%t1=0.07E-6; % m
%v1=0.17; % non dimensional
%a1=1.6;

% Material properties for TaN
E2_p= 240E9; % Pa  (For ALD TaN, E=320E9Pa)
S2_p= -2200E6; % Pa
t2=0.01E-6; % m
v2=0.34; % non dimensional
a2=9.3;

% Material properties for Ta
E3_p= 186E9; % Pa
S3_p= -2200E6; % Pa
t3= 0.02E-6; % m
v3=0.34; % non dimensional
a3=6.3;

% Material properties for Cu
E4_p= 110E9; % Pa
S4_p= 70E6; %
t4=1.0E-6; % m
v4=0.34; % non dimensional
a4=16.6;
```

```
% Material properties for SiN top layer
E5_p= 184E9; % Pa
S5_p= 50E6; % Pa
t5=0.07E-6; % m
v5=0.24; % non dimensional
a5=1.6;

%E5_p= 70E9; % Pa
%S5_p= -10E6; % Pa
%t5=0.07E-6; % m
%v5=0.17; % non dimensional
%a5=1.6;
w=20E-6; % m
L=100E-6;% m
Dt=10;

% Elastic modulus for bi-axial stress (used for a beam like structure)
E1 = E1_p;
E2 = E2_p;
E3 = E3_p;
E4 = E4_p;
E5 = E5_p;

%E1 = E1_p/(1-v1);
%E2 = E2_p/(1-v2);
%E3 = E3_p/(1-v3);
%E4 = E4_p/(1-v4);
%E5 = E5_p/(1-v5);

% Stress for bi-axial stress (used for a beam like structure)
%S1 = S1_p;
%S2 = S2_p;
%S3 = S3_p;
%S4 = S4_p;
%S5 = S5_p;

S1 = S1_p*(1-v1);
S2 = S2_p*(1-v2);
S3 = S3_p*(1-v3);
S4 = S4_p*(1-v4);
S5 = S5_p*(1-v5);
```

```
%Compute the variables
A1=E1*t1^2+E2*(t2^2-t1^2)+E3*(t3^2-t2^2)+E4*(t4^2-t3^2)+E5*(t5^2-t4^2);
B1=E1*t1+E2*(t2-t1)+E3*(t3-t2)+E4*(t4-t3)+E5*(t5-t4);
C1=-1*((S1*t1)+S2*(t2-t1)+S3*(t3-t2)+S4*(t4-t3)+S5*(t5-t4));
%C1=-1*((1-v1)*S1*t1+(1-v2)*S2*(t2-t1)+(1-v3)*S3*(t3-t2)+(1-v4)*S4*(t4-t3)+(1-
v5)*S5*(t5-t4));
%C1=((a1*Dt)-(1-v1)*S1*t1)+((a2*Dt)-(1-v2)*S2*(t2-t1))+((a3*Dt)-(1-v3)*S3*(t3-
t2))+((a4*Dt)-(1-v4)*S4*(t4-t3))+((a5*Dt)-(1-v5)*S5*(t5-t4));

A2=E1*t1^3+E2*(t2^3-t1^3)+E3*(t3^3-t2^3)+E4*(t4^3-t3^3)+E5*(t5^3-t4^3);
B2=E1*t1^2+E2*(t2^2-t1^2)+E3*(t3^2-t2^2)+E4*(t4^2-t3^2)+E5*(t5^2-t4^2);
C2=-1*((S1*t1^2)+S2*(t2^2-t1^2)+S3*(t3^2-t2^2)+S4*(t4^2-t3^2)+S5*(t5^2-t4^2));
%C2=-1*((1-v1)*S1*t1^2+(1-v2)*S2*(t2^2-t1^2)+(1-v3)*S3*(t3^2-t2^2)+(1-
v4)*S4*(t4^2-t3^2)+(1-v5)*S5*(t5^2-t4^2));
%C2=((a1*Dt)-(1-v1)*S1*t1^2)+((a2*Dt)-(1-v2)*S2*(t2^2-t1^2))+((a3*Dt)-(1-
v3)*S3*(t3^2-t2^2))+((a4*Dt)-(1-v4)*S4*(t4^2-t3^2))+((a5*Dt)-(1-v5)*S5*(t5^2-t4^2));

x1=(A2*B2)/(4*B1)-(A2/3);
y=C2-(C1*B2)/(2*B1);
% Length = L;
x = 0:2E-6:L;

%Calculation of curvature
k= (y/x1)
c=((A2*k)+(2*C1))/(2*B1)
rad_curvature = (1/k)
Beam_Shape2 = (0.5*k*(x).^2);
Deflection_tip = 0.5*(k*1E6)*L^2

%Experimental plots
x = 0:2E-6:L;
k1=0.00131;
r1=1/k1;
y1 = 0.5*r1*(x).^2;
%%
x = 0:2E-6:L;
k2=0.0055;
r2=1/k2;
y2 = 0.5*r2*(x).^2;

% Circular expression for beam profile:
% b = R - (R^2 - a.^2).^0.5;
% TipHeight = (RadCurvature_Stress - (RadCurvature_Stress^2 - x.^2).^0.5);
% TipHeightL = (RadCurvature_Stress - (RadCurvature_Stress^2 - L.^2).^0.5)/1E-6
```

```
 Meas_Data = csvread('c:/csv/imap20x250/MPCB20x250x.csv');
 MeasX   = Meas_Data(:,1);
 MeasY1   = Meas_Data(:,3);
% SimX   = Meas_Data(:,1);
% SimY   = Meas_Data(:,6);

figure(1);
hold on
plot (x/1E-6,Beam_Shape2./1E-6, '+g')
plot (x/1E-6,y1./1E-6, 'or')
%plot (x/1E-6,y2./1E-6, 'ob')
%plot (x/1E-6,TipHeight./1E-6, '+g')
%plot (MeasX,MeasY1, 'or')
title('Multilayer Beam Modeling','FontSize',16, 'FontName', 'IBM')
xlabel('IMAP Cantilever Beam Length (micron)','FontSize',14, 'FontName', 'IBM')
ylabel('Deformation (micron)','FontSize',14,'FontName', 'IBM')
axis([0 100 0 40])
grid off
h = legend('Multilayer Model', 'Measurements using PVD TaN', 2);
box
hold off
```