Technologies for enhancing multi-gate Si MOSFET performance

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ABSTRACT

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Doctor of Philosophy in Engineering –
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Suppression of short-channel effects (SCE) and reduction in device-to-device variability will be key challenges for transistor scaling in sub-45nm CMOS technologies. Multi-gate transistor structures such as the FinFET may eventually be needed to meet performance requirements in the sub-20nm gate length regime because SCE can be effectively suppressed without the need for high channel doping concentrations, resulting in enhanced carrier mobilities. However, these advanced device structures will likely require a metal gate technology that offers tunable work function to allow for threshold voltage (V_T) adjustment for proper CMOS circuit operation. Strained-Si has also been considered as a key technology for enhancing carrier mobilities via modification of the electronic band structure of the channel material. Optimization of the channel surface crystalline orientation can further increase on-state drive current (I_{on}), *e.g.,* electron mobility is highest for a (100) Si channel surface while hole mobility is highest for a (110) Si channel surface.

In this dissertation, various technologies for optimizing the performance of multi-gate Si MOSFETs are presented. Firstly, both symmetrical and asymmetrical double-gate MOSFET designs are considered and shown to be reasonably tolerant of process-induced variations. From device simulation results, it is found that both the SDG and ADG designs are reasonably tolerant of process-induced variations.

Secondly, a molybdenum gate technology with tunable effective work function for threshold-voltage adjustment is presented. With high-temperature forming-gas annealing (HTFGA), the work functions of Mo gate electrodes are successfully tuned in the range 4.6eV to 5.1eV. It is also found that the tuned work function of Mo by HTFGA is not retained during the subsequent source/drain activation annealing step unless a TiN capping layer is used to prevent nitrogen out-diffusion.

Finally, strain-induced mobility enhancement for multiple-gate (MuG) Si MOSFETs with optimized channel surface crystalline orientations for CMOS application ((100) NMOS and (110) PMOS, respectively) via a strained SOI substrate, strained SiN_x capping layer, tensile metal gate, and/or biaxial tensile wafer bending is discussed. The impact of strain on device performance is shown to be well modeled using the classic bulk-Si piezoresistance (PR) coefficients.

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Professor Tsu-Jae King Liu

Committee Chair

To my family and to the memory of my father

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Chapter 1 : Introduction

1.1 CMOS technology scaling

Since the innovative concept of an integrated circuit (IC) was invented by J. Kilby in 1958, the number of circuit components on a microchip has increased exponentially and the performance of a unit transistor has improved, resulting in incredible reductions in cost-per-function with enhanced performance. This has been enabled by the successful scaling, *i.e.,* miniaturization of geometrical parameters, of planar bulk-Si CMOS devices. Over the past four decades, the semiconductor industry has followed the trend first noted by G. Moore, *i.e.*, that the complexity of ICs approximately doubles every two years [1]. C. G. Hwang even suggested a new growth model for the memory industry: "a two fold increase per year in memory density [2]."

However, as the gate length (L_g) of a metal-oxide-semiconductor field-effect transistor (MOSFET) decreases, capacitive control of the channel potential by the gate becomes more difficult. This is because the drain potential can significantly influence the channel potential, resulting in severe short channel effects (SCE), such as increased off-state leakage current (I_{off}), threshold voltage (V_t) roll-off, *i.e.,* smaller V_t at shorter L_g, and drain-induced barrier lowering (DIBL), *i.e.,* smaller V_t at higher drain voltage (V_d) due to modulation of the source-channel potential barrier by the drain voltage. Above all, increased I_{off} is a severe concern that may limit CMOS scaling because of significant passive power consumption [3].

In order to suppress the SCE in bulk MOSFETs, other parameters have been scaled down together with L_g, such as the gate oxide thickness (T_{ox}), the channel depletion width (X_d), and the source/drain junction depth (X_j). However, the thickness of SiO_2-based gate dielectrics is approaching physical limits (<2nm), for which quantum mechanical tunneling induces severe gate leakage current through the gate dielectric [4]. Alternative gate dielectric materials with higher permittivity ("high-k gate dielectrics") can be used to further reduce the equivalent oxide thickness (EOT) with a physically thick dielectric to suppress gate leakage current. However, there are still many process integration challenges to be solved, including optimization of the interfacial layer to minimize carrier mobility degradation [5].

To scale down the depletion width, increased channel doping concentration is necessary. This reduces the off-state leakage current not only by increasing the channel potential relative to the source, which makes V_t high, but also by eliminating leakage current paths far from the gate dielectric interface. However, the high channel doping concentration degrades carrier mobility due to increased vertical electric field and more impurity scattering. It also increases band-to-band tunneling across the reverse-biased drain junction and gate-induced drain leakage (GIDL). In addition, statistical fluctuation of channel dopants causes more V_t variations, especially in the nanoscale regime [6].

Shallow source/drain junctions reduce the lateral junction capacitance, and thereby decrease the capacitive coupling of the source/drain to the channel. However, the formation of ultra-shallow junction depth is limited by process difficulties for low-energy ion implantation together with low thermal budget dopant activation to minimize dopant diffusion. The source/drain junction depth reduction can also increase parasitic series

resistance, resulting in degraded on-state drive current. Thus, raised source/drain technology is necessary to minimize parasitic series resistance.

Most of the scaling challenges faced by bulk-Si MOSFETs can be circumvented through the adoption of advanced MOSFET structures [7] such as ultra-thin-body (UTB) and double-gate (DG) silicon-on-insulator (SOI) MOSFETs described in the next section.

1.2 Advanced MOSFET structures

The off-state leakage current (I_{off}) increases as gate length (L_g) decreases because capacitive control of the channel potential by the gate becomes more difficult. Actually, the dominant leakage path is located far from the gate, which is least effectively controlled by the gate [8]. Therefore, advanced SOI MOSFETs with thin body thickness (T_{Si}) can suppress the leakage current by eliminating the part of the channel that is not effectively modulated by the gate (Fig. 1.1). However, an ultra-thin body (thinner than 50% of L_g) is necessary to effectively suppress the leakage current, which makes this approach technically challenging. The body thickness requirement for the double-gate (DG) MOSFET can be relaxed (to be 50% to 70% of L_g) due to enhanced channel control by the two gates.

In addition, the DG device does not require high channel doping to scale X_d because it is defined by the body thickness. As a result, mobility degradation and statistical dopant fluctuation problems can be eliminated. Similarly, X_j is also defined by the body thickness, thus the shallow junction can be realized relatively easily without developing complicated doping techniques. Therefore, the DG MOSFET is a promising structure for scaling CMOS into the sub-15nm L_g [9, 10].

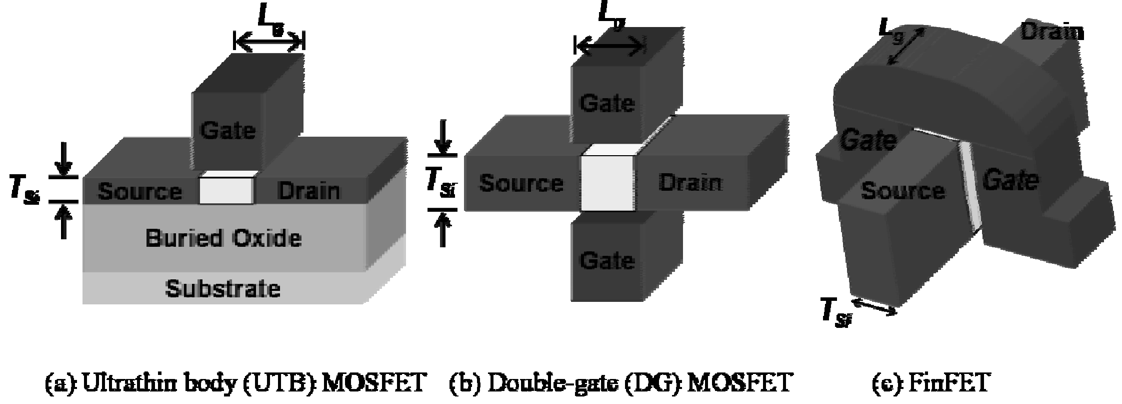

Figure 1.1: Advanced SOI MOSFET structures with a thin body thickness (T_{Si}).

However, the manufacturability of DG MOSFETs is still challenging. Many different methods have been proposed to fabricate DG devices but most of them suffer from technical challenges mainly due to the process complexity [11-21]. A FinFET is known to be the most manufacturable DG structure due to self-aligned gate electrodes compatible with conventional planar bulk CMOS process [14, 21]. In particular, a third gate can be easily implemented by utilizing the top surface of fin as a channel, which enables further relaxation of T_{Si} constraints [22].

1.3 Materials and process requirements for nanoscale CMOS

Advanced MOSFET structures such as the ultra-thin-body (UTB) MOSFET and the double-gate (DG) MOSFET are expected to be eventually adopted in CMOS technology nodes toward the end of the roadmap [10] due to improved control of short channel effects [23]. However, threshold voltage (V_T) adjustment for CMOS application will be difficult because the channel/body should be lightly doped ($< 10^{17}$ cm^{-3}) or

undoped in order to achieve high carrier mobilities and to minimize threshold-voltage (V_T) variations induced by channel dopant fluctuations.

In this case, a metal gate technology that offers tunable work function (Φ_M) for V_T adjustment is very desirable. In addition, metal gate enables further MOSFET scaling because it eliminates the issues of poly-Si gate technology, namely the gate depletion effect and boron penetration. The ranges of Φ_M required to fully adjust the V_T values of thin-body (fully depleted) MOSFETs for various applications is 4.4eV to 4.6eV for n-channel devices and 4.8eV to 5.0eV for p-channel devices [24]. Recently, A. Carlson *et al*. reported that a single metal gate technology with ~4.6eV work function should be advantageous for achieving large read and write margins in six-transistor (6-T) FinFET SRAM cells [25]. V. Varadarajan *et al*. showed that a single gate technology with near-midgap work function (~4.7eV) can be suitable for low-power DG CMOS technology, if fine-tuning of V_T is achieved by engineering the electrical channel length (L_{eff}) [26]. Thus, the ability to tune Φ_M near mid-gap should be useful for various applications.

To overcome the current geometrical scaling limit, the industry needs a new scaling vector. Strained Si technologies have been widely studied as a new promising scaling vector (mobility scaling) to improve on-state drive current without degrading off-state leakage current [27-37]. Mobilities of both electrons and holes can be improved by applying stress to induce appropriate strain in the channel, *e.g.,* tensile strain for n-channel MOSFETs and compressive strain for p-channel MOSFETs [33, 34]. To induce appropriate strain in the channel region of MOSFETs, various techniques have been introduced such as substrate-induced strain, process-induced strain, and bending-induced strain.

Optimization of channel surface crystalline orientations for maximum carrier mobilities can also provide for a significant improvement in CMOS performance [38]. Therefore, the ultimate CMOS technology will utilize each of these approaches (advanced MOSFET structures, metal gate with tunable Φ_M, strained Si, and channel orientation optimization) for performance enhancement.

1.4 Organization

In this dissertation, various technologies for optimizing the performance of multi-gate Si MOSFETs are investigated for the future nanoscale CMOS technologies. Key issues of double-gate MOSFET design for manufacturability are explored through device simulation and a new work function tuning method for Mo gate technology is demonstrated experimentally. Effects of strain on MuGFET performance are examined and modeled with classic bulk-Si piezoresistance (PR) coefficients [39].

Chapter 2 presents the effects of process induced parameter variations on the performance of DG MOSFETs. The differences in operation schemes of symmetric and asymmetric DG MOSFETs are briefly described by using energy band diagrams. The device performance sensitivity to process induced parameter variations such as body thickness (T_{Si}), gate length (L_g), gate oxide thickness (T_{ox}), and gate misalignment (MA) is also investigated for n-channel symmetric and asymmetric MOSFETs, via device simulation (ISE DESSIS).

In Chapter 3, Mo gate work function reduction by N^+ implantation is reviewed and issues for this approach are addressed. As an alternative approach to reduce Mo gate work function, the impact of HTFGA on Mo gate work function is investigated and

CMOS process integration issues are discussed. Finally, a theory for Mo gate work function reduction is presented.

The physics of strained Si is reviewed in Chapter 4 using electronic band structures and the simple piezoresistance model is also introduced to quantify mobility enhancement induced by strain.

In Chapter 5, the effects of strain on the performance of n-channel and p-channel MuGFETs with {110}/<110> and {100}/<100> surface-orientation/current-direction are investigated. Three typical types of strain (substrate-induced, process-induced, and bending-induced strains) for enhancing MuGFET performance are introduced. First, impact of strained SOI (sSOI) substrate on MuGFET performance is experimentally studied. For process-induced strain approaches, the impacts of a strained capping layer and tensile metal gate are then discussed. Finally, the impact of biaxial convex bending on MuGFET performance is presented. Mechanisms affecting carrier mobility in thin-body (fully depleted) MOSFET structures are also elucidated by using the PR model introduced in Chapter 4.

An overall summary of this dissertation is presented in Chapter 6. Key research contributions and suggestions for future research directions are highlighted.

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Chapter 2 : Double-Gate MOSFET Design for Manufacturability

2.1 Introduction

For the past four decades, the cost-per-function and the performance of integrated circuits have been dramatically improved by successful scaling of planar bulk Si CMOS devices. However, as the gate length (L_g) decreases, the capacitive control of the channel potential by the gate becomes more difficult. Instead, the source and drain influence significantly the channel potential, resulting in severe short channel effects (SCE), such as increased off-state leakage current (I_{off}), threshold voltage (V_t) roll-off, *i.e.,* smaller V_t at shorter L_g, and drain-induced barrier lowering (DIBL), *i.e.,* smaller V_t at higher drain voltage (V_d) due to modulation of source-channel potential barrier by the drain voltage.

In order to suppress the SCE in bulk devices, other parameters have been scaled down together with L_g, such as the gate oxide thickness (T_{ox}), the gate-controlled channel depletion width (X_d), and the source/drain junction capacitance (X_j).

A thin gate oxide increases the capacitive control of the channel by the gate. Therefore, the influence on the channel by the source/drain becomes relatively small. At the same time, more inversion charges are induced by T_{ox} scaling, resulting in higher on-state drive current (I_{on}). However, the thickness of SiO_2-based gate dielectric is already

approaching down to almost physical limit (<2nm), where the quantum mechanical gate tunneling induces severe gate leakage current through the gate dielectric [1]. The alternative high-κ gate dielectric is known to further reduce the equivalent oxide thickness (EOT) with a large physical dielectric thickness, which suppresses gate leakage current. However, in order to apply high-κ gate dielectric especially for sub-1nm EOT devices, there are still a lot of technical challenges including engineering of the interfacial layer degrading the carrier mobility [2].

To scale the gate-controlled depletion width, increased channel doping concentration is necessary, which reduces the off-state leakage current not only by increasing the channel potential relative to the source, which makes V_t high, but also by eliminating leakage current paths far from the gate dielectric interface. In particular, the locally high channel doping concentration near the source/drain regions has been widely implemented via lateral channel engineering such as halo or pocket implants [3, 4], which also increases the average channel doping concentration especially for sub-100nm L_g devices. However, the high channel doping concentration degrades carrier mobility due to increased vertical electric field and more impurity scattering. It also increases band-to-band tunneling across the junction and gate-induced drain leakage (GIDL). In addition, statistical fluctuation of channel dopants causes more V_t variations, especially for the nanoscale regime [5].

Shallow source/drain junctions reduce the junction capacitance, thereby decreasing the capacitive coupling of the source/drain to the channel. However, the formation of ultra-shallow junction depth is limited by the process difficulties in low-energy ion implantation together with low thermal budget dopant activation to minimize

dopant diffusion. The source/drain junction depth reduction also increases parasitic series resistance, resulting in degraded on-state drive current. The raised source/drain technology is necessary to minimize the parasitic series resistance.

The double-gate (DG) MOSFET is a promising structure for scaling CMOS into the sub-15nm L_g regime because of its excellent suppression of short channel effects (SCE) for a given equivalent gate-oxide thickness [6, 7]. For example, the DG device doesn't need to have high channel doping to scale X_d because it is defined by body thickness, which is normally 50 to 70% of L_g to suppress the SCE effectively. As a result, mobility degradation and statistical dopant fluctuation problems can be eliminated. Similarly, X_j is also defined by the body thickness, thus the shallow junction can be realized relatively easily without developing complicated junction implantation techniques.

Even though DG device structures can effectively suppress SCE due to aforementioned superiorities of DG devices over the conventional planar bulk MOSFETs, their manufacturability is still challenging. Many different methods have been proposed to fabricate DG devices but most of them suffer from technical challenges mainly due to the process complexity [8-18]. For example, the vertical devices with pillar-like channel [14-17] has a large gate overlap capacitance and the required processes are very complicated. In particular, it is not easy to have different gate lengths which are controlled by deposition thicknesses and/or etch back amounts. A FinFET is also a vertical device, the most manufacturable DG structure due to process compatibility with conventional planar bulk MOSFETs [11, 18]. However, the channel surface (fin sidewall) roughness induced by photolithography and dry etching degrades carrier mobilities

without subsequent surface smoothening process [18]. Since the effective channel widths are controlled by the number of fins, the independent control for two gates is almost impossible with limited physical spacing between fins required for layout efficiency, even though the gate separation process is available [15]. Independent gate control is relatively easy for the planar DG devices but it is not trivial to align the front and back gates without complicated process integration [8-10, 12, 13]. Above all, the performance fluctuation induced by process induced parameter variations is expected to be more significant for DG devices because nominal device parameters are already restricted to be very small.

In this chapter, the effects of process induced parameter variations on the performance of DG MOSFETs are presented [19, 20]. First, the differences in operation schemes of symmetric and asymmetric DG MOSFETs are briefly described by using energy band diagrams. Secondly, the device performance sensitivity to process induced parameter variations such as body thickness (T_{Si}), gate length (L_g), gate oxide thickness (T_{ox}), and gate misalignment (MA) is investigated for n-channel SDG and ADG MOSFETs with nominal gate length of 13nm and light body doping, via device simulation (ISE DESSIS).

2.2 Symmetric vs. Asymmetric Structures

As shown in Fig. 2.1, there are two types of DG MOSFETs: 1) symmetric (SDG), in which the gates have identical work function (Φ_M, intermediate to N^+ poly-Si and P^+ poly-Si work functions), and 2) asymmetric (ADG), in which the gates have different work functions (N^+ poly-Si for the front gate, P^+ poly-Si for the back gate, for an n-

channel device) [21]. At on-state, the two conductive channels (inversion layers) are formed for the SDG device but only one is formed for the ADG device unless the operation voltage is extremely high to form the other inversion layer near the P^+ gate. In addition, the SDG device shows higher carrier mobility due to its lower transverse electric field as compared to the ADG device.

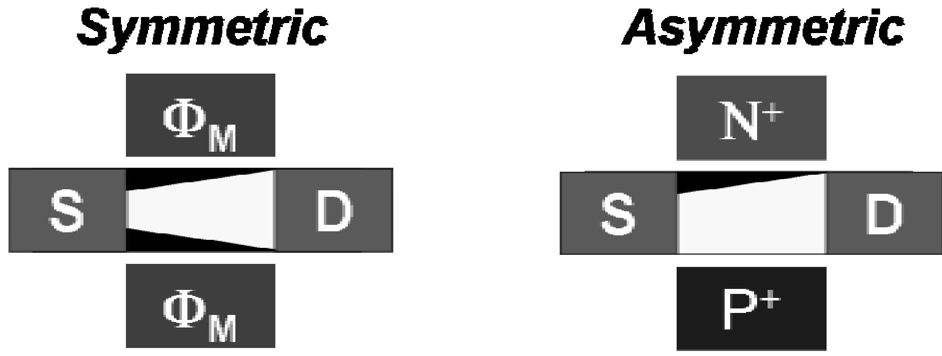
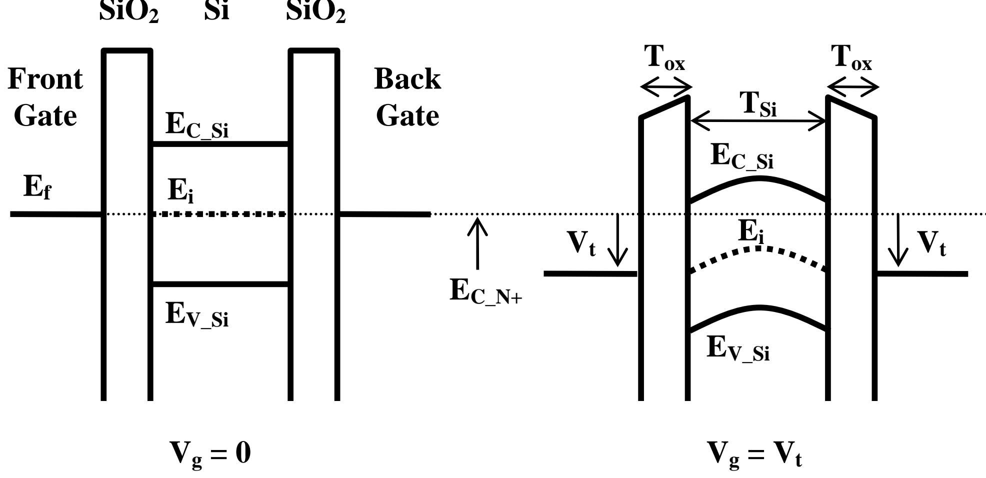


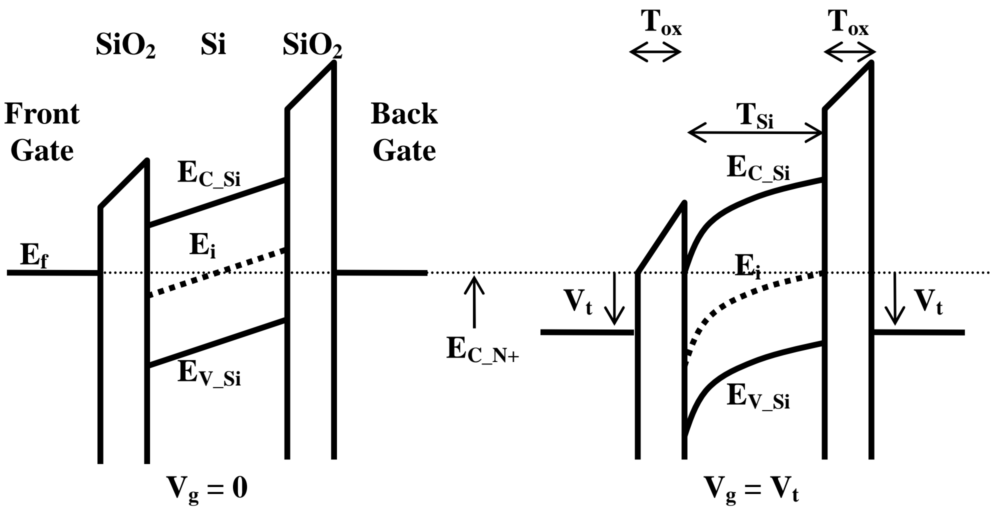
Figure 2.1: Symmetric and asymmetric double gate MOSFET structures.

The threshold voltage (V_t) of a SDG MOSFET must be adjusted by tuning the effective work function (Φ_M) of a metallic gate material, if light body doping is used to avoid dopant fluctuation effects (significant in the nanoscale regime). The range of required work functions for low power thin body CMOSFETs are 4.4-4.6 eV for PMOS and 4.8-5.0 eV for NMOS, respectively [22]. Without the metal gate technology with tunable or dual work functions, which will be introduced in chapter 3, the SDG device will not satisfy the V_t requirements. In contrast, the V_t of an ADG MOSFET can simply be adjusted by changing the body thickness T_{Si} and/or the gate-oxide thickness T_{ox}, without the need for exotic gate materials [23].

Fig. 2.2 shows the energy band diagram along the vertical direction (across the front and back gates) of the two structures shown in Fig. 2.1. It describes how conductive channels are formed for the undoped n-channel SDG and ADG MOSFETs, respectively.



(a) Symmetric DG MOSFET



(b) Asymmetric DG MOSFET

Figure 2.2: Schematic energy band diagrams for n-channel SDG and ADG MOSFETs.

(E_f: Fermi level, E_i: intrinsic Fermi level, E_{C_Si}: conduction band of the silicon body, E_{C_N+}: conduction band edge of the N^+ source/drain)

For the SDG device, the silicon bands are flat for the midgap gate work function at zero gate voltage. At $V_g=V_t$, the conduction band edge of the silicon body (E_{C_Si}) near the surface is bent and approaches the conduction band edge of the N^+ source/drain (E_{C_N+}). Since the work functions of two gates are identical, the conduction bands in both surfaces (under the front and back gates) are bent by the exactly same amount. As a result, at on-state, two conductive channels are formed for the SDG device, unless the silicon body thickness is not very thin (*e.g.,* <5nm). In that case, as the gate voltage approaches V_t, the bands of the whole silicon body including the center follow V_g, thus volume inversion takes place [24].

For the ADG device, the silicon bands have a nearly constant slope at zero gate voltage. Since this slope defines the transverse vertical electric field, the ADG device shows higher vertical electric field than the SDG device especially when the body thickness (T_{Si}) is small, resulting in mobility degradation. At $V_g=V_t$, further bend bending occurs at the silicon body surfaces, more at the left surface where the inversion charge layer is formed under N^+ front gate. In this case, the conduction band edge in the silicon body only near the left surface reaches the N+ source/drain conduction band edge, resulting in one conductive channel formation at on-state. However, if V_g is larger than 1V, two conductive channels will be formed even for the ADG device [21].

2.3 Performance sensitivity to process variations

The nominal DG MOSFET design with slightly larger effective gate length, defined as the distance between the positions where the source and drain dopant concentrations fall to $2\times10^{19}cm^{-3}$ (Fig. 2.3), was previously optimized for maximum on-state current [25]. For the SDG device, the gate work function is set to 4.414eV to achieve the same off-state leakage I_{off} as the ADG device. As can be seen from the I_d-V_g characteristics in Fig. 2.4, the SDG device achieves higher I_{on}, for a supply voltage of 0.9V. This is because it has two conductive channels and higher electron mobility due to lower transverse electric field as compared to the ADG device.

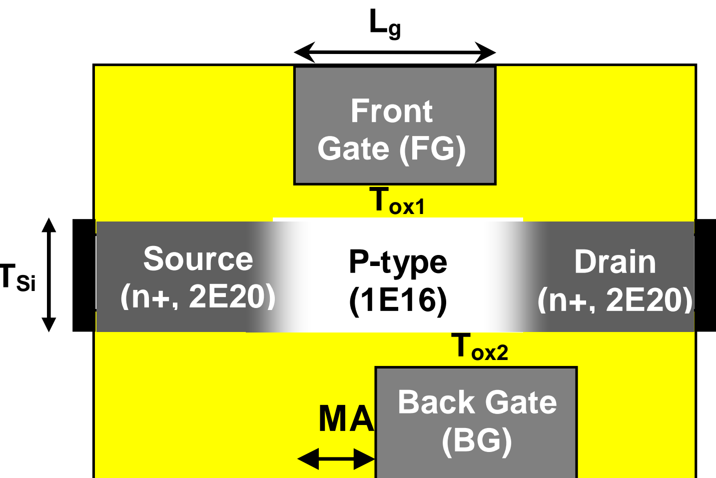


Figure 2.3: DG MOSFET structure used for simulations. Nominal parameter values: L_g = 13nm, $T_{ox1} = T_{ox2}$ = 1nm, T_{Si} = 5nm, V_{dd} = 0.9V, S/D gradient = 1.4nm/dec (optimal design for maximizing I_{on}) [25].

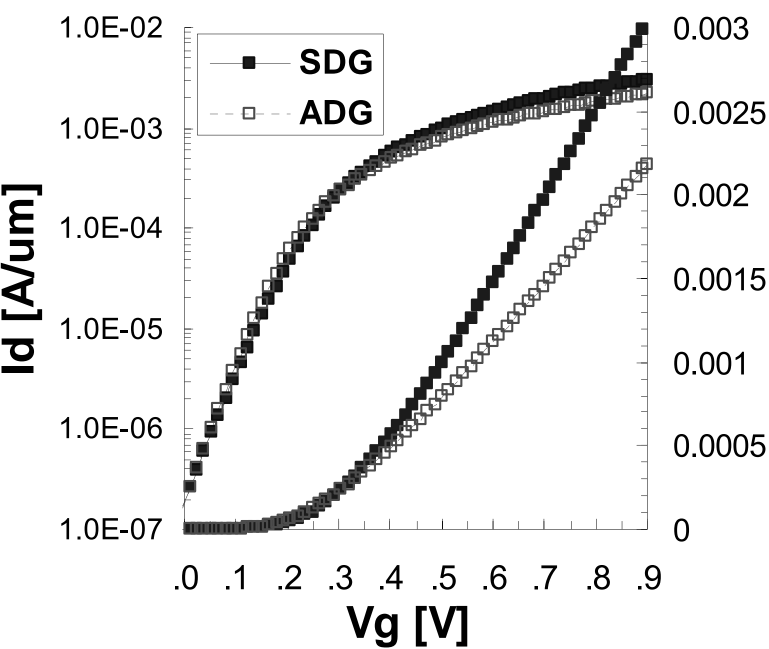


Figure 2.4: Nominal I_d-V_g curves (V_{ds}=0.9V) for SDG and ADG MOSFETs in both logarithmic and linear scales. The gate work function in the SDG device is 4.414eV to achieve the same I_{off} as the ADG device (n+ poly-Si front gate, p+ poly-Si back gate).

2.3.1 Impact of Parameter Variations

A thin body ($T_{Si} < L_g/2$) is necessary to effectively suppress SCE without body doping. I_{off} increases superlinearly with increasing T_{Si} (Fig. 2.5), more strongly so for the ADG device because its V_t is a sensitive function of T_{Si} (Fig. 2.6). I_{on} increases linearly with T_{Si} for both SDG and ADG devices due to reduced parasitic series resistance. The sub-threshold swing (SS) is steeper for the ADG device and is less sensitive to T_{Si} variation due to better suppression of drain-induced barrier lowering (DIBL) [23].

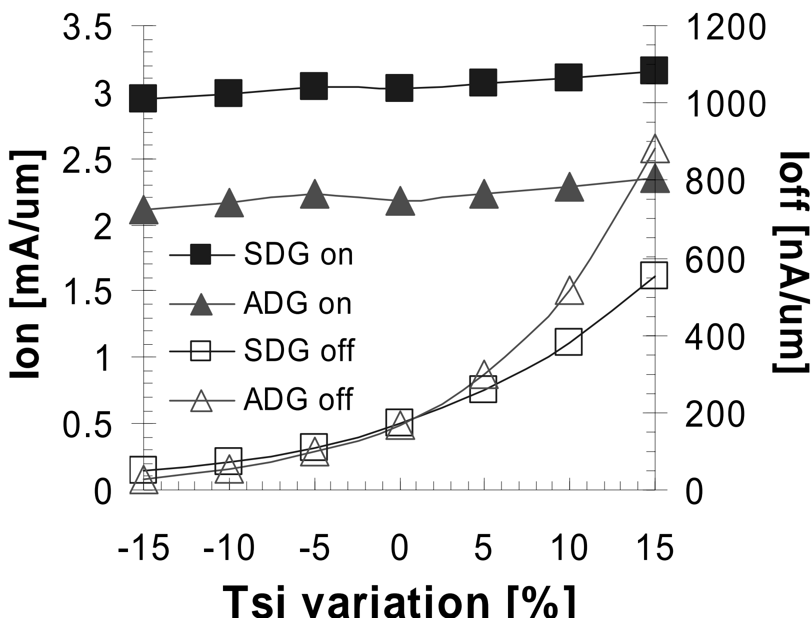


Figure 2.5: Impact of body thickness variation on drain current. (I_{on} = I_d for V_{gs}=V_{ds}=0.9V. I_{off} = I_d for V_{gs} = 0V and V_{ds} = 0.9V.) The ADG device shows larger I_{off} sensistivity as T_{Si} increases.

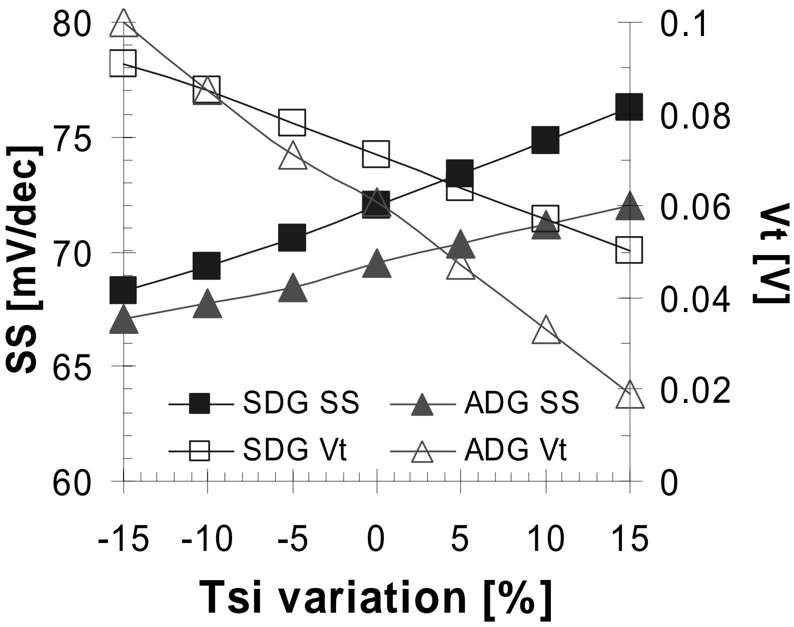


Figure 2.6: Impact of body thickness variation on SS and V_t. The ADG device shows larger V_t sensitivity, but slightly lower SS sensitivity.

Similarly, I_{off} increases superlinearly with decreasing L_g (Fig. 2.7), but comparably so for the SDG and ADG devices. I_{on} also increases ~linearly with decreasing L_g due to increased lateral electric field. The SDG and ADG V_t roll-off characteristics are similar, as shown in Fig. 2.8. Again, the ADG device shows better SS with less sensitivity to L_g due to better DIBL suppression.

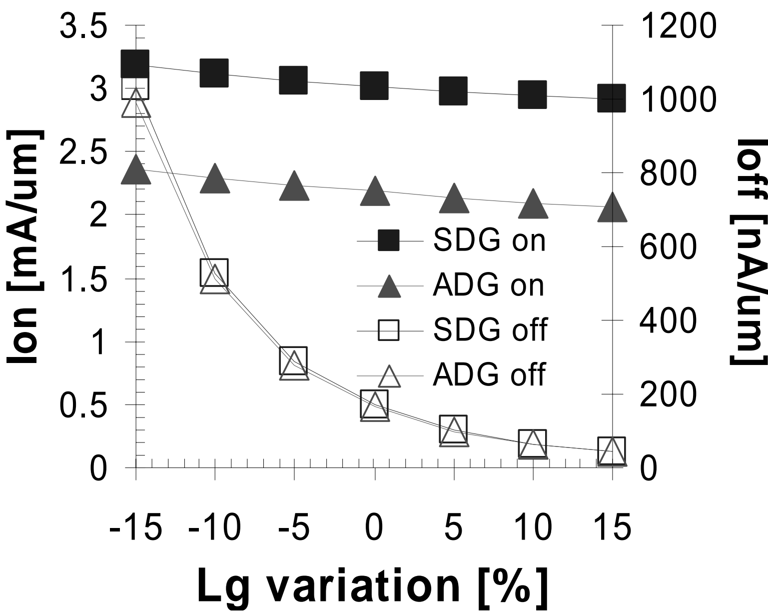


Figure 2.7: Impact of (front and back) gate length variation on drain current. Both SDG and SDG devices show large I_{off} sensitivity as L_g decreases.

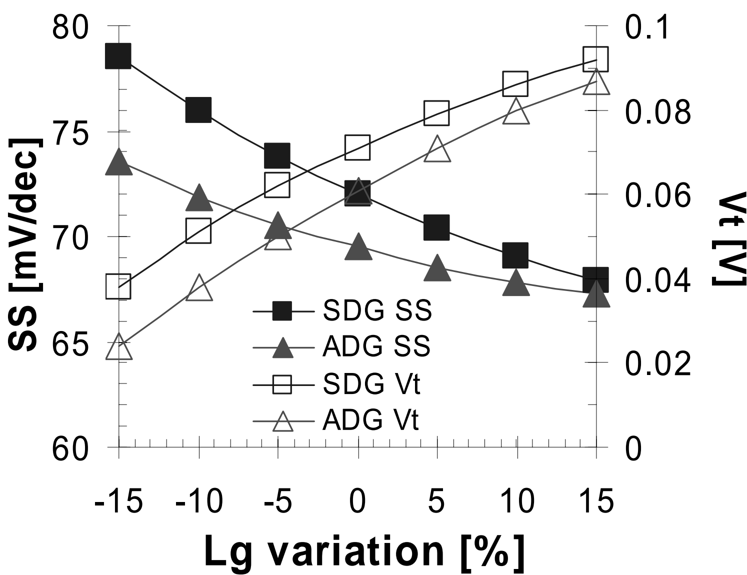


Figure 2.8: Impact of (front and back) gate length variation on SS and V_t. SDG and ADG devices show similar V_t roll-off and SS degradation as L_g decreases.

As shown in Fig. 2.9, I_{off} is less sensitive to percentage variations in T_{ox}, particularly for the ADG device, because SCE are effectively suppressed by using a thin T_{Si}. I_{on} is more sensitive to percentage variations in T_{ox} (*vs.* T_{Si} or L_g) for both the SDG and ADG devices because inversion-layer charge density is proportional to the gate capacitance. SS degrades slightly as T_{ox} increases due to reduced capacitive coupling between the gate and the channel, but less so for the ADG device due to its better DIBL suppression (Fig. 2.10). The V_t of the ADG device increases with T_{ox} because the equilibrium electron potential at the front channel is higher for thicker T_{ox} (*i.e.,* the fraction of the built-in vertical potential difference between the back and front gates, $\Phi_{(p+ poly-Si)} - \Phi_{(n+ poly-Si)}$, dropped across the front gate oxide increases with increasing T_{ox}). This is offset by worsening SCE (acting to lower V_t) with increasing T_{ox}, so that the sensitivity of V_t to T_{ox} variation is lower for the ADG vs. the SDG device.

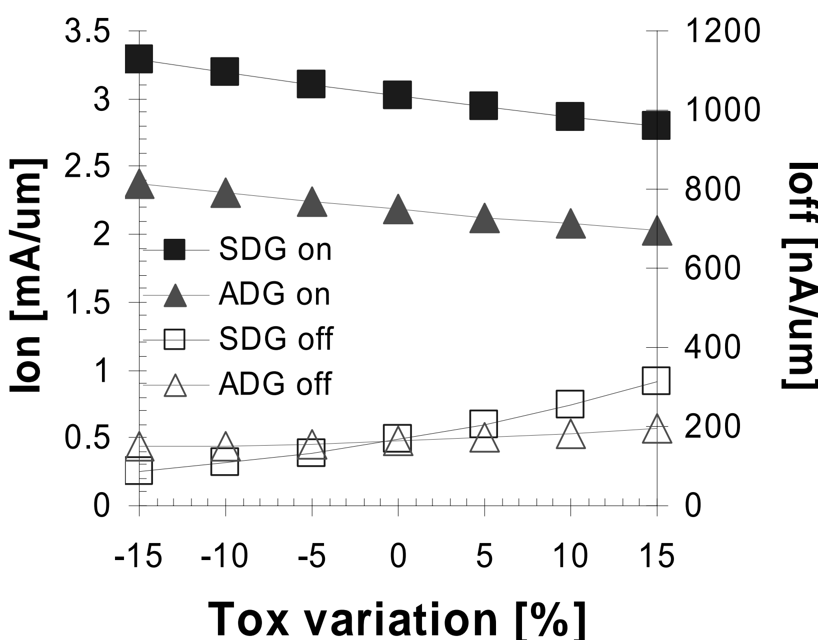


Figure 2.9: Impact of T_{ox} variation on drain current. The SDG device shows larger I_{off} sensitivity. I_{on} increases inversely with T_{ox} as expected for both SDG and ADG devices.

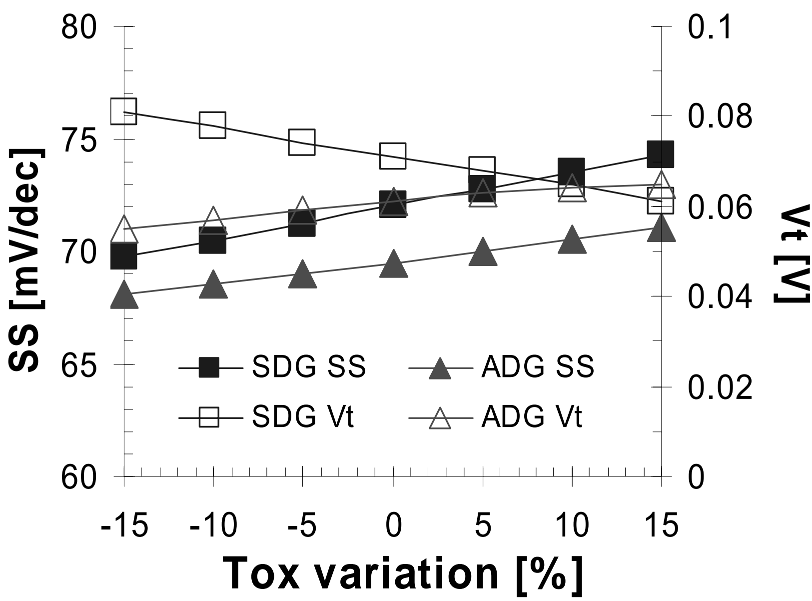


Figure 2.10: Impact of T_{ox} variation on SS and V_t. SS improves as T_{ox} decreases due to better SCE control. The SDG and ADG devices show opposite trends in V_t, with the ADG device showing less V_t sensitivity to T_{ox} variation.

2.3.2 Impact of back gate misalignment Variations

Capacitive coupling between the back-gate and channel decreases with increasing misalignment (MA) of the back gate. (MA < 0 if the misalignment is toward the source; MA > 0 if the misalignment is toward the drain.) Therefore, I_{off} increases with the magnitude of MA, particularly for MA > 50% (Fig. 2.11), and more so for the ADG device because it relies more heavily on the back gate to suppress leakage. I_{on} is more sensitive to MA for the SDG device because it results in a gate-underlapped source or drain at the back channel, which reduces the current drive there due to increased parasitic resistance; whereas it results in slightly improved I_{on} for the ADG device due to the reduced influence of the back gate on V_t, to keep it high. Reduced coupling between the back-gate and channel results in poorer control of SCE and hence degraded V_t and SS in both ADG and SDG devices (Fig. 2.12).

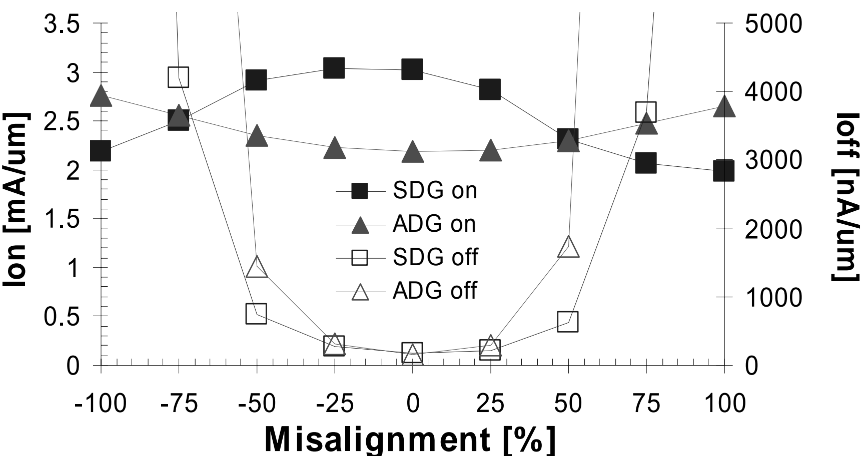


Figure 2.11: Impact of BG misalignment on drain current. The SDG device shows I_{on} degradation with increasing MA due to significantly increased parasitic resistance for the back channel. The ADG device shows higher I_{on} with increasing MA due to reduced V_t. I_{off} is very sensitive for |MA| > 25%, more for the ADG device than for the SDG device.

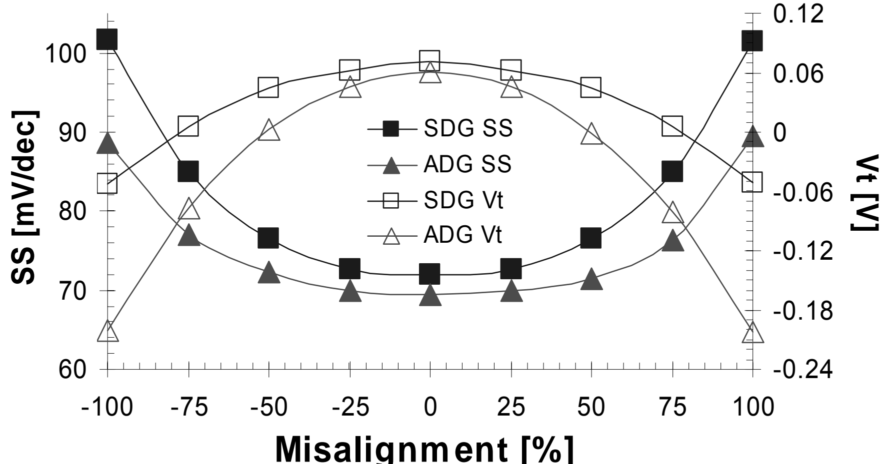


Figure 2.10: Impact of BG misalignment on SS and V_t. Both SDG and ADG devices show degraded SCE with increasing misalignment, due to reduced back-gate control.

2.4 Conclusion

Advanced ultrathin body (UTB) DG device structures are necessary for sub-15nm L_g MOSFETs. Two DG structures (SDG and ADG) are introduced and their operation schemes are compared by using schematic energy band diagrams.

We have also investigated the effect of process induced parameter variations (as large as ±15%) in T_{Si}, L_g, T_{ox}, and back-gate misalignment (as large as ±100%) on the performance of n-channel SDG and ADG MOSFETs with nominal gate length = 13nm and light body doping, via device simulation (ISE DESSIS). If the limits for variations in I_{on} and I_{off} are ±5% and +300nA/μm, respectively, the tolerable ranges of variation are:

- for T_{Si}: -15% to 5% for both SDG and ADG
- for L_g: -5% to 15% for SDG, -5% to 10% for ADG
- for T_{ox}: -5% to 5% for SDG, -5% to 10% for ADG

- for MA: ±25% for both SDG and ADG

Considering the capability of the modern device process technology, it is expected that both the SDG and ADG designs are reasonably tolerant of process-induced variations.

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Chapter 3 : Mo Gate Technology

3.1 Introduction

Metal gate technology can facilitate MOSFET scaling because it eliminates the issues of poly-Si gate technology, namely the gate depletion effect and boron penetration. Advanced transistor structures such as the ultra-thin-body (UTB) MOSFET and the double-gate (DG) MOSFET are more scalable than the classic bulk-Si MOSFET because of their superior control of short channel effects [1]; hence they may be adopted for CMOS technology nodes toward the end of the roadmap [2]. In order to achieve high carrier mobilities and to minimize threshold-voltage (V_T) variations, the channel/body should be lightly doped ($< 10^{17}$ cm^{-3}) or undoped. In this case, a metal gate technology that offers tunable work function (Φ_M) for V_T adjustment is very desirable. The ranges of Φ_M required to fully adjust the V_T values of thin-body (fully depleted) MOSFETs for various applications is 4.4V to 4.6V for n-channel devices and 4.8eV to 5.0eV for p-channel devices [3]. Recently, A. Carlson *et al*. reported that a single metal gate technology with ~4.6eV work function should be advantageous for achieving large read and write margins in six-transistor (6-T) FinFET SRAM cells [4]. V. Varadarajan *et al*. showed that a single gate technology with near-midgap work function (~4.7eV) can be suitable for low-power DG CMOS technology, if fine-tuning of V_T is achieved by

engineering the electrical channel length (L_{eff}) [5]. Thus, the ability to tune Φ_M near mid-gap should be useful for various applications.

P. Ranade *et al*. demonstrated that the work function of a molybdenum (Mo) gate electrode can be tuned over a wide range (4.5eV to 5.0eV) by nitrogen ion (N^+) implantation inducing structural and/or chemical changes in the Mo near at the gate dielectric interface [6]. Damage to the gate dielectric is a potential issue for this approach, however. Furthermore, high-tilt ion implantation would be needed to dope the gate electrodes of vertical transistor structures such as the FinFET [7], which limits device packing density (to avoid shadowing effects). To avoid these issues, nitridation of Mo by high-temperature forming gas annealing (HTFGA) [8] is an attractive alternative approach.

In this chapter, Mo gate work function reduction by N^+ implantation is reviewed and issues of for this approach are addressed. As an alternative approach to reduce Mo gate work function, the impact of HTFGA on Mo gate work function is investigated and CMOS process integration issues are discussed [9]. Finally, a theory for Mo gate work function reduction is presented.

3.2 Φ_M reduction by N implantation

Molybdenum (Mo) is an attractive candidate for tunable-Φ_M metal gate technology due to its strongly anisotropic work function [10], which is believed to arise from differences in interatomic spacing and atomic plane smoothness with crystal orientation [11]. In addition, it has excellent compatibility with Si CMOS processing

because of its high melting point (~2610°C), and low resistivity (~5μΩ-cm). A significantly lower Φ_M (~4.0eV) of Mo was observed for Mo gate electrodes with structural damage induced by Ar ion implantation, indicating that amorphous Mo has a very low work function [6]. However, upon thermal annealing the Mo recrystallizes, increasing Φ_M to ~5.0eV.

On the other hand, Φ_M reduction by N^+ implantation becomes more significant as thermal annealing temperature increases, as shown in Fig. 3.1 [6], suggesting that the Φ_M reduction is induced by chemical modification of the Mo film (*i.e.,* nitridation). The Φ_M increase of un-implanted Mo with increasing annealing temperature can be explained by the recrystallization and/or grain growth effect.

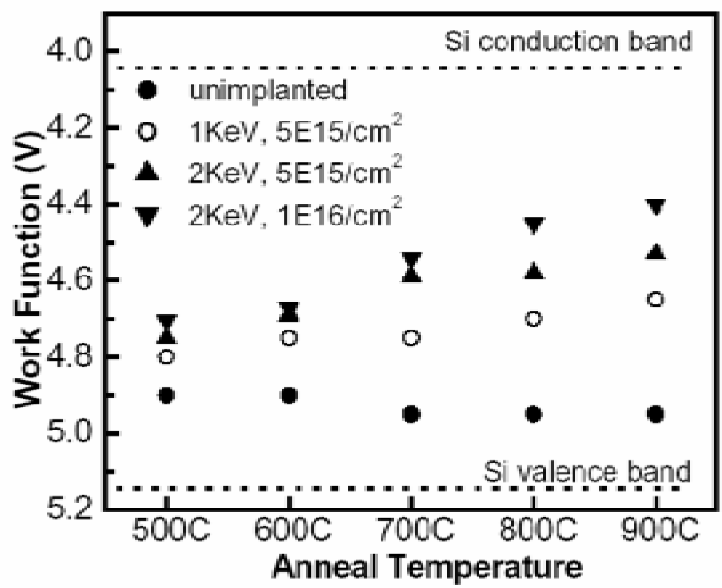


Figure 3.1: Variation of Mo (15nm) work function with thermal annealing. All anneals were 15 min long except for the 900°C anneal (15s) [6].

Fig. 3.1 also shows that higher N^+ implantation energy and dose are necessary for larger reduction of Mo work function. The implantation energy and dose determine the distribution profile of implanted ions into Mo. As long as the dose is higher than $10^{12}cm^{-2}$, the distribution can be described statistically and is often modeled to first order by a symmetric Gaussian distribution given by [12]

$$C(x) = C_p \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2} \right]$$

where R_p is the average projected range normal to the surface, ΔR_p is the straggle about that range, and C_p is the peak concentration given by

$$C_p = \frac{Q}{\sqrt{2\pi}\Delta R_p}$$

where Q is the implantation dose. Therefore, the distribution can be obtained if the implantation energy and dose are known. For example, Fig. 3.2 shows the plot of implanted N^+ into Mo with the energy of 15keV and the dose of $5\times10^{15}cm^{-2}$.

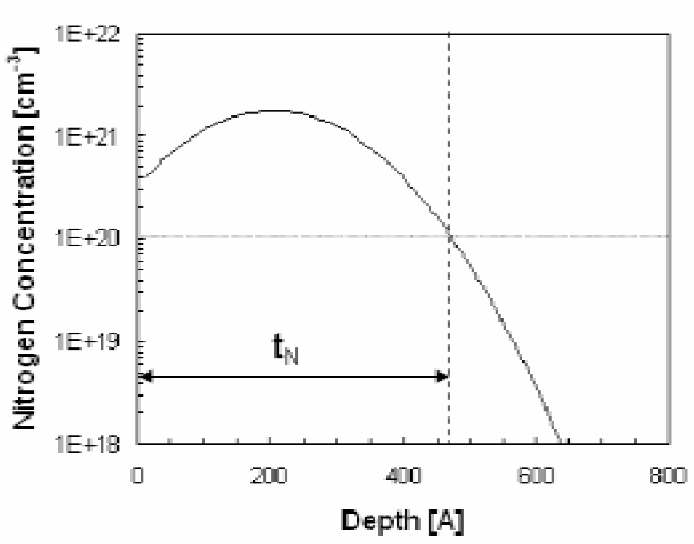


Figure 3.2: Distribution of N^+ implanted into Mo with the energy of 15keV and the dose of $5\times10^{15}cm^{-2}$.

For a fixed Mo film thickness (t_{Mo}), the relative implantation depth of N^+ is defined by subtracting the implantation depth (t_N), where nitrogen concentration is $10^{20}cm^{-3}$, from t_{Mo}. This relative depth is uniquely determined by the energy and dose of implanted N^+ together with t_{Mo}. For a given Mo film thickness, the relative depth decreases and becomes negative as the implantation energy and dose increase. (Negative t_{Mo}- t_N indicates that a significant fraction of the implanted nitrogen profile is located below the Mo film.)

From the experimental data reported previously [6, 13, 14], the relationship between the Φ_M of Mo and the relative implantation depth is plotted in Fig. 3.3. It is found that smaller (or even negative) relative implantation depth is required for more Φ_M reduction of Mo, indicating the damage to the gate dielectric is a potential issue for this approach. Actually, abnormal C-V curves were obtained for Mo gated capacitors with

high N^+ implantation energies [13]. Increased gate leakage current was also reported for the Mo gate capacitors with high N^+ implantation energy and dose [15].

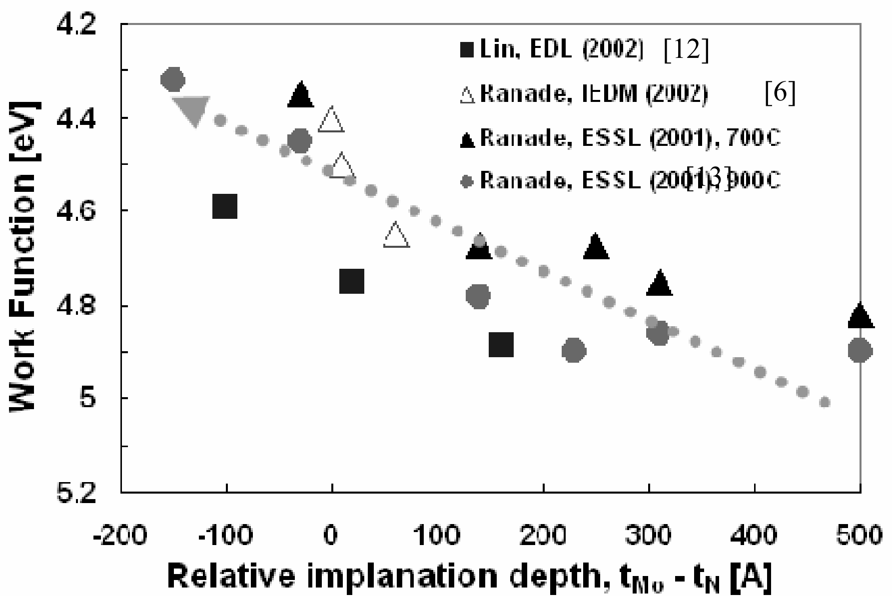


Figure 3.3: Experimentally observed work functions of Mo with different N^+ implantation conditions plotted as a function of relative implantation depth.

Metal gate technology is expected to be adopted for advanced transistor structures such as the FinFET [7]. However, high-tilt ion implantation would be needed to dope the gate electrodes of such a vertical transistor structure, which limits device packing density (to avoid shadowing effects). As an alternate approach to reduce Mo gate work function, without the aforementioned issues, the impact of HTFGA on Mo gate work function is investigated and CMOS process integration issues are discussed in the following section.

3.3 Φ_M reduction by FGA

In order to investigate the impact of high-temperature forming gas annealing (HTFGA) on the Mo gate work function reduction, Mo-gate capacitors were fabricated on lightly doped p-type silicon wafer substrates. Thermally grown SiO_2 was used as the gate dielectric. In order to account for the influence of oxide fixed charge, multiple SiO_2 thicknesses were obtained on a single wafer by the selective etchback method [6]. The Mo gate film (50nm thick) was sputter deposited with a PCT (Plasma Charge Trap) to minimize gate oxide damage [16]. Some samples received a post-deposition anneal for 1m at 900°C in N_2. Large-area capacitor electrodes (100μm×100μm) were then defined using i-line photolithography followed by highly selective dry etching of Mo over the gate oxide [17]. Polymer residue generated during the dry etching process was removed in EKC4000. To prevent the oxidation of Mo, the photoresist was stripped in PRS3000 solution at 80°C for 10 minutes followed by a de-ionized water rinse. Flat-band voltages (V_{FB}) were determined from capacitance *vs.* voltage (C-V) measurements, and Φ_M values were extracted from plots of V_{FB} *vs.* gate oxide thickness [18]. The capacitors were then subjected to various 15-minute anneals in forming gas (10% H_2 / 90% N_2) or N_2, and Φ_M was tracked.

Fig. 3.4 shows the work functions of Mo gate electrodes after various annealing treatments. Consistent with a previous report, annealed Mo starts out with a higher work function than unannealed Mo, due to a more columnar grain structure with (110) planes parallel to the substrate [18]. Regardless of the initial Φ_M value, the Mo gate work function converges to ~4.7eV after a 700°C HTFGA. This can be attributed to a

chemical change in the Mo film, induced by the HTFGA treatment. Indeed, it was previously reported that H_2 helps N_2 to react with Mo to form Mo_2N during HTFGA at temperatures greater than 600°C [8]. After the HTFGA treatment, the oxide fixed charge density (Q_f, extracted from the slope of the V_{FB} vs. oxide thickness plot) is lowered by one order of magnitude, and low resistivity (in the range from 10 to 20 μΩ-cm) is maintained.

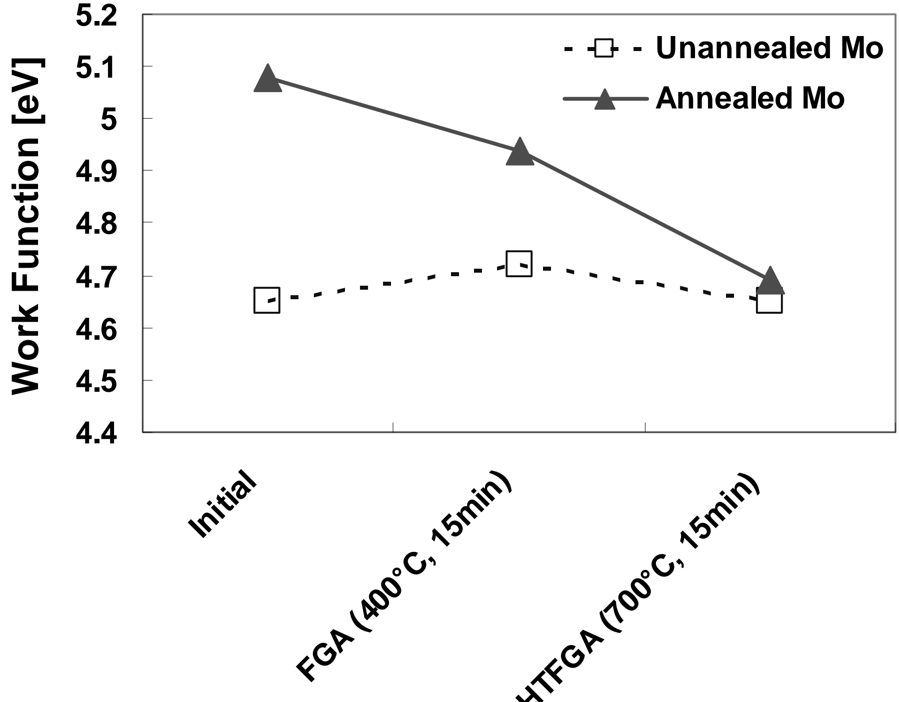


Figure 3.4: Work functions of Mo gate electrodes after various 15-minute annealing treatments. Annealed (1m at 900°C in N_2) Mo shows a higher initial work function than unannealed Mo, indicating that further crystallization of Mo increases its work function [18]. After a 700°C HTFGA, the Mo work function converges to ~4.7eV regardless of the initial value.

Fig. 3.5 shows that Φ_M decreases with HTFGA temperature (T_{anneal}) and saturates at a minimum value of 4.6eV for T_{anneal} > 800°C. However, the reduction in Φ_M is not retained with subsequent thermal annealing at 800°C in N_2 (ref. the filled triangle in Fig. 3.5), indicating that the incorporated nitrogen can easily out-diffuse. In order to prevent out-diffusion, a TiN capping layer can be used, so that low Φ_M is maintained with additional thermal annealing (ref. the filled square in Fig. 3.5). It has been reported that a nitrogen-rich TiN capping layer can serve as a source of nitrogen to reduce the Mo work function during a high-temperature anneal in N_2 [19]. In this work, a stoichiometric TiN film was used, so that a relatively small reduction in Φ_M with thermal annealing in N_2 is seen for TiN-capped Mo (ref. the open square *vs*. the filled triangle in Fig. 3.5). Therefore, we deduce that the TiN capping layer serves as an effective barrier to nitrogen out-diffusion (rather than a source of nitrogen) for a nitrided Mo film.

Figure 3.6 shows how the V_{FB} *vs*. gate oxide thickness characteristic (which is used to determine Φ_M and Q_f) changes after various 15-minute anneals, for capacitors with annealed Mo gate electrodes. The measured C-V curves for 25nm oxide thickness are shown in the inset for reference. A HTFGA treatment reduces Φ_M and Q_f (ref. filled circles *vs*. open triangles in Fig. 3.6). Subsequent high-temperature (800°C) annealing in N_2 causes nitrogen out-diffusion so that the HTFGA-induced reduction in Φ_M is lost and Q_f is increased (ref. filled triangles in Fig. 3.6). A TiN capping layer is effective for blocking nitrogen out-diffusion during the high-temperature anneal in N_2, so that low Φ_M and Q_f are retained (ref. filled squares in Fig. 3.6).

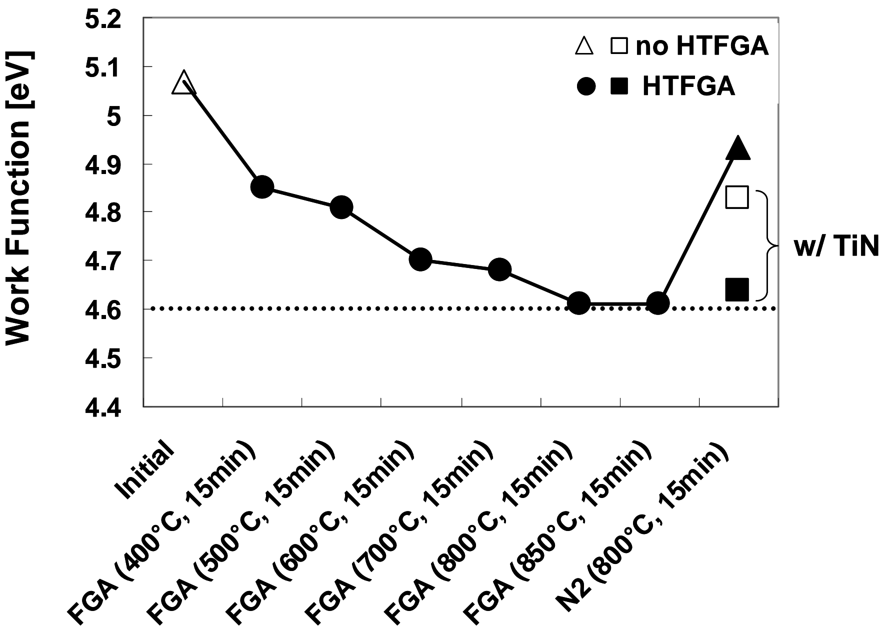


Figure 3.5: Evolution of Mo gate work function with sequential annealing. Φ_M decreases with increasing forming gas annealing temperature (T_{anneal}), and saturates at 4.6eV for T_{anneal} > 800°C. Unless a TiN capping layer is applied, the reduction in Φ_M is not retained with additional high-temperature annealing in N_2. Considering that a much smaller reduction in Φ_M is induced by the TiN capping layer itself (ref. the open square), these results indicate that TiN is an effective barrier to nitrogen out-diffusion.

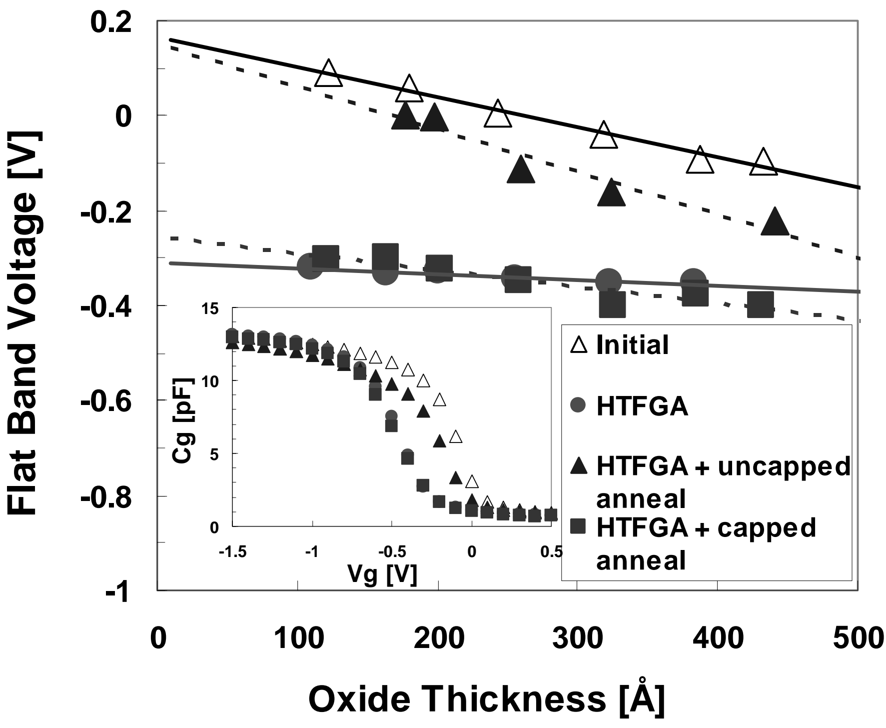


Figure 3.6: Flat band voltage *vs*. oxide thickness for capacitors with annealed Mo gate electrodes. The measured C-V curves for 25nm oxide thickness are shown in the inset for reference. A 15-minute, 800°C HTFGA reduces the Mo work function and lowers the fixed charge density (Q_f). N_2 annealing (15m at 800°C) after HTFGA causes the Φ_M reduction to be lost and results in worse Q_f. However, the Φ_M reduction and low Q_f are retained with a TiN capping layer.

Figure 3.7 shows how dual work function Mo gate electrodes may be achieved in an integrated CMOS process flow. In this flow, a HTFGA step is used to globally reduce the Mo gate work function; afterwards, the n-channel devices are selectively capped with TiN so that the low gate work function (4.6eV) is retained through the remainder of the device fabrication process. Since the p-channel devices are not capped,

the Mo gate work function will return to a high value (~5.0eV) as nitrogen out-diffuses during the various thermal process steps (*e.g.,* the source/drain dopant activation anneal). The ability to etch TiN with high selectivity to Mo is crucial for implementing this process flow. Fortunately, a standard Cl_2+O_2 dry etch process shows very high (>100:1) TiN etch selectivity to Mo.

- **Well Doping**
- **Gate stack deposition (Moly/Gox)**
- **HTFGA (H_2/N_2, 800°C, 15min)**
- **TiN sputtering**
- **Selective TiN etching for PMOS region**
- **Channel doping**
- **Gate patterning**
- **Slim spacer formation**
- **S/D extension IIP**
- **Spacer formation**
- **S/D IIP**
- **S/D Activation annealing**

Figure 3.7: Proposed CMOS process flow to achieve dual Mo gate work functions.

Therefore, high temperature forming gas annealing is an effective technique for tuning the gate work function of Mo. Φ_M decreases with increasing T_{anneal} and saturates at 4.6eV for T_{anneal} > 800°C. The reduction in Φ_M is not retained with subsequent thermal annealing (*e.g.* 15m at 800°C in N_2) due to nitrogen out-diffusion, however. In order to prevent out-diffusion, a TiN capping layer can be used, so that low Φ_M is

maintained with additional thermal annealing. By selectively using a TiN capping layer in the n-channel device regions, the HTFGA technique can be applied to achieve dual work function Mo gate electrodes suitable for advanced CMOS technologies employing thin-body MOSFETs.

3.4 Theory for Φ_M reduction

Structural and chemical modifications have been considered as major mechanisms for changing the work function of Mo by N^+ implantation and/or thermal annealing [20]. In general, densely packed crystallographic surfaces yield high work functions since these surfaces are smooth and relatively inert with few broken atomic bonds. On the other hand, open crystallographic surfaces yield low work functions due to a greater number of broken bonds. In the case of Mo, the densest plane is the (110) plane [21], and Mo films deposited by sputtering show a substantial fraction of grains with this orientation. Thus, the Φ_M of an as-deposited Mo film is normally high, increasing slightly with additional thermal annealing and becoming stable around at 5eV. This high Φ_M can be reduced by structural modification of the Mo film, such as amorphization by Ar^+ implantation. However, the Mo film is easily recrystallized and shows higher Φ_M again with subsequent thermal annealing, as indicated from the increased intensity of the (110) measured by X-ray diffraction (XRD) patterns.

N^+ implantation is also expected to amorphize the Mo film and is known to reduce Φ_M. In contrast, the reduced work function by N^+ implantation is retained or even reduced further as annealing temperature (T_{anneal}) increases, indicating that chemical

modification occurs. The metal work function in vacuum ($\Phi_{M, VAC}$), defined by the minimum energy required to remove an electron from the metal surface at 0K [22], is commonly assumed to be the same as the effective work function ($\Phi_{M, EFF}$), determined by the energy band alignment between the metal gate and gate dielectric. However, since $\Phi_{M, EFF}$ is found by plotting flat band voltage (V_{FB}) as a function of oxide thickness (T_{ox}) derived from C-V measurements, it additionally reflects the presence of dipole layers in the insulator layer of the MOS structure [23]. A centroid of charge at a fixed distance from the metal-insulator interface also affects $\Phi_{M, EFF}$ [24]. Nitrogen segregation to the Mo-SiO_2 interface is believed to result in a dipole moment and hence reduction in the $\Phi_{M, EFF}$ of Mo. Actually, nitrogen segregation th the Mo-SiO_2 interface was observed from secondary-ion mass spectroscopy (SIMS) analysis of an annealed N^+ implanted Mo sample [14].

In order to clarify the mechanism of Mo Φ_M reduction, the physical microstructure and chemical composition were investigated using high-resolution transmission electron microscopy (HR-TEM, Courtesy of Dr. Xiaoyu Xu and Prof. Eicke Weber). Fig. 3.8 shows the effect of T_{anneal} on Φ_M and average grain size of un-implanted Mo. N_2 annealing was performed for 15 minutes at 500°C, 600°C, or 700°C. All samples show similarly high Φ_M (~5.1eV) even though the average grain size becomes larger as T_{anneal} increases, while showing the same columnar grain structures (*i.e.,* (110) texture), indicating Φ_M is independent of the grain size. The crystalline quality, especially near to the Mo-SiO_2 interface, is also good for all the samples as shown in Fig. 3.9.

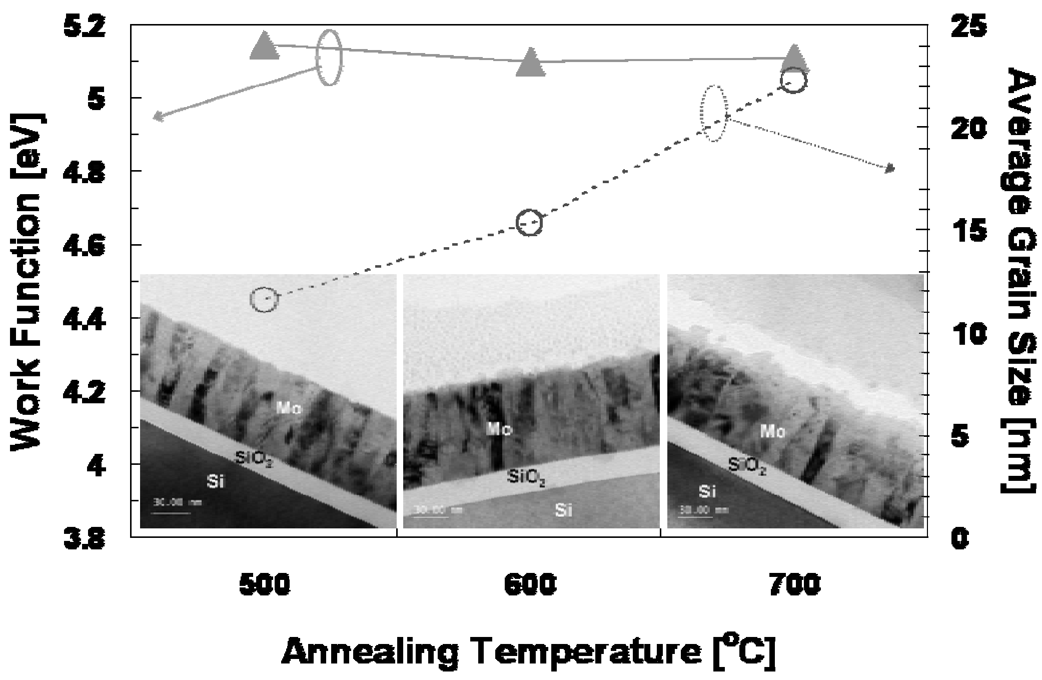
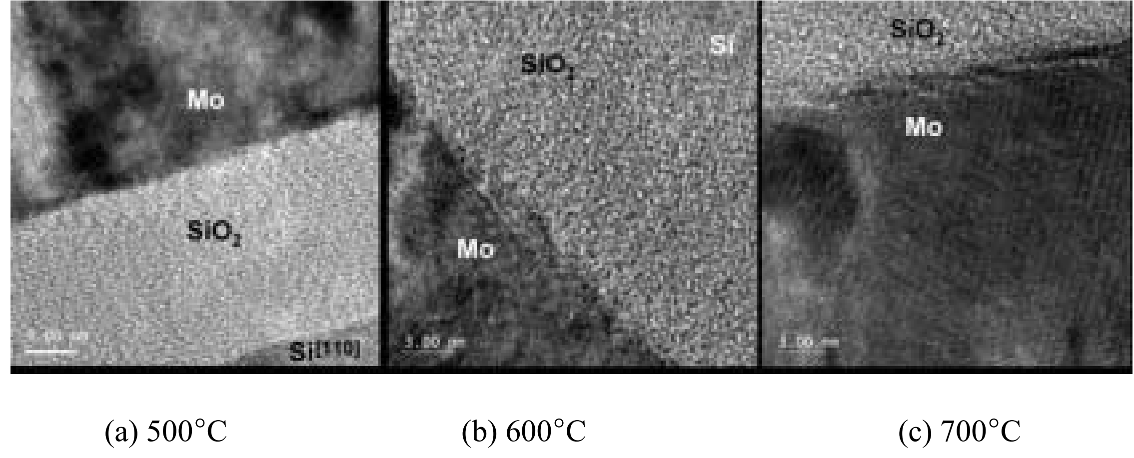


Figure 3.8: Annealing temperature effect on Φ_M and grain size of un-implanted Mo.



(a) 500°C (b) 600°C (c) 700°C

Figure 3.9: HR-TEM pictures showing crystalline quality near Mo-SiO_2 interface for un-implanted Mo.

Fig. 3.10 shows the effect of T_{anneal} on Φ_M and grain size, for Mo implanted with N^+ with $10^{16}cm^{-2}$ dose and 40keV energy. N_2 annealing was performed for 15 minutes at 600°C or 700°C. Again, HR-TEM pictures show columnar grain structures induced by thermal annealing; high Φ_M of Mo is anticipated. However, only the Mo sample annealed at 700°C shows high Φ_M (~4.9eV), while the Mo sample annealed at 600°C still shows reduced Φ_M (~4.3eV). Similar data has been reported in [14], showing that the Φ_M reduction by N^+ implantation is restored (becomes high again) as T_{anneal} increases. In that case, even more nitrogen segregation at the Mo-SiO_2 interface was observed by SIMS, excluding the possibility of N_2 out-diffusion. Instead, it was found that the intensity of the (110) diffraction peak further increased at higher T_{anneal}, indicating an improvement of crystalline quality of the film is a dominant effect for Φ_M change as compared to chemical modification effects. In addition, the average grain size of N^+ implanted Mo film is larger than that of un-implanted one with the same T_{anneal}. This can be explained by defect-assisted grain growth induced by ion implantation.

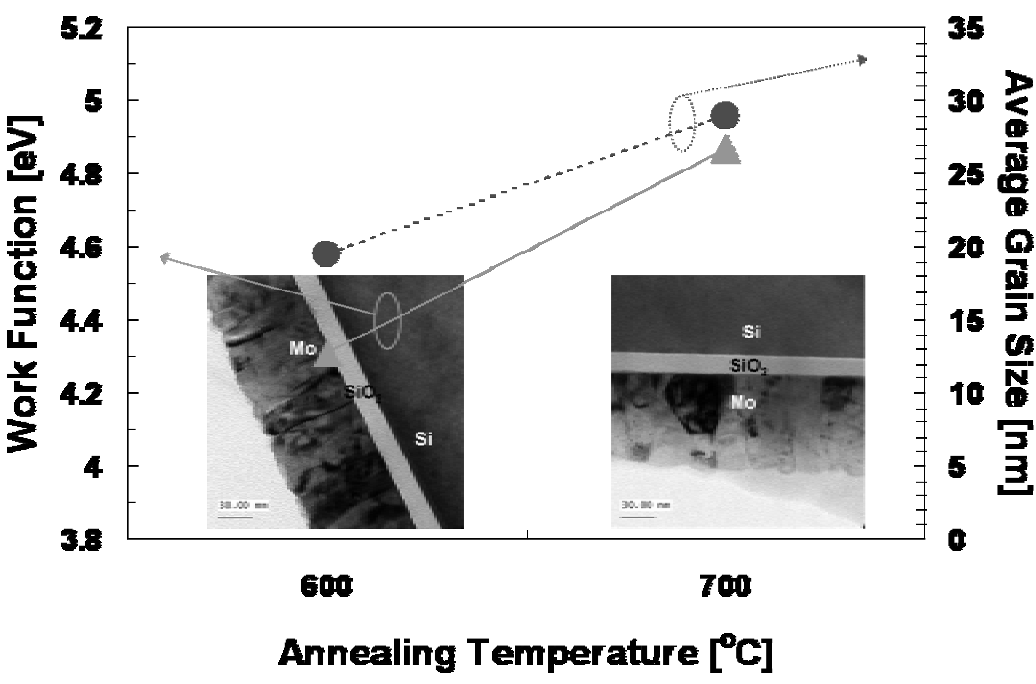
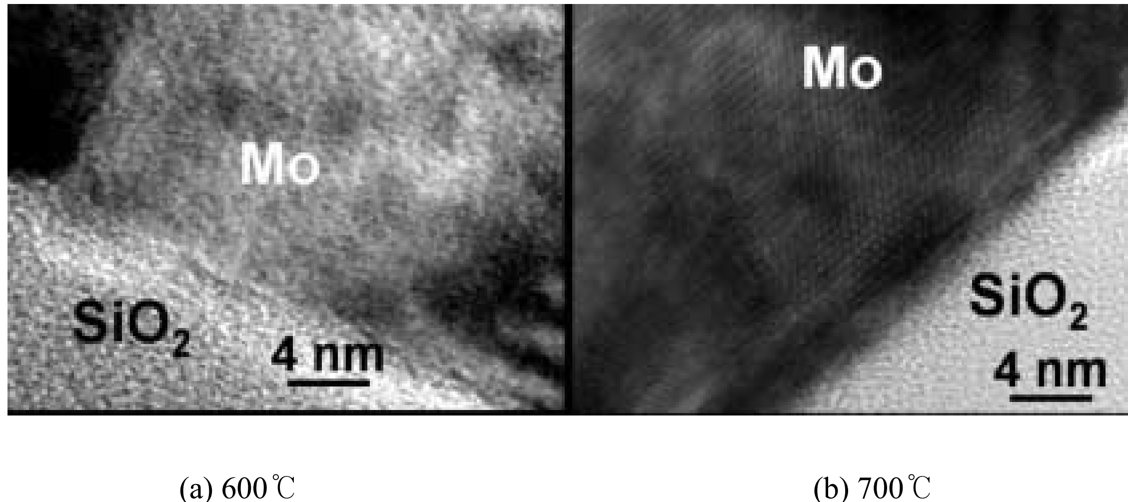


Figure 3.10: Annealing temperature effect on Φ_M and grain size of N^+ implanted Mo.

HR-TEM pictures in Fig. 3.11 consistently confirm that the crystalline quality of N^+ implanted Mo with higher T_{anneal} is better than that with lower T_{anneal}. However, these results are contradictory with those shown in Fig. 3.1, which show that Φ_M reduction induced by N^+ implantation further grows as T_{anneal} increases, indicating the importance of chemical modification (nitrogen segregation) for Φ_M reduction. Coincidentally, the low Φ_M was restored back to high Φ_M for thick Mo films (90nm, 150nm) but retained for thin Mo film (15nm). Therefore, it is clear that Φ_M of N^+ implanted Mo is determined by the combination of structural and/or chemical modification effects, but it seems that structural modification effects might become dominant as T_{anneal} increases unless the Mo film is very thin. Actually, thick Mo film has relatively small amount of nitrogen

concentration as compared to thin Mo film; it might be hard to maintain the minimum concentration of nitrogen near the interface required for reducing Φ_M by chemical modification.



(a) 600℃ (b) 700℃

Figure 3.11: HR-TEM pictures showing crystalline quality near to the Mo-SiO_2 interface for implanted Mo.

Finally, the possible mechanism for Φ_M reduction by HTFGA is also investigated using HR-TEM analysis. HTFGA is known to nitride the whole Mo film by a two step reaction: 1) reduction of molybdenum oxide (H_2 in the forming gas reacts with oxygen in molybdenum oxide and forms volatile H_2O gas), and 2) direct nitridation of Mo [8]. Therefore, chemical modification induced by HTFGA is expected to reduce Φ_M of Mo. In fact, reduced Φ_M (~4.7eV) of Mo by HTFGA (700°C, 15m) was observed as shown in Fig. 3.12. Almost identical C-V characteristics were observed between thin (15nm) and thick (90nm) Mo films, implying no differences in nitrogen concentrations near the Mo-SiO_2 interface achieved by nitridation of the whole Mo films. It is worthwhile to note that

process-induced Φ_M variation, *e.g.,* non-uniform Mo film thickness and implantation depth-profile, will become an issue for Mo Φ_M tuning technology with the N^+ implantation approach because the Φ_M is mainly dependent on the amount of nitrogen concentration (ref. Fig. 3.3) near to the Mo-SiO_2 interface, which varies accordingly.

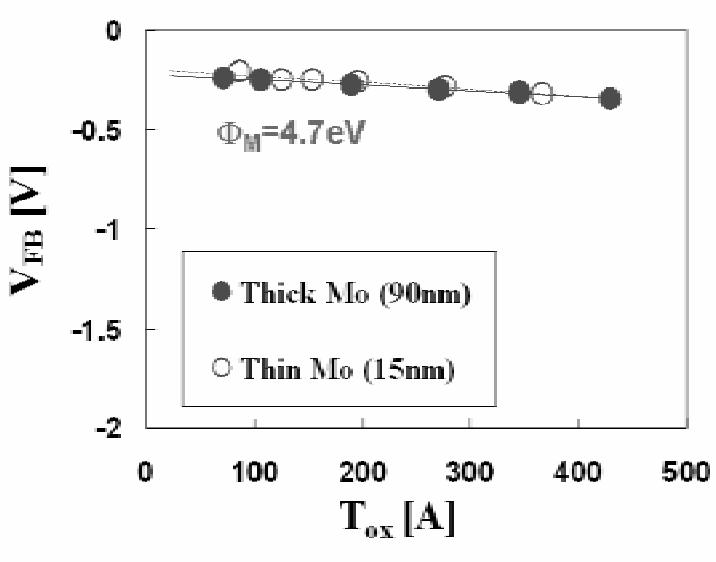


Figure 3.12: Flat band voltage *vs*. oxide thickness for capacitors with forming gas annealed Mo at 700°C for 15 minutes.

Fig. 3.13 shows a HR-TEM picture of 15nm-thick Mo film after HTFGA (700°C, 15m). As compared against the N^+ implanted samples, it shows better crystalline quality, almost as comparable to that of the un-implanted Mo samples. Therefore, chemical modification is believed to be the dominant effect for Φ_M reduction of Mo induced by HTFGA. In fact, Mo_3N_2 formation in Mo layer is confirmed by comparison of diffraction pattern with a simulated model by Crystalkit™.

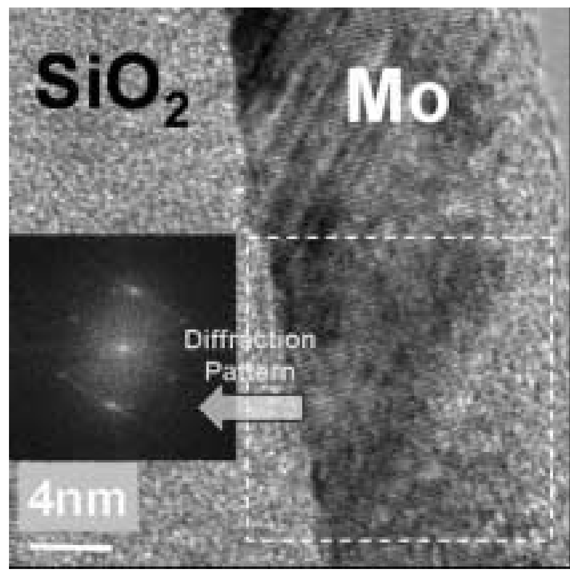


Figure 3.13: HR-TEM picture showing crystalline quality near Mo-SiO_2 interface for forming gas annealed Mo (700°C, 15m). Diffraction patterns confirm Mo_3N_2 formation in the Mo layer by comparison with a simulated model by Crystalkit^{TM}.

In conclusion, for un-implanted Mo film, Φ_M is mainly affected by the structural modification in the film. HRTEM showed columnar structures, *i.e.,* (110) texture, and better crystalline quality near at Mo-SiO_2 interface, explaining the increased Φ_M for the un-implanted Mo film with subsequent thermal annealing. Chemical modification (nitrogen segregation) to the Mo-SiO_2 interface is considered as a major effect for Φ_M reduction of N^+ implanted Mo film until Φ_M increases again with subsequent thermal annealing (especially for thick Mo film > 50nm) due to improved crystalline quality of the Mo film near to the Mo-SiO_2 interface. HTFGA can more effectively reduce and retain Φ_M dominantly by chemical modification, *i.e.,* nitridation of the whole Mo film, with relatively improved crystalline quality compared to N^+ implanted Mo.

3.5 Conclusion

In this chapter, Mo gate work function reduction by N^+ implantation is reviewed and the issues of this approach, such as damage to the gate dielectric and requirement for high-tilt ion implantation for FinFET gate electrodes, are addressed. It is found that smaller (or even negative) relative implantation depth is required for more Φ_M reduction of Mo, indicating the damage to the gate dielectric is a potential issue for this approach. HTFGA is introduced as an alternative technique for reducing the gate work function of Mo. Φ_M decreases with increasing T_{anneal} and saturates at 4.6eV for T_{anneal} > 800°C. The reduction in Φ_M is not retained with subsequent thermal annealing (*e.g.,* 15m at 800°C in N_2) due to nitrogen out-diffusion, however. In order to prevent out-diffusion, a TiN capping layer can be used, so that low Φ_M is maintained with additional thermal annealing. By selectively using a TiN capping layer in the n-channel device regions, the HTFGA technique can be applied to achieve dual work function Mo gate electrodes suitable for advanced CMOS technologies employing thin-body MOSFETs.

In order to clarify the mechanism of Mo Φ_M reduction, the physical microstructure and chemical composition are investigated using high-resolution transmission electron microscopy (HR-TEM). For un-implanted Mo film, Φ_M is mainly determined by the structural modification in the film. Chemical modification (nitrogen segregation) to the Mo-SiO_2 interface is considered as a major effect for Φ_M reduction of N^+ implanted Mo film until Φ_M increases again with subsequent thermal annealing (especially for thick Mo film > 50nm). HTFGA can more effectively reduce Φ_M

dominantly by chemical modification, *i.e.,* nitridation of the whole Mo film, with relatively improved crystalline quality compared to N^+ implanted Mo.

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Chapter 4 : Strained-Si Technologies

4.1 Introduction

The performance of integrated circuits including cost-per-function has been dramatically improved by geometric scaling of Si CMOS devices. From a unit device performance point of view, the success of scaling depends on achieving higher on-state drive current (I_{on}), while maintaining as low as possible off-state leakage current (I_{off}). I_{on} can be increased in three major ways: increasing areal gate capacitance (C_{ox}), decreasing gate length (L_g), or increasing carrier mobility (μ), which can be easily expected from the long-channel MOSFET drain current equation below.

$$I_{on} \sim \mu C_{ox} \frac{W}{L_g} (V_{gs} - V_t)^2$$

where

μ : carrier mobility

C_{ox} : gate capacitance

W : channel width

L_g : gate length

V_{gs} : gate to source voltage

V_t : threshold voltage

To date, device performance has been mainly improved by geometrical scaling, such as scaling down of gate oxide thickness (T_{ox}) and gate length (L_g). However, before L_g scaling is limited by lithography technology, the severe SCEs (especially increased I_{off}) are becoming a dominant factor limiting L_g scaling [1]. T_{ox} scaling is also limited by the quantum mechanical tunneling, which induces severe gate leakage current through the gate dielectric with thickness of less than 2nm [2]. Increased channel doping concentration, such as halo or pocket implants, can suppress I_{off} but degrades carrier mobility due to increased vertical electric field and more impurity scattering. In addition, statistical fluctuation of channel dopants causes more V_t variations, especially for the nanoscale regime [3].

To overcome the current geometrical scaling limit, the industry needs a new scaling vector. Mobility scaling is getting attention as a very promising scaling vector to improve drive current [4-6]. Strained Si technologies have been widely studied as a promising means for mobility scaling [7-17]. Mobilities of both electrons and holes can be improved by applying stress to induce appropriate strain in the channel, *e.g.,* tensile strain for n-channel MOSFETs and compressive strain for p-channel MOSFETs [13, 14]. It can be mainly understood by changes in complicated electronic band structures [18, 19]. On the other hand, piezoresistance (PR) model suggests relatively easy approach to correlate the channel stress components with mobility changes [20-22]. In this chapter, the physics of strained Si is reviewed using electronic band structures and the simple PR model is also introduced to quantify mobility enhancement induced by strain.

4.2 Physics of strained Si

Uniaxial and/or biaxial tensile strain changes the electronic band structure of Si with an indirect band gap, leading to carrier repopulation and band splitting between subvalleys, resulting in a change in effective carrier mobility [18, 23]. In other words, strain enhances the carrier mobility, which is given by $\mu = q\tau/m^*$, by reducing the conductivity effective mass (m^*) and/or increasing the relaxation time (τ) [5].

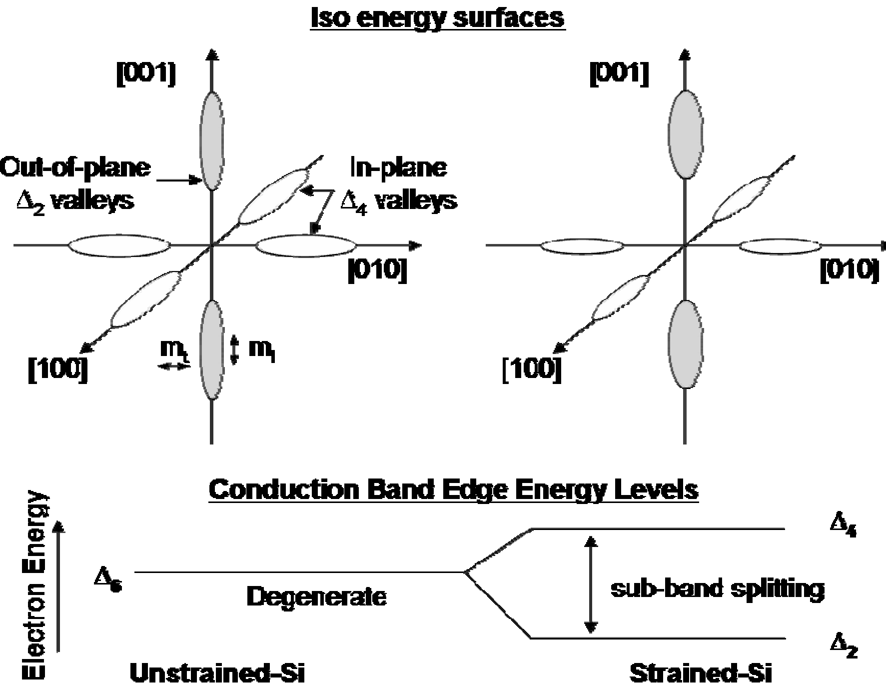

Figure 4.1: The effect of biaxial tensile strain on the Si conduction band structure [6].

For example, biaxial tensile strain reduces the total electron conductivity effective mass (m^*) and suppresses inter-valley scattering due to band repopulation and sub-band splitting as shown in Fig. 4.1. The conduction band of unstrained-Si consists of six

degenerate valleys or bands of equal energy along (100) orientations of k-vector. The total electron conductivity effective mass (m*) of unstrained Si is obtained by adding the contributions of the six degenerate valleys with anisotropic effective masses, m_l (longitudinal effective mass) and m_t (transverse effective mass). Since the effective mass is inversely proportional to the curvature of the electron energy function in each direction, $m_l=0.98m_0$ is larger than $m_t=0.19m_0$, where m_0 is the free electron mass. When biaxial tensile strain is applied on a (001) Si wafer, the strain removes the degeneracy between the four in-plane valleys (Δ_4) and the two out-of-plane valleys (Δ_2) by lifting the energy of Δ_4 and lowering the energy of Δ_2. Thus, Δ_2 valleys with small in-plane effective mass (m_t) and large out-of-plane effective mass (m_l) are preferentially occupied by electrons, reducing total in-plane electron conductivity effective mass. At the same time, the energy splitting between Δ_4 and Δ_2 valleys also suppresses inter-valley scattering.

The biaxial tensile strain also improves hole mobility by reducing hole conductivity effective mass and suppressing inter-valley scattering. With strain, the hole conductivity effective mass becomes anisotropic due to band warping, and holes preferentially occupy higher energy light hole (LH) valleys due to energy splitting (Fig. 4.2). As a result, the net in-plane hole conductivity effective mass becomes smaller, resulting in enhanced hole mobility. However, this effect is relatively small for biaxial tensile strain. The hole mobility enhancement under biaxial tensile strain is mainly due to the large reduction of hole inter-valley scattering from energy splitting between light hole (LH) and heavy hole (HH) bands, especially for stress higher than 1GPa.

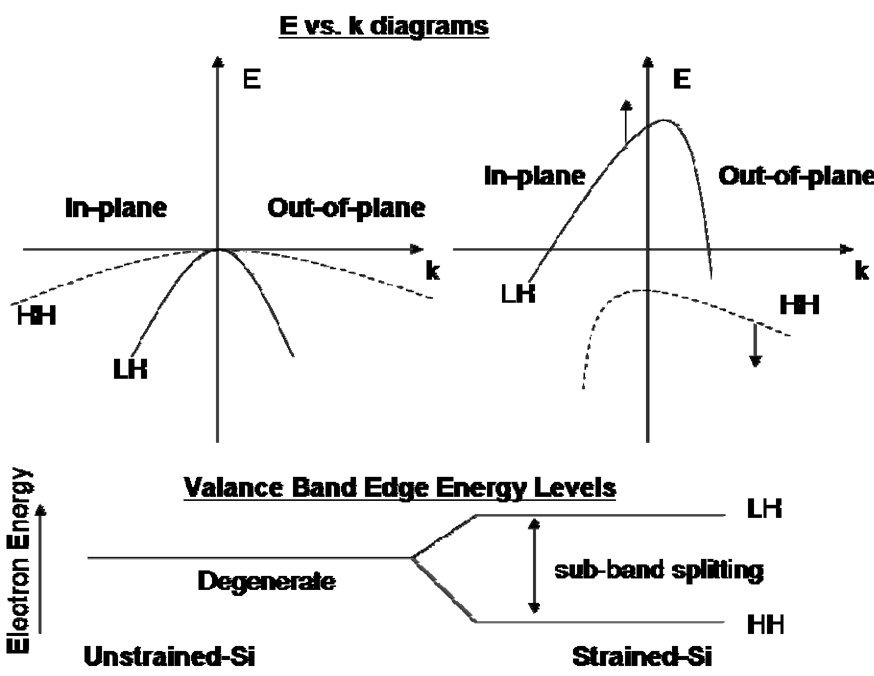

Figure 4.2: The effect of biaxial tensile strain on the Si valance band structure [6].

However, this energy splitting between LH and HH bands decreases at high vertical electric field (E_{eff}) due to the quantum mechanical confinement effect as shown in Fig. 4.3. Actually, at high E_{eff} (>0.6MV/cm), the hole mobility with biaxial tensile strain is almost the same as that of the bulk Si PMOS devices [11]. This can be explained by surface confinement effect in the inversion layer, which also splits the LH and HH bands under high E_{eff} [5]. In this case, the strain-induced splitting mainly depends on the magnitude of the out-of-plane effective masses. As E_{eff} increases, the sub-bands will shift down due to the quantum confinement effect. In particular, the bands with a light out-of-plane effective mass will shift more in energy relative to bands with a heavy mass. Under biaxial tensile strain, the top-most occupied band is the LH band with a lower out-of-plane effective mass compared to the next occupied band (HH band). As a result, the

band splitting is reduced dramatically since the LH band shifts down faster than the HH band with quantum confinement.

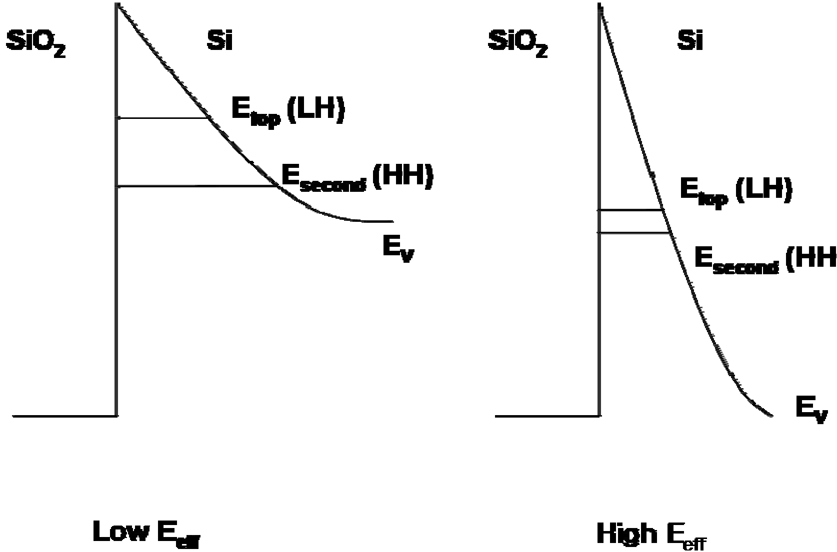

Figure 4.3: The effect of vertical electric field on valence band splitting of biaxial tensile strained Si [5].

Uniaxial strain along the silicon channel has been also widely used to enhance both electron and hole mobilities. Similar to biaxial tensile strain, uniaxial tensile strain improves electron mobility by reducing the net in-plane conductivity effective mass by band repopulation, i.e., electrons preferentially occupy the four lower energy valleys (unstrained valleys) with small in-plane effective mass. Inter-valley scattering is also suppressed by the energy splitting between strained valleys (two in-plane valleys) and unstrained valleys (two in-plane and two out-of-plane valleys) but this is smaller than that for biaxial strain, giving an advantageously small NMOSFET V_t shift [24].

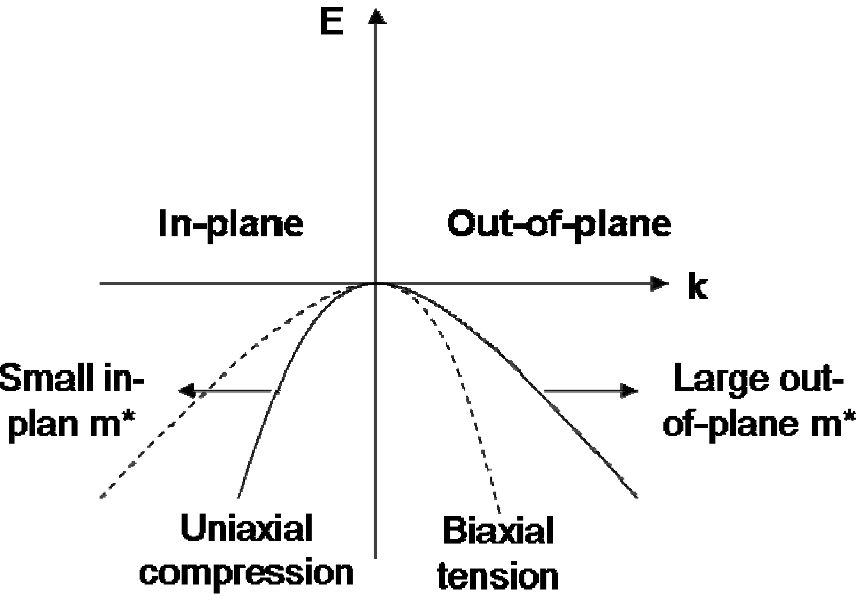

Figure 4.4: The valance band structures for strained Si under longitudinal uniaxial compression and biaxial tension [6].

On the other hand, uniaxial compressive strain improves hole mobility more effectively as compared to biaxial tensile strain. Under uniaxial compressive strain, the net in-plane hole conductivity effective mass becomes much smaller due to reduced in-plane hole conductivity effective mass of the top (LH) band, while biaxial tensile strain shows the opposite top band curvature as shown in Fig. 4.4. The reduction of hole inter-valley scattering from energy splitting between light hole (LH) and heavy hole (HH) bands also improves hole mobility. In particular, the band splitting is maintained even at high E_{eff} due to anisotropic out-of-plane hole effective masses of top (LH) and second (HH) bands. The top (LH) band has larger out-of-plane hole conductivity effective mass, hence less band shifting down toward the second (HH) band. On the contrary, the HH band has smaller out-of-plane hole conductivity effective mass, hence more band shifting

down toward the next sub-band. As a result, band splitting is maintained, even increased, at high E_{eff} under uniaxial compressive strain. For electrons, band splitting is also maintained at high E_{eff} regardless of strain types because the out-of-plane electron conductivity effective mass (m_l) for the top-most occupied band (Δ_2) is always large.

Finally, it is also expected that the performance enhancement induced by strain will be maintained even in the ballistic transport regime for very small L_g. As MOSFET carrier transport becomes more ballistic, the carrier transport can be limited by carrier injection at the source. Assuming current continuity, the on-state drive current (I_{on}) can be given by

$$I_{on} = WC_{ox} < \upsilon(0) > \left(V_{gs} - V_t\right)$$

where $<\upsilon(0)>$ is the average velocity of carriers at the beginning of the channel [25]. The maximum value of $<\upsilon(0)>$ is approximately the equilibrium uni-directional thermal velocity (υ_T), because the positive velocity carriers at the beginning of the channel are injected from source, which is at the thermal equilibrium [26]. The thermal velocity is mainly determined by the lattice temperature and the effective mass. In fact, υ_T is inversely proportional to the square root of the effective mass. Therefore, the strain-induced reductions in the effective mass will still enhance the drive current in ballistic MOSFETs.

4.3 Piezoresistance Model

The resistance change (ΔR) of a metal gauge by applied stress (σ) mainly originates from dimensional changes in the length, width and/or thickness of the gauge. On the contrary, in semiconductor gauges, the resistivity change ($\Delta\rho$) is the dominant factor for the resistance change induced by stress [27]. The relationship between the applied stress and the resistivity change in a semiconductor can be expressed by

$$\frac{\Delta\rho}{\rho} = \Pi X$$

where Π is a six-by-six matrix of piezoresistance (PR) coefficients and X is the stress vector with six compontents of σ_{11}, σ_{22}, σ_{33}, σ_{23}, σ_{13}, and σ_{12}. For a semiconductor with cubic symmetry such as silicon, Π reduces to

$$\Pi = \begin{pmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{pmatrix}$$

with three primary axes of [100], [010] and [001]. In this case, the resistivity change along [100] can be expressed by $\Delta\rho_{[100]}/\rho = \pi_{11}\sigma_{11} + \pi_{12}\sigma_{22} + \pi_{12}\sigma_{33}$. In addition, since mobility (μ) is inversely proportional to the resistivity, the mobility change by the applied stress can be expressed by $\Delta\mu/\mu = -\Delta\rho/\rho = -\Pi X$. The three fundamental cubic PR coefficients (π_{11}, π_{12} and π_{44}) have been experimentally obtained by Smith for n-type and p-type silicon as shown in Table 4.1 [20].

Table 4.1: Bulk silicon piezoresistance (PR) coeffiecients measured by Smith [20].

Type & Resistivity	PR coefficients [10^{-11} Pa^{-1}]		
	π_{11}	π_{12}	π_{44}
n-Si (11.7Ω-cm)	-102.2	53.4	-13.6
p-Si (7.8Ω-cm)	6.6	-1.1	138.1

The PR coefficients for arbitrary crystallographic directions can be obtained by an appropriate coordinate transformation [21]. Typically, two different PR coefficients are considered to explain the effect of uniaxial stress. One is the longitudinal PR coefficient (π_l) relating the stress and the change in resistivity when the directions of stress and current are parallel to each other. The other is the transverse PR coefficient (π_t) relating the stress and the change in resistivity when the directions of stress and current are perpendicular to each other. Table 4.2 shows the PR coefficients for a right-handed Cartesian coordinate system whose three axes have direction cosines [l_1 m_1 n_1], [l_2 m_2 n_2], and [l_3 m_3 n_3] with respect to the cubic axes. Here, π_v is another type of π_t with different stress direction, *i.e.,* π_v also accounts for the relationship between the stress and current perpendicular to each other. For MOSFETs, the stress directions corresponding to π_l, π_v, and π_t are along the channel (σ_{xx}), vertical to the channel (σ_{yy}), and across the channel (σ_{zz}), respectively as shown in Fig. 4.5.

Table 4.2: The PR coefficients for arbitrary crystallographic directions of uniaxial stress and current ([l m n] : direction cosines).

Stress Axes	PR coefficients Formula
x [l_1 m_1 n_1]	$\pi_l = \pi_{11} - 2(\pi_{11} - \pi_{12} - \pi_{44})(l_1^2 m_1^2 + m_1^2 n_1^2 + n_1^2 l_1^2)$
y [l_2 m_2 n_2]	$\pi_v = \pi_{12} + (\pi_{11} - \pi_{12} - \pi_{44})(l_1^2 l_2^2 + m_1^2 m_2^2 + n_1^2 n_2^2)$
z [l_3 m_3 n_3]	$\pi_t = \pi_{12} + (\pi_{11} - \pi_{12} - \pi_{44})(l_1^2 l_3^2 + m_1^2 m_3^2 + n_1^2 n_3^2)$

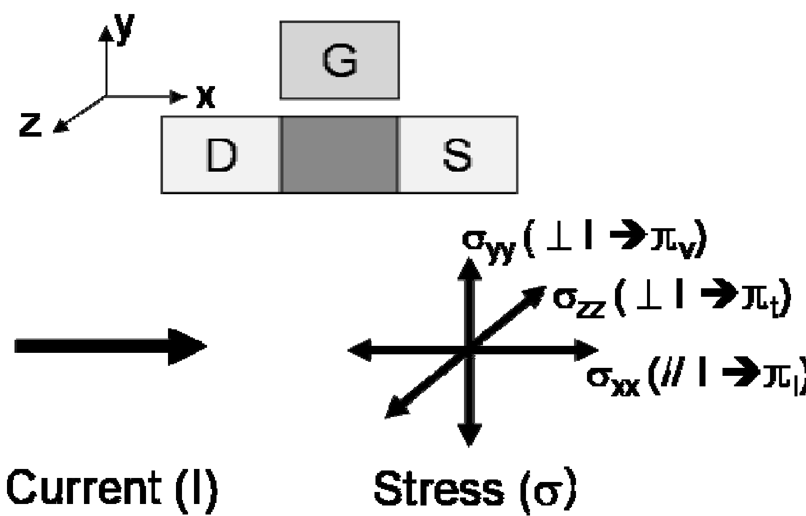

Figure 4.5: Axes definition for stress and current in MOSFETs. (σ_{xx}: stress along the channel, σ_{yy}: stress vertical to the channel, σ_{zz}: stress across the channel)

Table 4.3 shows axes configurations for three typical channel surface/current orientations of vertical multiple-gate (MuG) FET and bulk/planar MOSFET devices. The three different configurations can be obtained by simple layout rotation together with adopting a substrate with {} and/or {110} surface orientations. The channel surface of a

MuGFET device is the sidewall of the semiconductor fin, resulting in different definitions of three axes (x, y and z) between the MuGFET and the bulk MOSFET to maintain the physical meaning of stress directions to be the same, *i.e.,* x: along the channel, y: vertical to the channel, and z: across the channel.

Table 4.3: Axes configurations for three typical channel surface/current orientations of MuGFET and bulk/planar MOSFET devices.

MuGFET/ Bulk (or planar)	Surface/ Current	x	y	z
MuGFET (axes z, x, y)	{100]/ <100>	<100>	<010>	<001>
	{110]/ <110>	$\langle 1\bar{1}0 \rangle$	<110>	<001>
	{100]/ <110>	$\langle 1\bar{1}0 \rangle$	<001>	<110>
Bulk (or planar) (axes y, x, z)	{100]/ <100>	<100>	<001>	$\langle 0\bar{1}0 \rangle$
	{110]/ <110>	$\langle \bar{1}10 \rangle$	<110>	$\langle 00\bar{1} \rangle$
	{100]/ <110>	<110>	<001>	$\langle 1\bar{1}0 \rangle$

The impact of stress components parallel to the three primary axes on carrier mobility in MuGFET and bulk/planar MOSFET devices are summarized in Table 4.4 and Table 4.5, respectively. In order to account for mobility change (not resistivity change), a minus sign is put on the PR coefficients which are obtained from the formula in Table 4.2. Bulk Si PR coefficients measured by Smith [20] are used to quantify the percent change in mobilities of PMOS and NMOS devices with 1GPa tensile stress. Only a change in the sign of the percent change in mobilities is necessary for -1GPa compressive stress. For

more accurate PR modeling, the impurity concentration-dependent PR coefficients need to be considered [22].

Table 4.4: The impact of 1GPa tensile stresses parallel to the three primary axes on mobility enhancement of MuGFET devices

	% change in mobility per +1GPa					
	{100} Surface <100> Current		{110} Surface <110> Current		{100} Surface <110> Current	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
σ_{XX} (along channel)	$-\pi_{11}$		$-(\pi_{11}+\pi_{12}+\pi_{44})/2$		$-(\pi_{11}+\pi_{12}+\pi_{44})/2$	
	102.2	−6.6	31.2	−71.8	31.2	−71.8
σ_{YY} (vertical to channel)	$-\pi_{12}$		$-(\pi_{11}+\pi_{12}-\pi_{44})/2$		$-\pi_{12}$	
	−53.4	1.1	17.6	66.3	−53.4	1.1
σ_{ZZ} (across channel)	$-\pi_{12}$		$-\pi_{12}$		$-(\pi_{11}+\pi_{12}-\pi_{44})/2$	
	−53.4	1.1	−53.4	1.1	17.6	66.3

Table 4.5: The impact of 1GPa tensile stresses parallel to the three primary axes on mobility enhancement of bulk/planar MOSFET devices

	% change in mobility per +1GPa					
	{100} Surface <100> Current		{110} Surface <110> Current		{100} Surface <110> Current	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
σ_{XX} (along channel)	$-\pi_{11}$		$-(\pi_{11}+\pi_{12}+\pi_{44})/2$		$-(\pi_{11}+\pi_{12}+\pi_{44})/2$	
	102.2	−6.6	31.2	−71.8	31.2	−71.8
σ_{YY} (vertical to channel)	$-\pi_{12}$		$-(\pi_{11}+\pi_{12}-\pi_{44})/2$		$-\pi_{12}$	
	−53.4	1.1	17.6	66.3	−53.4	1.1
σ_{ZZ} (across channel)	$-\pi_{12}$		$-\pi_{12}$		$-(\pi_{11}+\pi_{12}-\pi_{44})/2$	
	−53.4	1.1	−53.4	1.1	17.6	66.3

As shown in Table 4.5, about 30% NMOS mobility enhancement is expected when 1GPa tensile stress is applied along the channel with {100} channel surface/<110> current flow direction, which is a typical surface/current orientation for bulk MOSFETs. On the other hand, -1GPa compressive stress along the channel is necessary to improve PMOS mobility by about 70% for the same device configuration. Many experimental data have shown the effect of uniaxial tensile (compressive) stress along the channel for NMOS (PMOS) devices with {100} channel surface/<110> current flow direction, supporting the validity of the PR modeling [7, 8, 13, 14]. It is also consistent with experimental data that in plane (x-z plane for bulk MOSFETs) biaxial tensile stress is beneficial to improve bulk NMOS with {100} channel surface/<110> current flow direction.

4.4 Conclusion

The physical mechanisms of strain-induced mobility enhancement of silicon are reviewed. Strain changes the electronic band structure, such as the carrier repopulation and band splitting between subvalleys, resulting in a change in carrier mobility. The biaxial tensile strain is beneficial for both NMOS and PMOS mobility enhancement by reducing the net in-plane effective mass (m*) and suppresses inter-valley scattering. However, the hole mobility enhancement under biaxial tensile strain is relatively small because it is mainly due to the large reduction of hole inter-valley scattering, which requires high stress level (>1GPa). In addition, the hole mobility enhancement under biaxial tensile stress is reduced at high vertical effective field (E_{eff}) because the energy

splitting between LH and HH bands decreases at high E_{eff} due to the quantum mechanical confinement effect.

Uniaxial tensile strain also enhances electron mobility by reducing effective mass and suppressing inter-valley scattering. However, the energy splitting between strained valleys and unstrained valleys are smaller than that of biaxial strain, giving an advantageously small NMOSFET V_t shift. Uniaxial compressive strain improves hole mobility more effectively comparing to biaxial tensile strain because the effective mass becomes much smaller than that of biaxial tensile strain. Under uniaxial compressive strain, the band splitting is maintained even at high E_{eff} due to anisotropic out-of-plane hole effective masses of top (LH) and second (HH) bands. The performance enhancement induced by strain will be maintained even at the ballistic transport regime with very small L_g. This can be explained by strain-induced effective mass reduction, which increases thermal velocity (υ_T).

A simple PR model is introduced to quantify strain-induced mobility enhancement. The PR coefficients with arbitrary crystallographic orientations can be obtained by an appropriate coordinate transformation. The impact of stress on mobility enhancement of MuGFET and bulk/planar MOSFET devices with different surface/current orientations are quantitatively investigated using the bulk Si PR coefficients measured by Smith. For more accurate PR modeling, the impurity concentration-dependent PR coefficients need to be considered.

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Chapter 5 : Strain Effects on MuGFET Performance

5.1 Introduction

Enhancement of carrier mobilities by stress is necessary to sustain the historical pace of improvement in transistor performance with gate-length scaling, and is already used in leading-edge CMOS technology today [1, 2]. In order to induce appropriate strain in the channel region of MOSFETs, various techniques have been introduced such as substrate-induced strain, process-induced strain, and bending-induced strain [3-6]. The expitaxially grown Si on relaxed $Si_{1-x}Ge_x$ layer is a typical example of substrate-induced strain. The lattice of the Si layer is stretched (biaxial tensile strain) in the plane of the interface due to the lattice mismatch between Si and $Si_{1-x}Ge_x$ [7, 8]. By increasing Ge concentration (x), more biaxial tensile strain in the Si layer is induced as long as its thickness is under critical thickness. However, strain relaxation during high temperature processes and high defect density (*e.g.,* misfit and threading dislocations) remain issues for production. In addition, the hole mobility enhancement is reduced at high E_{eff} for biaxial tensile strain [9].

Process-induced strain can be applied during the fabrication process by adding new process steps or using existing process steps with relatively low cost. In addition,

typical process-induced strain technologies, such as strained capping layer and embedded $Si_{1-x}Ge_x$ source/drain, are known to generate uniaxial strain along the channel, which offers similar electron mobility enhancement compared with biaxial strain, while the hole mobility enhancement is retained at high E_{eff} [1]. Therefore, it has been effectively applied for the 90nm node and beyond. However, special layout engineering is required for practical application because process-induced stain is localized strain and depends on the physical dimensions of the transistor, such as gate length and channel width [10, 11] as well as the surrounding structures.

Strain in the Si channel can be also induced by bending the Si wafer directly or bending a package substrate with a Si chip glued firmly on it [12]. Package strain can further improve CMOS performance after the fabrication with low cost. In addition, the performance of both short and long channel devices can be improved by bending-induced strain because it is global strain [13].

In addition, advanced transistor structures such as multiple-gate field-effect transistors (MuGFETs) [14-16] improve carrier mobilities further because a heavily-doped channel is not necessary to control short-channel effects as compared with the bulk-Si MOSFET; hence they may be adopted in CMOS technology nodes toward the end of the roadmap [17]. Optimization of channel surface crystalline orientations for maximum carrier mobilities can also provide for a significant improvement in CMOS performance [18]. The ultimate CMOS technology will utilize each of these approaches (strained Si, MuGFETs, and channel orientation optimization) for performance enhancement. Thus, the enhancement of MuGFET performance via process-induced strain has been investigated recently by several groups [19-25].

In this chapter, the effects of strain on the performance of n-channel and p-channel MuGFETs with {110}/<110> and {100}/<100> surface-orientation/current-direction are investigated. All three types of strain technologies (substrate-induced, process-induced, and bending-induced strains) are introduced. First, impact of strained SOI (sSOI) substrate on MuGFET performance is experimentally studied. As process-induced strain, strained capping layer and tensile metal gate are introduced. Finally, the impact of biaxial convex bending on MuGFET performance is presented. Mechanisms affecting carrier mobility in thin-body (fully depleted) MOSFET structures are also elucidated by using the piezoresistance (PR) model introduced in Chapter 4.

5.2 Substrate-induced strain: Impact of sSOI substrate on MuGFET performance

In order to investigate the impact of substrate-induced strain on MuGFET performance, (001) sSOI wafers with 60nm strained silicon top layer and 150nm buried oxide (BOX) were used as starting material. Control devices were made on Standard Unibond® SOI wafers with the same body thickness (T_{si}) and BOX thickness as the sSOI wafers. Raman spectroscopy analyses (Fig. 5.1) showed that the starting sSOI material had 1.5GPa biaxial tensile strain. After a nitride hardmask deposition, sub-20nm-wide fins were defined with 193nm lithography and reactive ion etching (RIE). Fig. 5.2 shows the cross-sectional TEM of sSOI fins covered by the poly-Si gate layer for a) {110}/<110> fin cross-section and b) {100}/<100> fin cross-section. No additional processing was done to smoothen the fin sidewalls, so the etched surfaces are rough and

degrade inversion-layer mobility at high transverse fields [15]. The MuGFETs in this work have large source and drain contact landing pads (> 1μm x 1 μm).

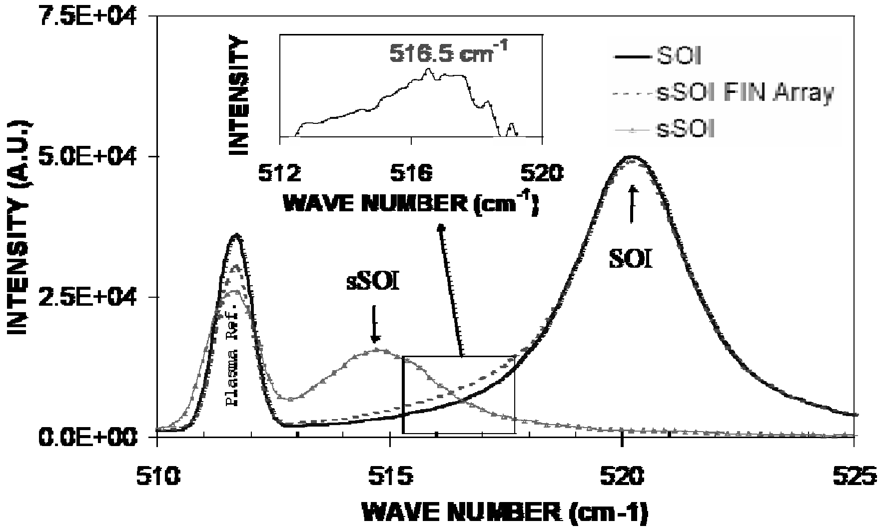


Figure 5.1: UV-Raman spectra for starting sSOI and SOI wafers. The inset shows the difference of signals from sSOI fin array right after fin patterning and SOI wafer. A peak at 516.5cm^{-1} indicates that 1.1GPa strain is retained on <20nm-wide fins

The dotted line in Fig. 5.1 shows the Raman spectroscopy scan of a 200 μm long fin array (4000 fins in parallel). A peak at 516.5cm^{-1} is observed when we subtract the silicon signal from the sSOI fin array signal, which indicates that 1.1GPa or 75% of the original strain was retained for the <20nm-wide fins (Fig. 5.1 inset). The fins were doped by ion implantation to ~10^{18}/cm^3 for both NMOS and PMOS. Gate oxide (2nm) was grown by In-Situ Steam Generated Oxidation (ISSG) at 900°C for 25 seconds followed by poly-Si gate deposition. FinFETs with {110} and {100} channel surface crystalline orientations were made on the same wafer by rotating the fin layout orientation by 45

degrees. Source/drain ion implant peaks were 25nm into the Si to avoid complete amorphization of the sSOI film. Dopants were activated by a 1060°C, spike anneal.

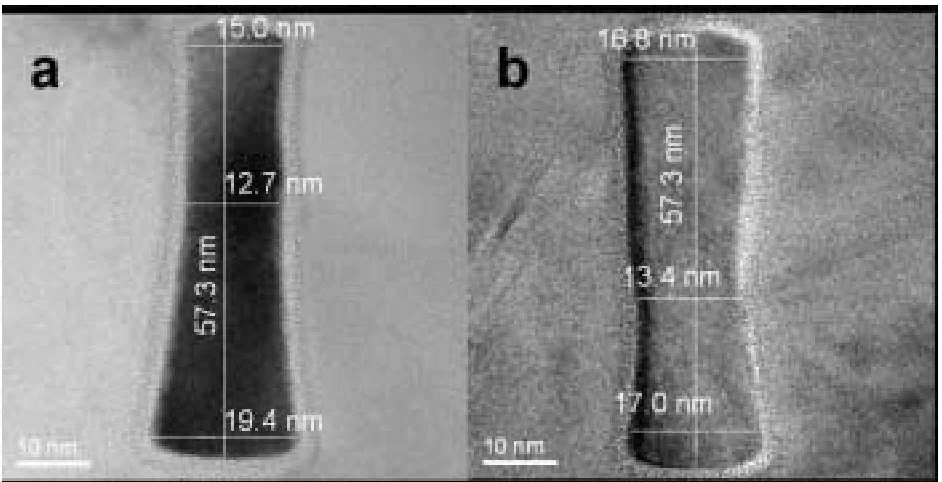


Figure 5.2: Cross-sectional HRTEM images of sub-20nm sSOI fins under the poly-Si gate a) {110}/<110> fin. <110> direction is perpendicular to the plane of the cross section; (b) {100}/<100> fin. <100> direction is perpendicular to the plane of the cross section. {100} fins are made by rotating the fin layout by 45 degrees.

Fig. 5.3 shows L_g=10um NMOS and PMOS linear G_m-V_g curves for 20-fin devices with {110}/<110> and {100}/<100> fin surface/direction, respectively. For NMOS devices, sSOI V_t is 100mV lower than for the control devices due to the conduction-band shift induced by strain [26, 27]. The linear drive current at a fixed gate overdrive for the sSOI devices is 55% or 23% higher than for the control devices, for {110}/<110> or {100}/<100> fins, respectively. Electron mobility *vs.* inversion charge density (Q_{inv}) is plotted in Fig. 5.4. sSOI provides 60% enhancement in {110} electron mobility and 30% enhancement in {100} electron mobility, at $Q_{inv}=1.5\times10^{-6}$ C/cm^2.

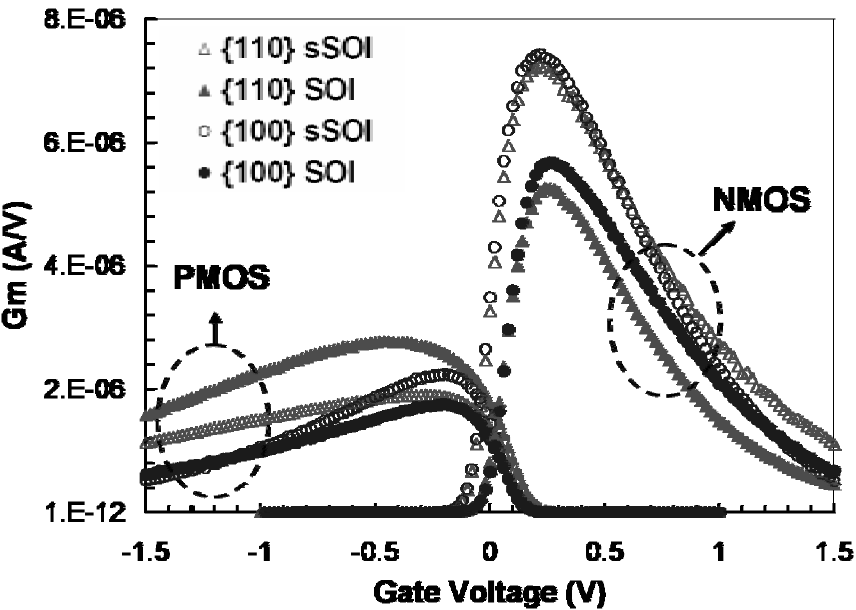


Figure 5.3: Measured NMOS and PMOS G_m-V_g curves for both {110}/<110> and {100}/<100>. L_g=10μm, 20-fin devices. NMOS sSOI V_t is 100mV lower than SOI V_t due to a strain-induced shift in conduction-band edge.

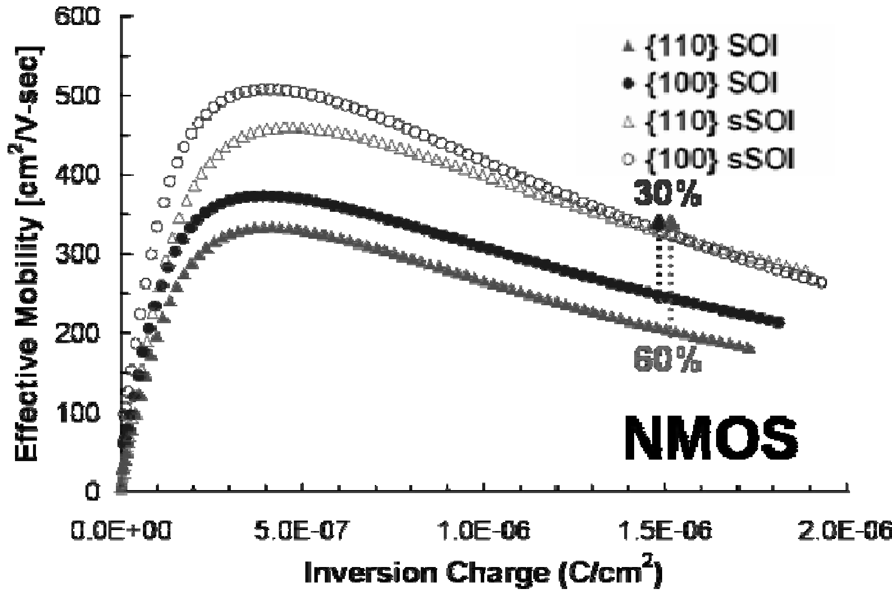


Figure 5.4: Electron mobility *vs.* inversion charge density. Mobility was measured on 10μm L_g, 20-fin devices with the split C-V method. At higher Q_{inv}, the mobility difference between {100} and {110} sSOI is minimal.

For PMOS devices, less than 25mV V_t reduction for sSOI *vs.* SOI devices is seen because the strain-induced valence-band shift is smaller than the conduction-band shift [26, 27]. Fig. 5.5 shows sSOI degrades {110}/<110> hole mobility by 35%. However, sSOI provides significant enhancement in {100)/<100> hole mobility: 30% at low Q_{inv}, decreasing to 18% at high Q_{inv}.

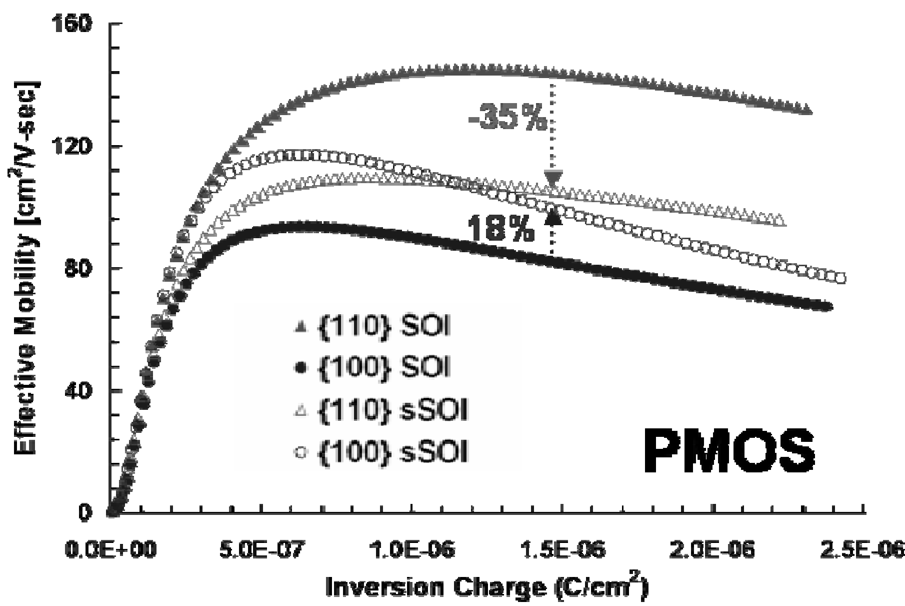


Figure 5.5: Hole mobility *vs.* inversion charge density. Mobility was measured on 10μm L_g, 20-fin devices with the split C-V method. Enhancement in {100}/<100> sSOI mobility decreases with increasing Q_{inv}.

For the 3-D MuGFET, the plane of current conduction is orthogonal to the plane of the substrate, thus the effect of a biaxially strained sSOI substrate is expected to be different for a MuGFET as compared to a planar MOSFET. The experimentally observed

effect of strain on MuGFET carrier mobility can be used to estimate the average stress in each direction within the channel using the PR model.

Table 5.1 summarizes the measured mobility enhancement percentage values (at Q_{inv}=1.5×10^{-6} C/cm^2) for MuGFETs fabricated in this work. The coefficients taken from Smith [28] are for lightly doped Si, whereas those from K. Matsuda *et al*. [29] are for heavily doped Si (>10^{18} cm^{-3}). Uniaxial tensile σ_{xx} stress is inadequate to explain the observed mobility change. The best fit of the bulk-Si piezoresistance model to the experimental results is achieved assuming significant tensile σ_{xx} (1.23GPa) and tensile σ_{yy} (1.11GPa), and compressive σ_{zz} (-0.41GPa), utilizing the heavily doped Si coefficients [29].

Table 5.1: Summary of experimentally measured mobility enhancement percentage values for MuGFETs fabricated in this work.

		STRESS (MPa)			MOBILITY ENHANCEMENT (%)			
		σ_{XX}	σ_{YY}	σ_{ZZ}	{100} NMOS	{110} NMOS	{100} PMOS	{110} PMOS
Experiment					30	60	18	-35
Theory	Smith	0.5	0	0	51.1	15.6	-3.3	-35.9
	Smith	0.8	0.6	0	23.5	38.2	-4.7	-40.5
	Smith	0.77	0.69	-0.3	30.3	60.6	-4.7	-35
	Matsuda	1.23	1.11	-0.4	29.5	60.3	2.7	-36

The fitting is done by adjusting the σ_{xx}, σ_{yy}, and σ_{xx} values until the mobility enhancements calculated using the formula as below (uniquely match the experimental results).

Mobility enhancement [%]

$= (\Delta\mu/\mu)\times100$ [%]

$= [(1-\pi_l\times\sigma_{xx})\times(1-\pi_v\times\sigma_{yy})\times(1-\pi_t\times\sigma_{zz})-1]\times100$ [%]

For example, 30% mobility enhancement for a {100} NMOS is obtained based on the simple calculation $[(1+1.022\times0.77)\times(1-0.534\times0.69))\times(1-0.534\times(-0.3))-1]\times100=30$ [%].

This inverse modeling result is consistent with the strain measurement from Raman spectroscopy (Fig. 5.1 inset). Furthermore, the large reduction in NMOS V_t (-100mV) observed on sSOI samples also suggests that a significant amount of strain is retained through the MuGFET processing. Hole mobility enhancement for {100}/<100> fins is higher than predicted by piezoresistance considerations alone. This is due to higher sensitivity of {100} hole mobility at higher levels of stress (>0.5GPa), caused by scattering suppression and significant energy-level splitting which is not predicted by the piezoresistance model as observed for planar {100} PMOSFETs [30].

In conclusion, it is found that for fin widths down to <20nm, strain can be retained in patterned sSOI films to provide mobility enhancements in MuGFET devices. This is likely dependent on the source/drain geometry. For the devices studied here, the Si fins were "anchored" by large source/drain pad regions. NMOS MuGFET mobility is improved by 60% and 30% for {110}/<110> and {100}/<100> fin surface/direction, respectively. Although PMOS MuGFET mobility is degraded by 35% for {110}/<110> fins, it is enhanced by up to 18% for {100}/<100> fins. Therefore, sSOI can be used for

performance enhancement of CMOS MuGFETs with {100}/<100> fins, or it can also enhance the performance of CMOS MuGFETs with {110}/<110> fins as long as strain in PMOS region can be relaxed. These results are qualitatively consistent with predictions based on bulk-Si piezoresistance coefficients.

5.3 Process-induced strain

5.3.1 Simulation study of FinFETs with strained capping layer

The technique of inducing stress by using a tensile (for NMOS) or compressive (for PMOS) SiN_x capping layer is attractive because of its relatively simple process and its extendibility from bulk-Si to silicon-on-insulator (SOI) MOSFETs [31]. In this section, the impact of tensile and compressive capping layers on electron and hole mobilities is investigated for Si fins with {100} sidewalls and <100> current-flow direction, and Si fins with {110} sidewalls and <110> current-flow direction, which are optimal for maximum electron and hole mobilities, respectively [32, 33]. The effects of various structural parameters (gate-electrode thickness, gate length, and fin aspect ratio) are studied to provide insight for strain engineering in non-planar FET structures. The classic bulk-Si PR model is then used to predict the impact on carrier mobilities.

Fig. 5.6 shows the nominal 3-D FinFET structure used for Ansys 5.7 simulations in this work. The 100nm-thick SiN_x capping layer has uniform hydrostatic stress of either 1GPa (tensile) or -1GPa (compressive). The bottom, left, and right surfaces in Fig. 5.6 are constrained to zero displacement. (The bottom surface is the bottom of the 400nm-thick buried oxide.) It is assumed that a thin gate oxide layer will have negligible effect on the stress transfer from the capping layer to the channel, and so it was

not included in the simulated structure, for simplicity. A thick dielectric hard mask on top of the fin was not included, for relevance to the tri-gate FET. (The contribution of the top fin surface to FinFET current is negligible [34].)

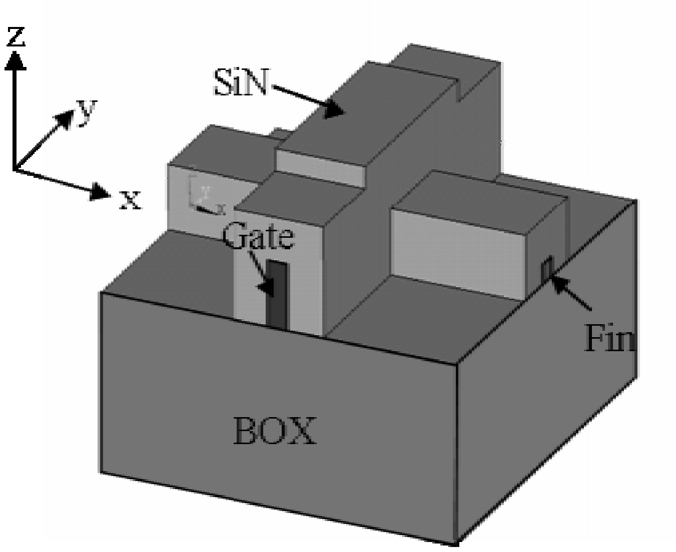


Figure 5.6: 3-D structure used for simulations.

(Nominal values: BOX Thickness=400nm, Fin Width=50nm, Fin Height=50nm, Gate Length=50nm.)

Two types of Si fins, shown in Fig. 5.7, were studied. Note that these can be achieved on a standard {100} Si starting substrate with <110> notch, by orienting the PMOS fins parallel or perpendicular to the notch and rotating the fin layout orientation for NMOS fins by 45° [35].

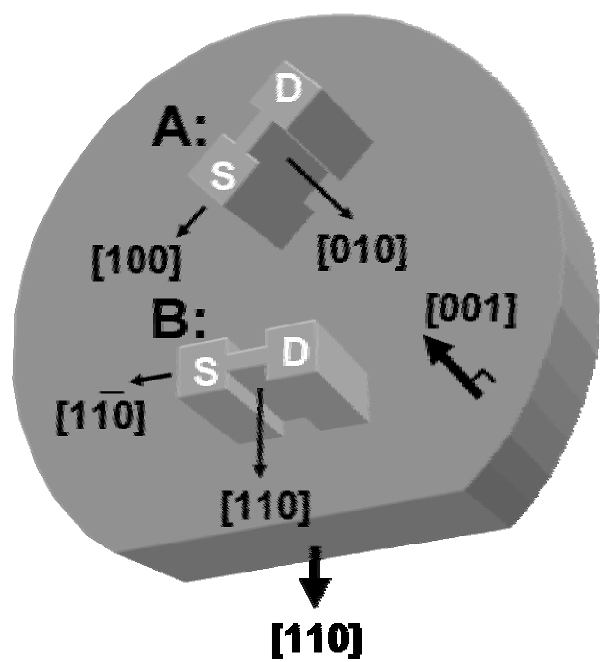


Figure 5.7: Two Fin orientations studied in this work.

A: {100} channel surface (side walls of Fin) with <100> current direction.

B: {110} channel surface (side walls of Fin) with <110> current direction.

Table 5.2 shows the values of expected percentage change in carrier mobility for NMOS and PMOS devices per 1GPa (tensile or compressive) stress along the channel in each direction (ref. Fig. 5.6). As shown in Chapter 4, these were derived from classic bulk-Si PR coefficients [28] for the specific crystallographic directions of uniaxial stress and current, by appropriate coordinate transformations [36], and were used to calculate the net impact of 3-D stress on carrier mobility. Table 5.3 lists the default structural parameters for various cases studied in this work.

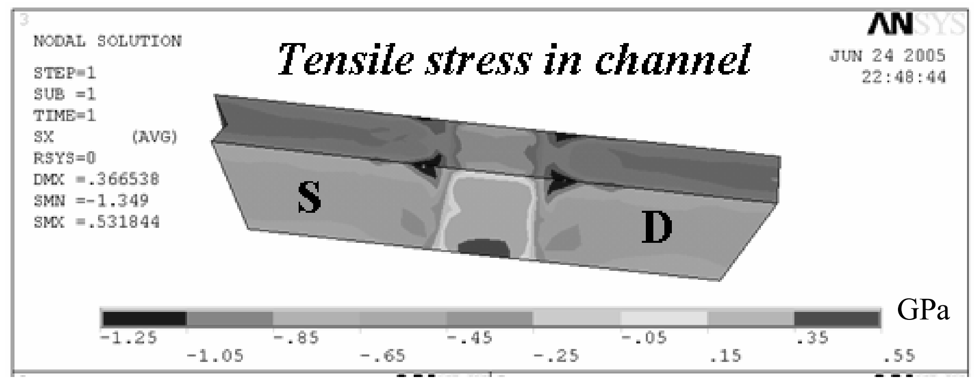
Table 5.2: Expected percentage change in mobilities per 1GPa tensile channel stress based on piezoresistance coefficients. For compressive stress, these values should be multiplied by -1

	% change in mobility per +1GPa			
	{100} surface		{110} surface	
	NMOS	PMOS	NMOS	PMOS
σ_{XX} (along channel)	$-\pi_{11}$		$-(\pi_{11} + \pi_{12} + \pi_{44})/2$	
	102.2	-6.6	31.2	-71.8
σ_{YY} (vertical to channel)	$-\pi_{12}$		$-(\pi_{11} + \pi_{12} - \pi_{44})/2$	
	-53.4	1.1	17.6	66.3
σ_{ZZ} (across channel)	$-\pi_{12}$		$-\pi_{12}$	
	-53.4	1.1	-53.4	1.1

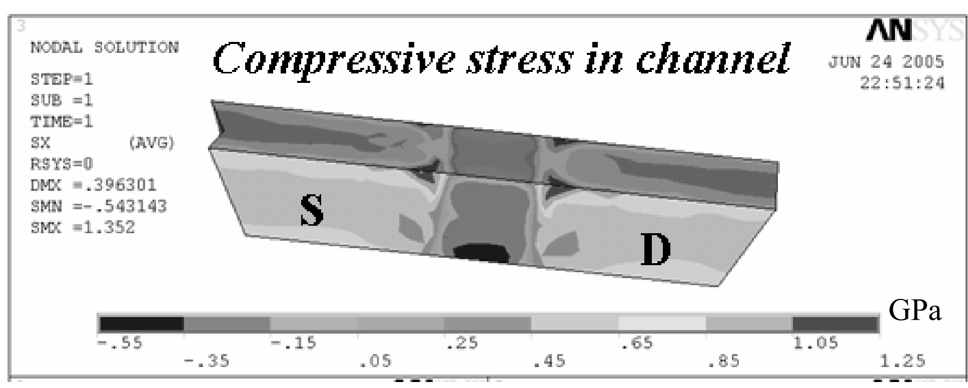
Table 5.3: Structural parameters for each of the cases.

	{100} Nominal	{100} HAR	{110} Nominal	{110} HAR
T_{SiN} [nm]	100	100	100	100
W_{Fin} [nm]	50	25	50	25
T_{Fin} [nm]	50	100	50	100
L_g [nm]	50	50	50	50
T_{Gate} [nm]	150	150	150	150
T_{BOX} [nm]	400	400	400	400
Surface Orientation	{100}	{100}	{110}	{110}

The 3-D profiles of stress parallel to the direction of current flow (σ_{xx}) are shown in Fig. 5.8(a) and 5.8(b), for {100}-sidewall fins (aspect ratio = 1) with a tensile capping layer and a compressive capping layer, respectively. Note that the stress profiles are identical, except for a change in sign. The amount of induced stress in the channel depends on the distance between the capping layer and the fin, which increases toward the bottom of the fin due to the non-zero thickness of the gate electrode. Thus, the induced stress profile is non-uniform from the top to the bottom of the fin.



(a) With tensile capping layer (1GPa)



(b) With compressive capping layer (-1GPa)

Figure 5.8: 3-D stress profiles along the channel direction (σ_{xx}) in the {100} Fin surface.

The average stress in each direction along each fin channel surface, induced by a 1GPa tensile or -1GPa compressive capping layer, is summarized in Table 5.4. Tensile σ_{xx} is induced along the {100} fin sidewall with a tensile capping layer. In contrast, compressive σ_{xx} is induced along the {110} fin sidewall with a tensile capping layer. Sidewall-surface values are listed under "DG"; top-surface values are listed under "TG". For TG, the impact of sidewall is weighted by a factor of 2 in the mobility enhancement factor calculation.

Table 5.4: Summary of average induced stress along the fin surfaces and the resultant impact on carrier mobilities, for fins with aspect ratio = 1 ("Nominal").

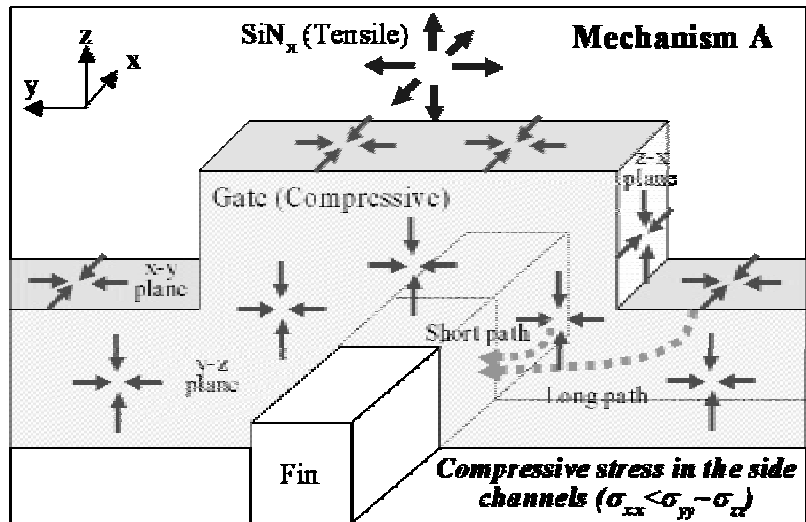
Stress in Channel [GPa]	Tensile Capping Layer (1GPa)				Compressive Capping Layer (-1GPa)			
	{100}		{110}		{100}		{110}	
	DG	TG*	DG	TG*	DG	TG*	DG	TG*
σ_{xx}	0.24	-0.13	-0.35	-0.48	-0.24	0.13	0.35	0.48
σ_{yy}	-0.79	-1.25	-0.89	-1.29	0.79	1.25	0.89	1.29
σ_{zz}	-0.68	-1.07	-0.92	-1.17	0.68	1.07	0.92	1.17
% change in μ_n	***141%***	***137%***	12%	10%	-72%	-76%	-35%	-38%
% change in μ_p	-3%	-3%	-49%	-60%	3%	3%	***20%***	***21%***

The effect of the fin sidewall crystalline orientation on σ_{xx} is explained with the aid of Fig. 5.9 as follows. There are two pathways for transfer of mechanical stress from the capping layer to the channel. First, stress can be transferred directly through the gate stack (Mechanism A). In this case, a tensile capping layer induces compressive σ_{xx} in the sides of the fin (side channels). The amount of induced stress depends on the distance between the capping layer and the fin, which is the distance between the side channels

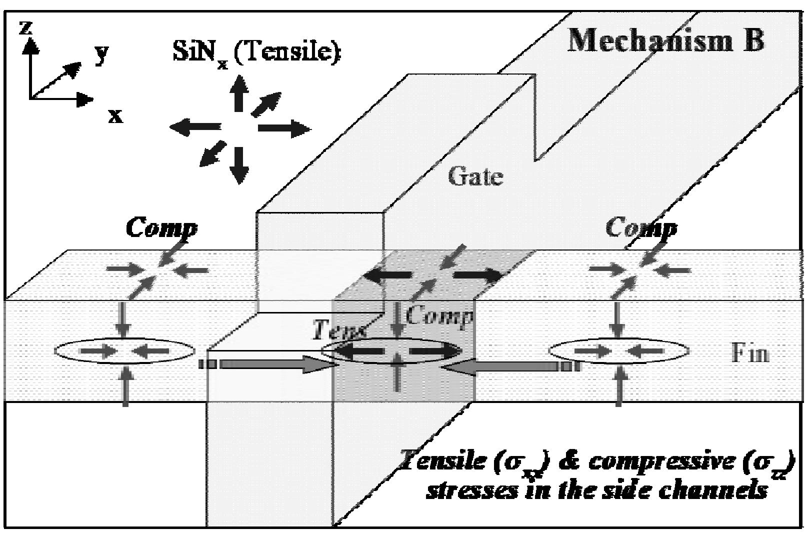
and the planes of the gate surfaces (x-y, y-z and z-x planes). Thus, σ_{xx} induced by this mechanism is smaller at the bottom of the fin than at the top of the fin, due to the non-zero thickness of the gate layer (Fig. 5.9a).

Second, stress can be transferred through the source/drain (S/D) regions (Mechanism B). In this case, tensile stress is induced in the side channels because the capping layer induces compressive stress in the S/D regions (Fig. 5.9b). Higher compressive stress in the S/D regions results in commensurately higher tensile stress in the channel region. Because {110} Si has a higher Young's modulus (E_{110} = 168.0GPa) than does {100} Si (E_{100} = 129.5GPa), it is more difficult to transfer stress from a capping layer to a {110} Si surface, so that Mechanism B yields lower tensile stress for a {110} fin.

The stress distribution in the channel is determined by the superposition of the two mechanisms. Due to the anisotropic Young's modulus, the net σ_{xx} induced within a {100} fin is tensile (dominated by Mechanism B), whereas the net σ_{xx} induced within a {110} fin is compressive (dominated by Mechanism A). The strength of Mechanism B is increased for fins with larger aspect ratio, so that the induced σ_{xx} is more tensile (or less compressive). Stresses σ_{yy} and σ_{zz} induced parallel to the y- and z- directions, respectively, are also determined by the combination of these two stress-transfer mechanisms.



(a) Stress transfer through the gate stack: Compressive stress is induced in the side channels. With increasing distance between the side channels and the planes of the gate surfaces (x-y, y-z and z-x plane), where the stress starts to transfer, stress induced in the side channels decreases.



(b) Stress transfer through the source/drain (S/D) regions: Compressive stress is induced by the capping layer in the S/D regions, which in turn results in tensile stress along the x-direction in the side channels.

Figure 5.9: Stress transfer mechanisms from tensile capping layer to the channel.

For a non-planar transistor structure such as the MuGFET, the other two stress components, σ_{yy} (vertical to the channel surface) and σ_{zz} (across the channel width) can be significant and hence their effects on mobility must be taken into account. Considering the percentage change in mobility per 1GPa stress (ref. Table 5.2) and the average induced 3-D stress along each fin channel surface, the effect of a 1GPa tensile or -1GPa compressive capping layer on FinFET (DG) and tri-gate FET (TG) electron and hole mobilities were calculated and are summarized in Table 5.4 for fin aspect ratio = 1. The results show that electron mobility in a {100}-sidewall double/tri-gate FET can be greatly enhanced (by well over 100%) by a tensile capping layer, due largely to the significant induced compressive σ_{yy} and σ_{zz} as well as the tensile σ_{xx}. Although hole mobility in a {110}-sidewall fin is degraded due to the tensile σ_{xx} induced by a compressive capping layer, it is enhanced more so by the large induced tensile σ_{yy} so that the net impact of a 1GPa compressive capping layer on a {110}-sidewall fin is to enhance the hole mobility by a modest amount (less than 25%).

The effect of gate-electrode thickness (T_{Gate}) on the average induced stress components along the channel surfaces of a {100} fin with aspect ratio = 1 is shown in Fig. 5.10, for a DG device with tensile (1GPa) capping layer. (The induced stress for a compressive capping layer is easily obtained from this data by multiplying it by a factor of -1.) By thinning the gate electrode, the distance between the capping layer and the fin is reduced, facilitating the transfer of stress directly through the gate stack (versus through the S/D regions), causing σ_{xx} and σ_{yy} to become slightly more compressive (or less tensile). The net impact of T_{Gate} scaling on carrier mobilities is small because the

effect of the change in σ_{xx} on mobility is compensated by the effect of the change in σ_{yy} (Fig. 5.11).

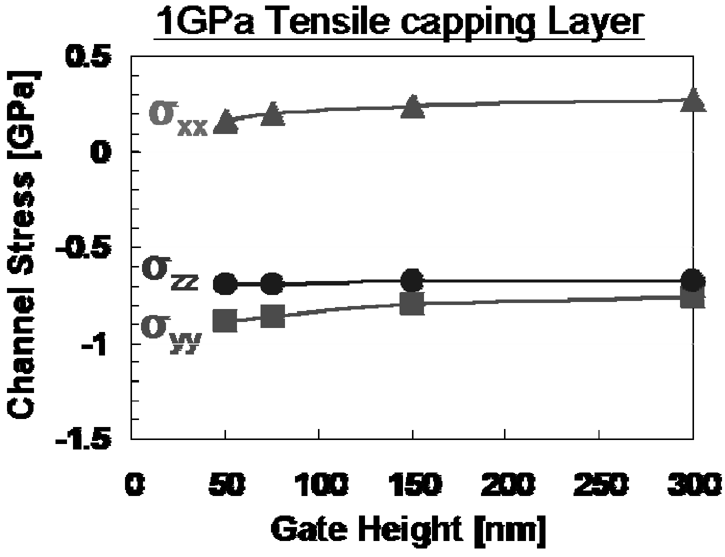


Figure 5.10: Gate height effect on channel stress. Tensile capping layer (1GPa) is applied for {100} nominal structure with various gate thicknesses.

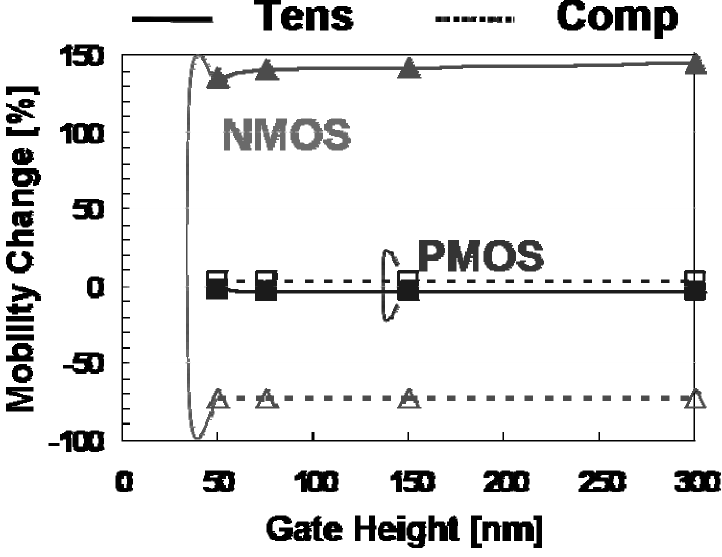


Figure 5.11: Gate height effect on DG mobility enhancement for {100} nominal structure with various gate thicknesses. TG mobility shows almost the same trend (data not shown).

The effect of gate length L_g on channel stress for a {100} fin with aspect ratio = 1 is shown in Fig. 5.12, a DG device with tensile (1GPa) capping layer. As the gate length decreases, the stress transferred through the S/D regions is enhanced compared to the stress transferred directly through the gate (due to the increase in relative volume of the compressively stressed S/D regions). The compressively stressed S/D regions induce compressive σ_{yy} and σ_{zz} in the channel region. For σ_{xx}, the compressive stress in the source/drain regions results in tensile stress in the channel region. If L_g is comparable to the characteristic "decay length" of the compressive strain within the channel region, however, the average σ_{xx} can become more compressive (less tensile) with decreasing L_g, as is seen to be the case for L_g=50nm in Fig. 5.12. The effect of increased compressive σ_{yy} and σ_{zz} is dominant and results in significant enhancement of electron mobility with decreasing L_g (Fig. 5.13).

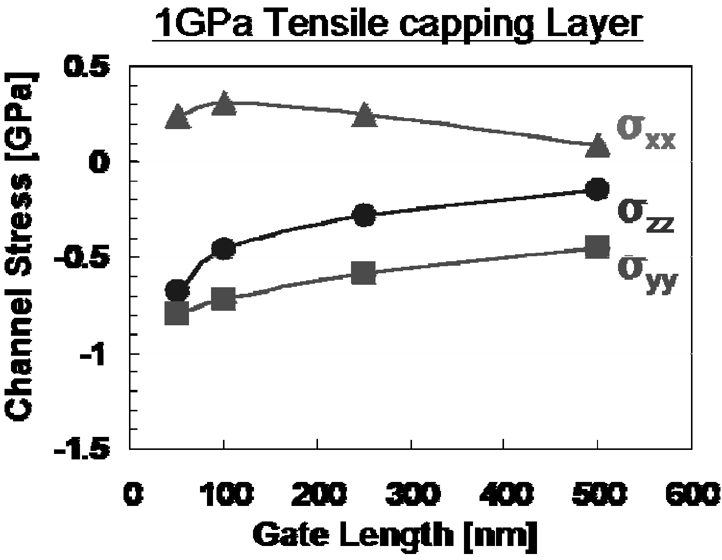


Figure 5.12: Gate length effect on channel stress. Tensile capping layer (1GPa) is applied for {100} nominal structure with various gate lengths.

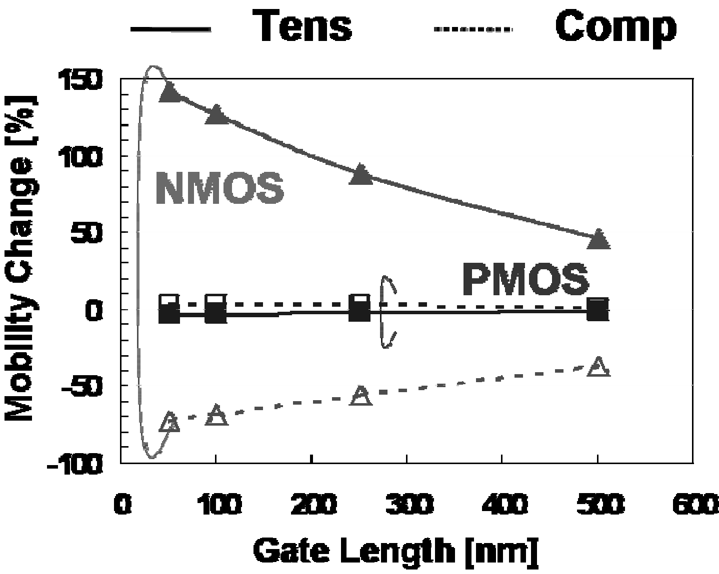


Figure 5.13: Gate length effect on DG mobility enhancement for {100} nominal structure with various gate lengths. TG mobility shows almost the same trend (data not shown).

The effect of fin aspect ratio on channel stress is shown in Fig. 5.14, for a {100} fin (DG) with tensile (1GPa) capping layer and a {110} fin (DG) with compressive (-1GPa) capping layer. The magnitude of the induced σ_{zz} increases (which increases the corresponding mobility enhancement factor), whereas the magnitude of the induced σ_{yy} decreases (which decreases the corresponding mobility enhancement factor), as the fin aspect ratio increases. σ_{xx} becomes less tensile with increasing fin aspect ratio, which decreases the corresponding mobility enhancement (degradation) factor for NMOS (PMOS) devices.

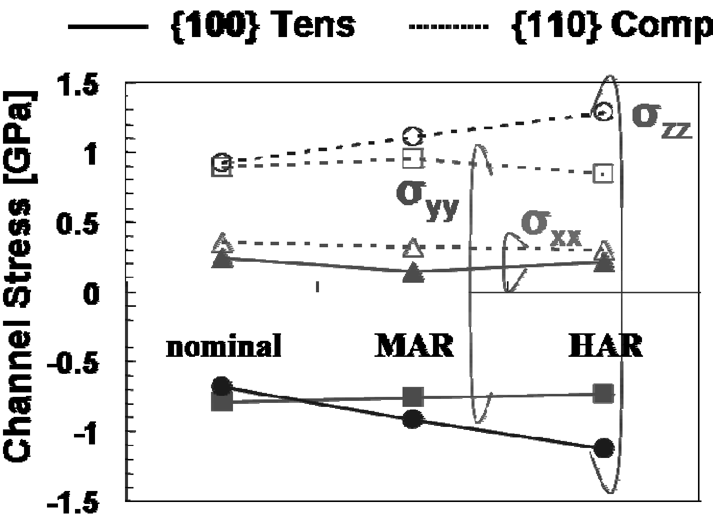


Figure 5.14: Fin aspect ratio effect on channel stress. 1GPa tensile capping layer is used for {100}-sidewall fins and -1GPa compressive capping layer is used for {110}-sidewall fins. Fin width/height for nominal, Moderate Aspect Ratio and High Aspect Ratio is 50nm/50nm, 50nm/100nm and 25nm/100nm, respectively.

The net impact of fin aspect ratio on mobility enhancement is shown in Fig. 5.15 for {100} NMOS with a tensile capping layer and {110} PMOS with a compressive capping layer. NMOS mobility is enhanced the most for a tall and narrow fin (T_{fin}/W_{fin} = 100nm/25nm). PMOS mobility enhancement is maximized for moderate fin aspect ratio > 1. Thus, a stressed capping layer is expected to provide larger enhancement in performance for double-gate FET (FinFET) devices as compared with tri-gate FET devices.

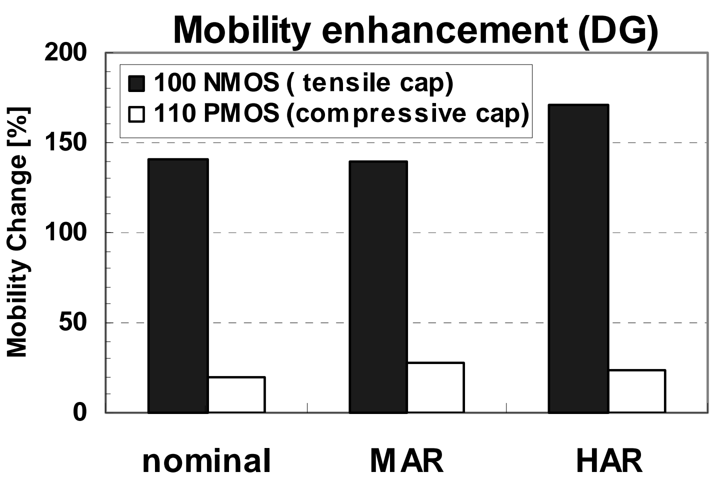


Figure 5.15: Fin aspect ratio effect on DG mobility enhancement for {100} NMOS with 1GPa tensile capping layer and {110} PMOS with -1GPa compressive capping layer.

In conclusion, a tensile capping layer is expected to provide dramatic enhancement (>100%) in electron mobility for a {100}-sidewall fin with <100> current flow, while a compressive capping layer is expected to provide a modest amount (<25%) of hole mobility enhancement for a {110}-sidewall fin with <110> current flow. Therefore, dual stress capping layers with hybrid orientations are still expected to improve the CMOS MuGFET performance. Mobility enhancement is greater for fins with high aspect ratio (greater than 1), so that greater performance enhancement is expected for double-gate-FET (FinFET) *vs.* tri-gate FET devices.

5.3.2 Impact of tensile metal gate on MuGFET performance

A simple method to induce local strain in the channel is to use a stressed gate electrode [37]. In this section, the impact of highly tensile (3GPa) metal gate electrodes on MuGFET performance is presented.

SOI and sSOI wafers with 60nm silicon top layer (T_{Si}) and 150nm buried oxide were used as the starting substrates. The sSOI had initial bi-axial strain of 1.5 GPa as shown previously (Fig. 5.1) Wafers with the T_{Si} <110> notch rotated by 45° were used to fabricate MuGFETs with {100} channel surfaces. The starting T_{Si} was p-type (2x10^{15}/cm^{3}) for both sSOI and SOI wafers. No additional channel doping was used. Fins down to 11nm in width were patterned with 193nm lithography and RIE. UV-Raman measurement of an array of 20nm-wide fins indicated that the sSOI strain was reduced to ~1.1 GPa after fin etching (Fig. 5.1 inset). 2nm SiO_2 gate dielectric was grown by *in-situ* steam oxidation. A 7nm-thick, 3GPa-tensile TiSiN gate layer was deposited by LPCVD, then capped with 100nm poly-Si (Fig. 5.16). Gate electrodes down to 50nm L_g were formed. Implanted source/drain dopants were activated by a 1000°C, 10s anneal. The BEOL process was conventional Al-Si based.

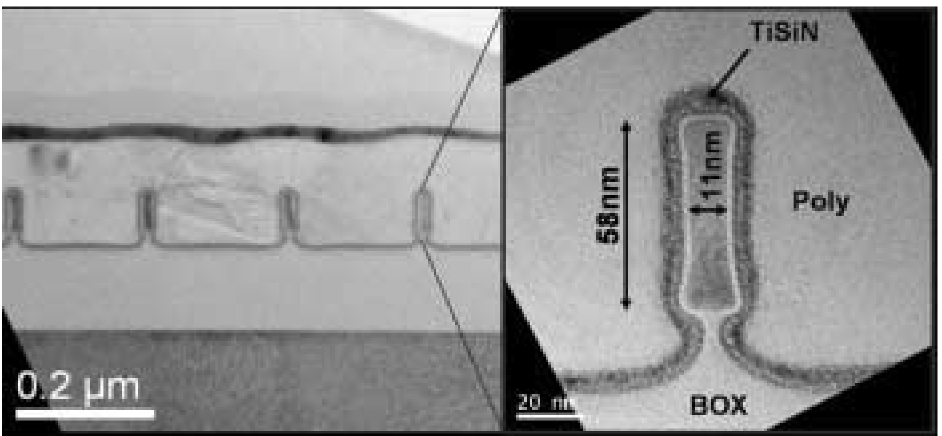
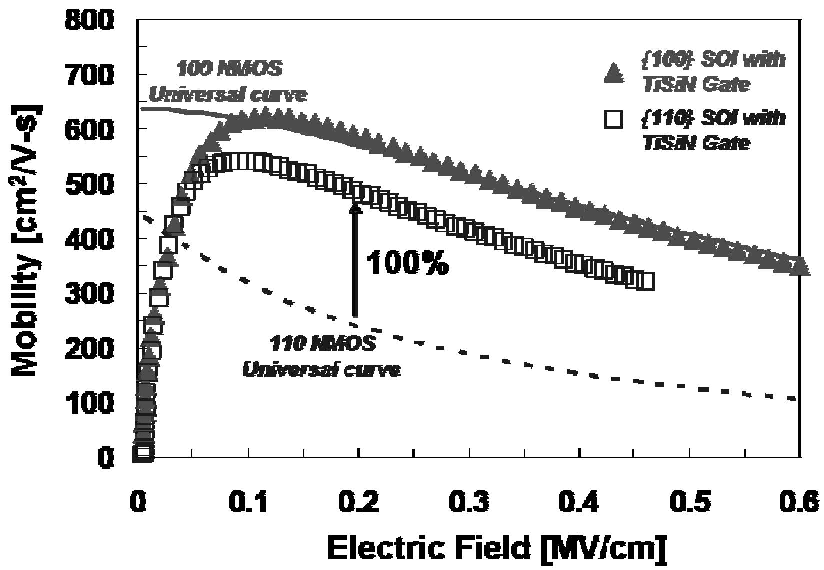


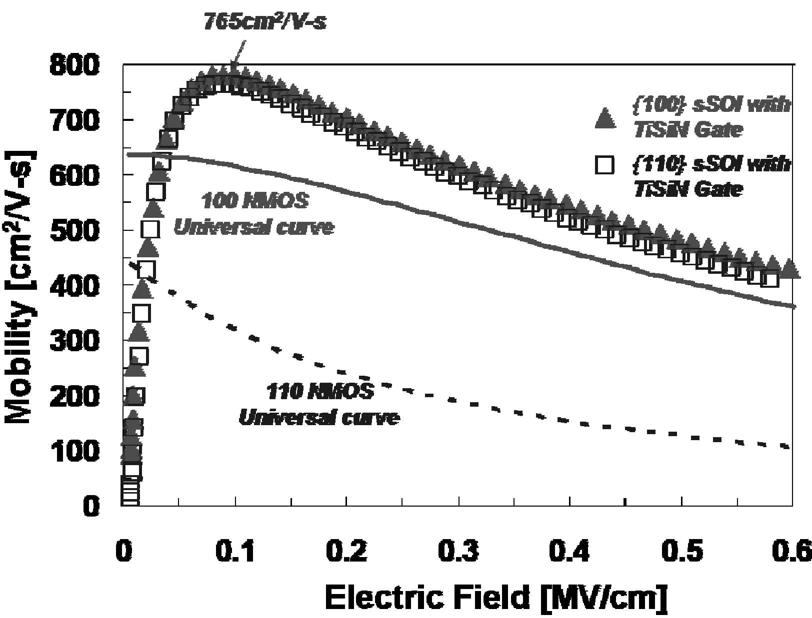
Figure 5.16: Cross-sectional TEM showing the silicon fins under a 3 GPa tensile TiSiN electrode. Fin width is 11nm and fin height is 58nm.

Figure 5.17 shows that the tensile gate improves {110} electron mobility by 100% over the {110} universal curve at a fixed vertical effect electric field (0.2MV/cm), to be 85% of the {100} universal curve. The impact of a tensile gate on {100} electron mobility is minimal. Further enhancement in {110} electron mobility is achieved with fins fabricated from an sSOI substrate. The combination of global strain in the sSOI fins and locally induced strain from the tensile TiSiN gate results in {110} electron mobility above the (100) universal curve, reaching a peak of 765cm^2/V-s.

The tensile gate does not affect {110} hole mobility, but improves {100} hole mobility by ~15%, for SOI PMOS-MuGFETs (Fig. 5.18). The additional use of an sSOI substrate degrades {110} hole mobility by 30%, but improves {100} hole mobility further by 40%. Best PMOS performance is achieved with (110)-sidewall fins fabricated on an SOI substrate.

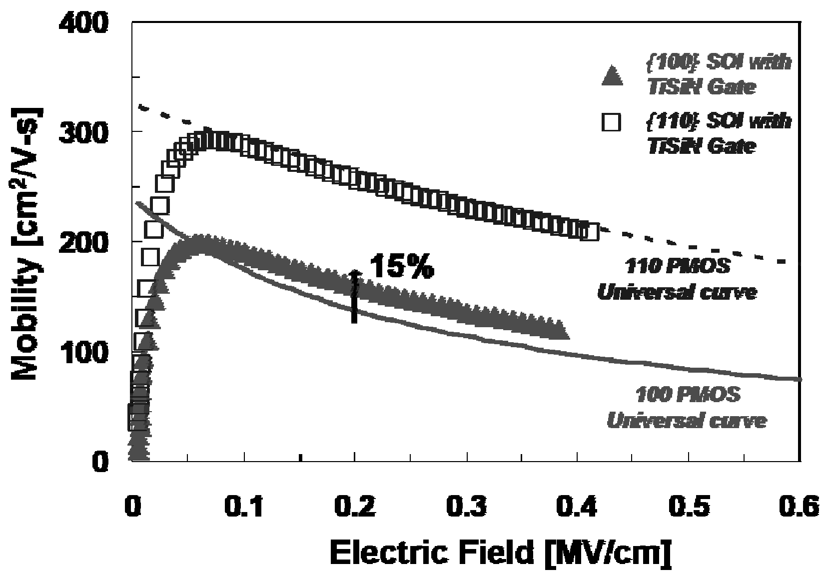


(a) Tensile metal gate-induced strain effect on electron mobility

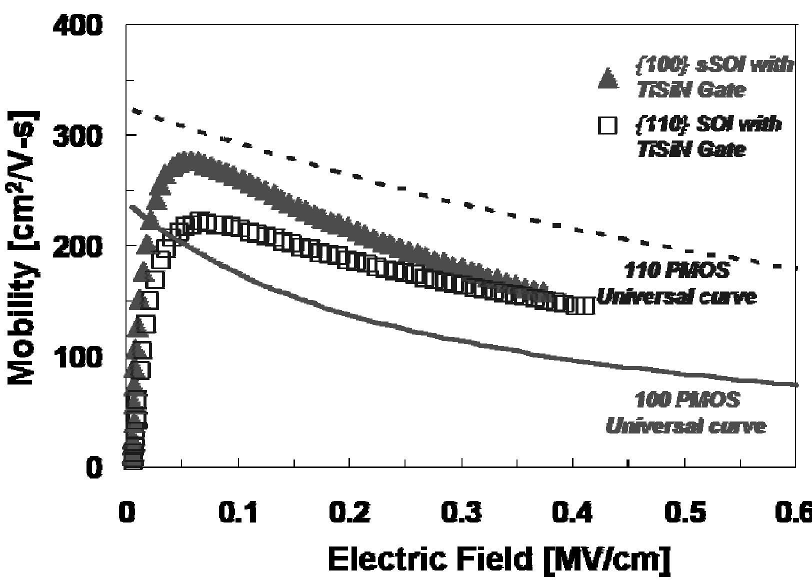


(b) Electron mobility for the combination of sSOI and tensile gate

Figure 5.17: Electron mobility vs. transverse electric field. (a) The tensile metal gate improves {110} electron mobility (solid squares) by 100% over the {110} universal mobility curve. (b) The combination of sSOI and tensile gate pushes the {110} electron mobility to be 20% above the {100} universal curve.



(a) Tensile metal gate-induced strain effect on hole mobility



(b) Hole mobility for the combination of sSOI and tensile gate

Figure 5.18: Hole mobility vs. transverse electric field. (a) {110} hole mobility is not affected by the tensile gate, but {100} hole mobility is improved by 15% over the {100} universal curve. (b) sSOI degrades (110) hole mobility, but improved {100} hole mobility.

The experimental observations can be qualitatively explained using the piezoresistance (PR) model with the same coefficients taken from the previous chapter. Table 5.5 summarizes the measured mobility enhancement values at a fixed transverse electric field (0.2MV/cm) and compares these with values obtained using the bulk-Si PR model. The experimental data can be explained consistently, except for the {100} PMOS-MuGFETs. Again, the {100} PMOS mobility enhancements indicate significant band splitting resulting in suppressed inter-band scattering (not predicted by the bulk-Si PR model).

Table 5.5 Comparison of measured *vs.* predicted mobility enhancements. The experimental findings are consistent with expectations based on inverse modeling using bulk-Si piezoresistance coefficients, except for {100} PMOS devices.

		STRESS (MPa)			MOBILITY ENHANCEMENT (%)			
z, x, y		σ_{xx}	σ_{yy}	σ_{zz}	{100} NMOS	{110} NMOS	*{100} PMOS*	{110} PMOS
GATE INDUCED	EXPERIMENT				3	100	*15*	0
	THEORY	-689	-464	-3330	3	101	*-1*	0
GATE+sSOI INDUCED	EXPERIMENT				24	185	*56*	-28
	THEORY	825	1200	-1630	24	184	*6*	-28

The average stress values obtained by inverse modeling suggest that significant compressive stresses σ_{xx}, σ_{yy}, and especially σ_{zz} are induced along the channel surfaces by the tensile metal gate, while significant tensile σ_{xx} and σ_{yy}, and compressive σ_{zz}, result from a combination of tensile gate and sSOI (bi-axial tensile) starting material.

In conclusion, the use of a highly tensile gate together with an sSOI substrate pushes MuGFET {110} electron mobility to be above the {100} universal curve, reaching a peak of 765cm^2/V-s. However, {110} hole mobility degrades by 30%. Since {110} hole mobility is not affected by the tensile gate stress alone, the use of tensile gates together with an sSOI substrate can be effective to enhance {110} CMOS MuGFET performance if the sSOI can be selectively relaxed in the PMOS regions. On the other hand, the combination of tensile gate with sSOI substrate enhances {100} electron and hole mobilities, and hence is attractive for {100} CMOS MuGFET technology.

5.4 Bending-induced strain: Biaxial convex bending-induced strain effect on MuGFET performance

In this section, the effect of biaxial mechanical bending on n-channel and p-channel MuGFETs with {110}/<110> and {100}/<100> surface-orientation/current-direction is presented. Mechanisms affecting carrier mobility in thin-body (fully depleted) MOSFET structures are elucidated.

(001) Standard Unibond® p-type (2x10^{15}/cm^3) SOI wafers with 60nm-thick silicon top layer and 150nm buried oxide (BOX) were used as the starting material. Device fabrication began with nitride hardmask deposition. Si fins of width down to 20nm were then defined with 193nm lithography and reactive ion etching. {110} and {100} sidewall surface crystalline orientations were made on the same wafer by rotating the fin layout orientation [35]. The gate oxide (2nm) was grown by wet oxidation at 900°C followed by 100nm-thick poly-Si gate deposition. The poly-Si gate was heavily

doped. Both NMOS and PMOS fins were doped to ~5x10^{17}/cm^{3}. Source/drain ion implants were activated by a 1000°C, 10s anneal. The BEOL process was conventional Al-Si based.

A bending apparatus similar to that used by K. Uchida *et al*. [6] was then used to apply stress to the MuGFETs by bending wafer samples biaxially. The induced surface strain was determined from the sample thickness and radius of curvature as measured by a Tencor FLX-2320.

The mobility enhancement parameters in table 5.2 were used again to predict the percentage change in electron (NMOS) and hole (PMOS) mobilities per 1GPa tensile stress in each axis direction. Assuming that current flow along the fin sidewalls is dominant, for NMOS MuGFETs, tensile stress σ_{xx} in the direction parallel to current flow is beneficial, more so for a {100} fin as compared to a {110} fin; tensile stress σ_{yy} in the direction perpendicular to the channel surface is undesirable for a {100} fin but somewhat beneficial for a {110} fin; and compressive stress σ_{zz} across the channel (along the height of the fin) is beneficial for both {100} and {110} fins. Biaxial convex bending should induce tensile σ_{xx} and σ_{yy}, and compressive σ_{zz} in the MuGFETs, and hence is expected to provide significant electron mobility enhancements for {100} and {110} NMOS MuGFETs. For PMOS MuGFETs, biaxial convex bending is not expected to have much impact on hole mobility in {100} fins, and should degrade hole mobility in {110} fins, if the bulk-Si PR model is applicable.

The impact of biaxial convex bending is shown in Fig. 5.19 for {100} and {110} long-channel (L_g=5μm, W_{fin}=20nm) poly-Si-gate NMOS devices, respectively. For 0.11% surface strain (~200MPa), peak electron mobility is improved by 14% for {100} fins and by 26% for {110} fins, with a very slight reduction in threshold voltage (<20mV). Inverse PR modeling is used again to match these observations and it is confirmed that biaxial convex bending induces tensile σ_{xx} and σ_{yy}, and compressive σ_{zz} in the MuGFETs as shown in Table 5.6.

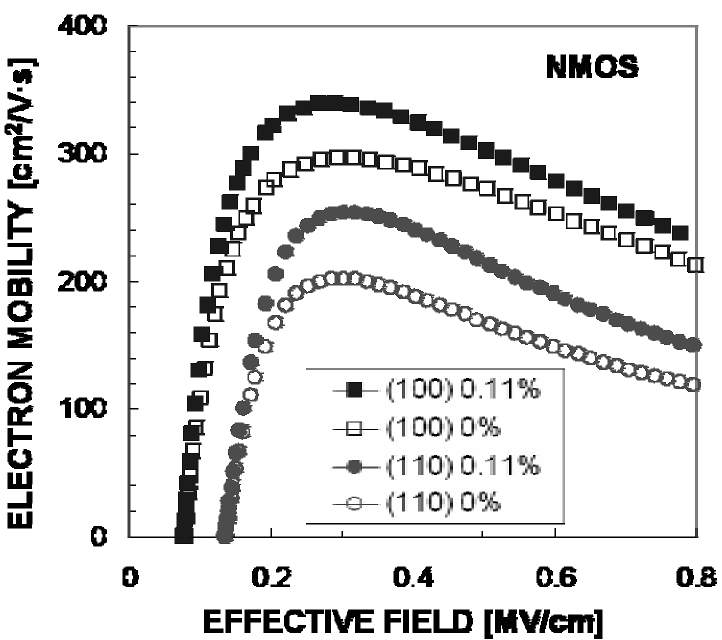


Figure 5.19: Impact of biaxial convex bending on inversion-layer electron mobilities for {100} and {110} long-channel (L_g=5μm, W_{fin}=20nm) poly-Si-gate NMOS devices. For 0.11% surface strain (~200MPa), peak electron mobility is improved by 14% for (100) fins and by 26% for (110) fins.

Table 5.6: Summary of MuGFET mobility enhancements achieved with biaxial convex bending. The 3-dimensional average stress values (σ_{xx}, σ_{yy}, and σ_{xx}) that yield the best theoretical fit of the bulk-Si piezoresistance model to the experimental results are shown.

	STRESS (MPa)			MOBILITY ENHANCEMENT (%)			
	σ_{XX}	σ_{YY}	σ_{ZZ}	(100) NMOS	(110) NMOS	(100) PMOS	(110) PMOS
Experiment				14.4	25.9	8.1	-2.6
Theory	290	350	-160	14.4	25.6	1.7	-2.6

The impact of biaxial convex bending is shown in Fig. 5.20 for {100} and {110} long-channel (L_g=1μm, W_{fin}=20nm) poly-Si-gate PMOS devices, respectively. Surprisingly, a noticeable improvement (8%) in {100} hole mobility is seen. This is indicative of band splitting, resulting in suppressed inter-band scattering (not predicted by the bulk-Si PR model), consistent with a previous report [20]. The observed small (<3%) degradation in (110) hole mobility is close to that predicted by the bulk-Si PR model (Table 5.6).

Figure 5.21 shows the percent change in peak linear transconductance (g_m) induced by biaxial convex bending, as a function of gate length for MuGFETs with {100}/<100> surface-orientation/current-direction. It can be seen from this figure that the bending-induced performance enhancement is largely retained with gate-length scaling down to 80nm. This is expected, since bending is a global strain method.

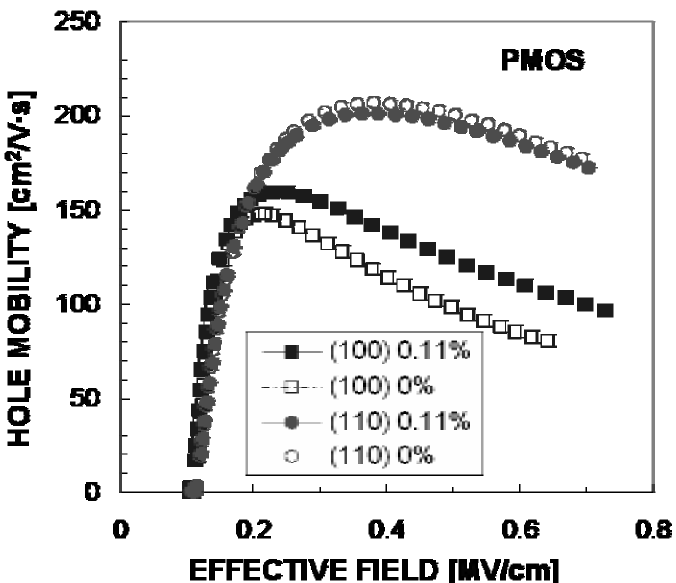


Figure 5.20: Impact of biaxial convex bending on inversion-layer hole mobilities for {100} and {110} long-channel (L_g=1µm, W_{fin}=20nm) poly-Si-gate PMOS devices. For 0.11% surface strain (~200MPa), surprisingly, a noticeable improvement (8%) in {100} hole mobility is seen and small (<3%) degradation in {110} hole mobility is observed.

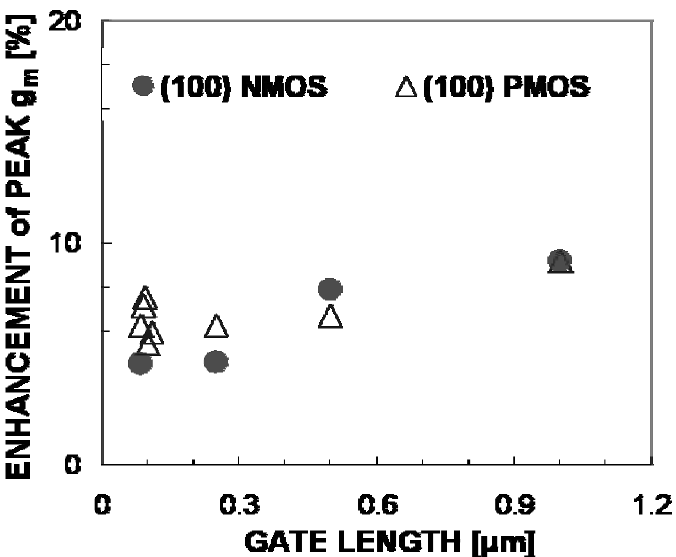


Figure 5.21: Peak g_m enhancement induced by biaxial convex bending as a function of gate length, for NMOS and PMOS MuGFETs with {100}/<100> surface-orientation/current-direction.

In conclusion, biaxial convex wafer bending is an effective means for enhancing {100} CMOS MuGFET performance with a relatively low level (~0.1%) of strain, post-fabrication. The bending-induced performance enhancement is largely retained with gate-length scaling. This makes package strain a potentially attractive approach to enhancing MuGFET-based CMOS performance at low cost. This technique will therefore be available in complement with local and/or other global (*e.g.,* sSOI) strain techniques.

5.5 Conclusion

The effects of strain on the performance of CMOS MuGFETs with {110}/<110> and {100}/<100> surface-orientation/current-direction have been investigated. First, substrate-induced strain was studied and it was found that sSOI improves {110} and {100} electron mobility by 60% and 30%, respectively. Although {110} hole mobility is degraded by 35%, {100} hole mobility is enhanced by up to 18%. Therefore, sSOI is suggested for performance enhancement of {100} CMOS MuGFETs, or {110} CMOS MuGFETs with selective strain relaxation in PMOS region.

A tensile capping layer is expected to provide dramatic enhancement (>100%) in {100} electron mobility, while a compressive capping layer is expected to provide a modest amount (<25%) of {110} hole mobility enhancement. Therefore, dual stress capping layers with hybrid orientations are suggested as a promising performance booster of CMOS MuGFETs. Mobility enhancement is greater for fins with high aspect ratio (greater than 1), so that greater performance enhancement is expected for double-gate-FET (FinFET) *vs.* tri-gate FET devices.

A highly tensile gate together with an sSOI substrate pushes {110} electron mobility to be above the {100} universal curve, while degrading {110} hole mobility by 30%. Since {110} hole mobility is not affected by the tensile gate stress alone, the use of tensile gates together with an sSOI substrate can be effective to enhance {110} CMOS MuGFET performance if the sSOI can be selectively relaxed in the PMOS regions. The combination of tensile gate with sSOI substrate also enhances {100} electron and hole mobilities, and hence is attractive for {100} CMOS MuGFET technology.

Finally, biaxial convex wafer bending improves {100} CMOS MuGFET performance with a relatively low level (~0.1%) of strain, post-fabrication. In addition, the performance enhancement is largely retained with gate-length scaling, making package strain potentially attractive for enhancing MuGFET-based CMOS performance at low cost.

Mechanisms affecting carrier mobility in MuGFET structures are investigated by using piezoresistance (PR) model introduced in Chapter 4. All the experimental results are qualitatively consistent with predictions based on classic bulk-Si PR coefficients [28].

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Chapter 6 : Conclusion

6.1 Summary

For the past four decades, the performance of very-large-scale integrated (VLSI) circuits and cost-per-function has been steadily improved by geometric scaling of MOSFETs. From a unit device performance point of view, the success of transistor scaling depends on achieving high on-state drive current (I_{on}), while maintaining low off-state leakage current (I_{off}). However, as the gate length (L_g) decreases, short-channel effects (SCE) become severe, resulting in dramatic increase in I_{off}. Increased channel doping has been widely implemented via lateral channel engineering such as halo or pocket implants to suppress I_{off}. However, carrier mobility is degraded with these techniques due to increased vertical electric field and impurity scattering. In addition, statistical dopant fluctuation effects result in threshold voltage (V_T) variation, especially in the nanoscale regime.

Advanced transistor structures, such as multiple-gate (MuG) or ultra-thin-body (UTB) silicon-on-insulator (SOI) MOSFETs, are very promising for extending MOSFET scaling because SCE can be suppressed without high channel doping concentrations, resulting in enhanced carrier mobilities. However, the manufacturability of advanced device structures is still an issue, especially for double-gate (DG) devices. Many different methods have been proposed to fabricate DG devices but most of them suffer from

technical challenges mainly due to the process complexity [1-5]. Above all, performance fluctuations due to process-induced parameter variations is expected to be more significant for DG devices [6].

In addition, advanced transistor structures require metal gate technology, preferable with tunable work function (Φ_M) for V_T adjustment. Metal gate technology can also facilitate MOSFET scaling because it eliminates the issues of poly-Si gate technology, namely the gate depletion effect and boron penetration. The ranges of Φ_M required to fully adjust the V_T values of thin-body (fully depleted) MOSFETs for various applications is 4.4eV to 4.6eV for n-channel devices and 4.8eV to 5.0eV for p-channel devices [7]. Various approaches have been reported to achieve appropriate metal gate work functions. Among them Mo gate technology with tunable work function induced by N^+ implantation has been successfully used to achieve proper V_T values for thin-body CMOSFETs [8].

Strained-Si technology is beneficial for enhancing carrier mobilities to boost I_{on}. Both electron and hole mobilities can be improved by applying stress to induce appropriate strain in the channel, *e.g.,* tensile strain for n-channel MOSFETs and compressive strain for p-channel MOSFETs [9]. This phenomenon can be understood by considering induced changes in the complicated electronic band structures of Si [10]; the piezoresistance (PR) model provides a relatively easy approach to estimate the impact of channel stress components on carrier mobilities [11]. Optimization of the crystalline orientation can further increase I_{on}, *e.g.,* electron mobility is highest for a (100) Si channel surface while hole mobility is highest for a (110) Si channel surface [12].

In this dissertation, technologies for enhancing the performance of multiple-gate (MuG) FETs have been studied. First, the effects of process-induced parameter variations on the performance of DG MOSFETs have been investigated. Transistor performance sensitivity to variations in body thickness (T_{Si}), gate length (L_g), gate-oxide thickness (T_{ox}), and gate misalignment (MA) have been examined for n-channel symmetric-double-gate (SDG) and asymmetric-double-gate (ADG) MOSFETs with nominal L_g of 13nm and light body doping, via device simulation (ISE DESSIS).

Mo gate work function tuning by N^+ implantation has been reviewed and issues of this approach have been addressed. As an alternative approach to reduce Mo gate work function, HTFGA has been investigated and CMOS process integration issues have been discussed. A theory for Mo gate work function reduction has been also presented.

Finally, the physics of strained Si has been reviewed using electronic band structures, and the simple PR model has been also introduced to quantify mobility enhancement induced by strain. Then, three typical types of strains (substrate-induced, process-induced, and bending-induced strains) for enhancing MuGFET performance have been described. The impact of strained SOI (sSOI) substrate on MuGFET performance has been experimentally studied. The impact of a strained capping layer and tensile metal gate has been presented. Finally, the impact of biaxial convex bending on MuGFET performance has been studied. Mechanisms affecting carrier mobility in thin-body (fully depleted) MOSFET structures have been also elucidated by using the PR model.

6.2 Contributions

In this dissertation, technologies for enhancing MuGFET performance have been investigated. This section summarizes some of key contributions arising from this work. From the simulation study for the effect of process-induced parameter variations, it has been found that both the SDG and ADG designs are reasonably tolerant of process-induced variations, considering the capability of the modern device process technology.

HTFGA has been newly developed as an alternative technique for reducing the gate work function of Mo. In order to maintain the reduced Φ_M of Mo, a TiN capping layer has been applied, and the Φ_M was successfully retained. Therefore, the HTFGA together with a selective TiN capping layer in the n-channel regions has been proposed as a new work function tuning technique for Mo gates, suitable for advanced CMOS technologies employing thin-body MOSFETs.

The effects of three typical types of strains (*i.e.,* substrate-induced, process-induced, and bending-induced strains) on the performance of CMOS MuGFETs withe {110}/<110> and {100}/<100> surface-orientation/current-direction have been investigated. It was found that an sSOI is suitable for performance enhancement of {100} CMOS MuGFETs, or {110} CMOS MuGFETs with selective strain relaxation in the PMOS regions.

The impact of a stressed capping layer on MuGFET performance has been studied. A tensile capping layer is expected to provide dramatic enhancement (>100%) in {100} electron mobility, while a compressive capping layer is expected to provide a modest amount (<25%) of {110} hole mobility enhancement. Therefore, dual stress capping layers with hybrid orientations are suggested to boost CMOS MuGFET performance.

It was also found that the combination of a highly tensile gate together with an sSOI substrate can boost {110} electron mobility to be above the {100} universal curve, while it degrades {110} hole mobility by 30%. Since {110} hole mobility is not affected by the tensile gate stress alone, the use of tensile gates together with an sSOI substrate can be effective to enhance {110} CMOS MuGFET performance if the sSOI can be selectively relaxed in the PMOS regions. This combination of two stress technologies also provides enhanced {100} electron and hole mobilities, and hence is attractive for {100} CMOS MuGFET technology.

Finally, biaxial convex wafer bending has been shown to improve {100} CMOS MuGFET performance with a relatively low level (~0.1%) of strain, post-fabrication. In addition, the performance enhancement was largely retained with gate-length scaling, making package strain potentially attractive for enhancing MuGFET-based CMOS performance at low cost.

6.3 Suggestions for future work

HTFGA together with a selective TiN capping layer in the n-channel regions has been proposed as a new work function tuning technique of Mo gate suitable for advanced CMOS technologies employing thin-body MOSFETs, based on C-V measurements of MOS capacitors fabricated. Thus, the integration of this approach for advanced transistor structures, especially with high-k gate dielectrics, needs to be demonstrated. High-k dielectric may affect the effective work function of Mo due to a different dielectric screening effect from conventional SiO_2 gate dielectric [13]. Studying other Φ_M tuning techniques based on controlling the amount of nitrogen in the Mo gate will be also

interesting. For example, MoN_x film can be directly deposited by adding N_2 gas during sputtering process of Mo target with inert gas such as Ar. Nitrogen concentration in MoN_x film can be controlled by changing the partial pressure of N_2, resulting in different Φ_M.

With a simple PR model based on the classic bulk-Si PR coefficients measured by Smith in 1950s [14], the performance (mobility) enhancement of MuGFETs induced by different type of strains have been consistently explained. However, this model could not predict the experimentally observed {100} hole mobility enhancements (always higher than prediction), suggestive of significant band splitting, resulting in suppressed inter-band scattering. In addition, it is assumed that the PR coefficients are independent of the vertical electric field (E_{eff}), which can not explain the E_{eff} dependence on mobility enhancement. However, the PR coefficients varies with E_{eff} [15], and they are also affected by impurity concentration and temperature [16]. Therefore, a new PR model including all these effects is needed to predict the strain-induced mobility enhancement more precisely. Further modifications in the PR model may be required based on the updated PR coefficients measured recently or newly.

The effects of mechanical wafer bending on the performance of MuGFETs have been also investigated for the first time. However, only convex wafer bending (biaxial tensile strain) has been applied, hence it will be worthwhile to apply other type of wafer bending-induced strains, such as biaxial compressive strain and/or uniaxial tensile/compressive strain, to acquire a complete set of experimental data for more robust PR modeling.

Finally, the reliability of strained-Si MuGFETs needs to be rigorously studied. Although strain induces considerable change in a fundamental property (*i.e.,* the lattice constant) of the materials used for fabrication of Si-CMOSFETs, not much attention has been given to reliability of strained-Si devices, especially for MuGFETs, and no severe reliability degradation has been reported yet [17-20]. Therefore, reliability study with different type of strains will be very useful to determine the most robust strained-Si MuGFET technology. It will be also worthwhile to investigate the combined effect of different stress technologies (more than two).

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