Novel Processes and Structures for Low Temperature Fabrication of Integrated Circuit Devices

by

Joanna T Lai

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Committee in charge:

Professor Tsu-Jae King Liu, Chair
Professor Nathan Cheung
Professor Costas Grigoropoulos

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Abstract

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Low temperature fabrication of integrated circuit (IC) devices is important for large-area electronics and 3-D integration with CMOS electronics. This work addresses novel processes and transistor structures for these applications.

Polycrystalline silicon thin film transistors (poly-Si TFTs) are the highest performing devices for flat panel displays such as active matrix liquid crystal displays. Though the poly-Si TFT market share in the flat panel display industry is growing, realizing system-on-panel (SOP) products with all electronic circuitry directly fabricated on the display substrate requires improved device uniformity and reliability.

Two new processes are investigated to improve the performance, uniformity and reliability of poly-Si TFTs. The first is an ultra-low-temperature ultraviolet (UV) oxidation process with a maximum substrate temperature of 150°C developed for fabrication of poly-Si TFTs on flexible substrates. The UV oxide interfacial layer with a gate oxide deposited by PECVD shows excellent gate oxide characteristics for poly-Si TFT technology. Next, a defect passivation technique by selenium ion implantation into the TFT channel is shown to successfully passivate defects and improve TFT reliability under hot carrier bias conditions.

An alternative TFT design is examined, the accumulation-mode TFT. The accumulation-mode TFT employs a moderately-doped channel ($\sim 10^{18}\text{cm}^{-3}$) of the same dopant type as the source and drain regions. Using a 2-dimensional device simulator, it is shown that this device can achieve good electrical characteristics, with thin gate oxide and silicon channel film thickness. Simulations for a single grain boundary in the TFT channel show that the accumulation-mode design is less sensitive to the grain boundary location as compared to a conventional enhancement-mode design.

A novel device, the poly-Si tunneling field effect transistor (TFET), is fabricated with a maximum process temperature of 600°C. The short channel TFETs exhibit enhanced on-state current mostly due to carrier multiplication by impact ionization, at a trade-off of high leakage currents. An optimal TFET device design is proposed to decrease the off-state current levels.

Several low-thermal-budget materials are investigated as candidate structural MEMS materials for 3-D integration with CMOS circuitry. The mechanical properties of four metals (Al, Ti, TiN and Ni) are extracted. Of the four, only Al exhibited a low average tensile stress suitable for MEMS applications, but it had large strain gradient. Poly-Si formed by aluminum-induced-crystallization (AIC) at a maximum temperature of 350°C showed improved mechanical properties (low compressive stress and moderate strain gradient). An additional excimer laser anneal (ELA) at low laser fluence of 100 $\frac{\text{mJ}}{\text{cm}^2}$ yields superior mechanical properties so that AIC poly-Si is suitable for integrated MEMS applications such as inertial sensors and hybrid relay/CMOS circuits.

Professor Tsu-Jae King Liu
Dissertation Committee Chair

Dedicated to my Mommy and Daddy.

Your encouragement, faith and love have helped me through this journey.

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Chapter 1

Introduction

1.1 Low-Thermal-Budget Device Fabrication for Large-Area Electronics and 3-D Integration with CMOS Electronics

Low-temperature fabrication of switching devices, such as thin film transistors and microelectromechanical (MEM) relays, is necessary for fabrication of large-area electronics, such as displays and RFID tags, fabricated on glass or plastic substrates, and for 3-dimensional (3-D) integration with complementary metal-oxide-semiconductor (CMOS) electronics for enhanced integrated circuit (IC) chip functionality. In display applications, the process thermal budget is limited by the low strain point temperature of large-area glass or plastic substrates. Table 1.1 shows the maximum process temperature and optical transmission of some display substrates commonly used for large-area electronics [1, 2].

3-D integration of switching devices over CMOS electronics can enhance system functionality, improve packing density and reduce off-chip interconnects for better system performance. Fabrication of any device over CMOS electronics has process thermal budget limitations to prevent severe degradation of the underlying CMOS circuitry. Depending on the material of the CMOS metal layers, the maximum process thermal budget can range from 450°C for a standard 0.25-μm foundry CMOS technology with aluminum

Table 1.1. Substrate materials for TFTs [1, 2].

Substrate Material	Maximum Process Temperature (°C)	Optical Transmission
Glass	550-600	$> 92\%$
PET (polyethylene terephthalate)	115-170	$\sim 80\%$
PES (polyethesulphone)	180-220	$< 80\%$
PAR (polyarylate)	180	$\sim 80\%$
PA (polycarbonate)	115-130	$\sim 80\%$

interconnects [3] to 850°C for a specialized CMOS technology with tungsten interconnects [4]. It is desirable to limit the post-CMOS process thermal budget so as to be compatible with a conventional foundry process. That way, the benefits of a low-cost, reliable, high-performance CMOS foundry process can be leveraged.

Polycrystalline silicon thin film transistors (poly-Si TFTs) presently offer the highest performance among low-thermal budget devices. However, challenges for poly-Si TFT technology include formation of high-quality gate dielectric interfaces, passivation of defects, low on-state current, and performance non-uniformity. In this work, processes and device structures are discussed to alleviate these device issues.

1.2 Active Matrix Liquid Crystal Display Technology

Active matrix liquid crystal displays (AMLCDs) utilize TFTs to control an array of light valves. An exploded view of a twisted nematic liquid crystal display is shown in Fig. 1.1. Light from a backlight goes through a polarizing film. The polarized light then travels through an active matrix backplane consisting of pixels arranged in rows and columns with a TFT to control the light transmission at each pixel. Each pixel TFT drives a pixel electrode, which forms a liquid crystal capacitor with a common counter electrode on the cover sheet. The liquid crystal material is sandwiched between the backplane and cover sheet. The electric field across the liquid crystal determines whether it changes the

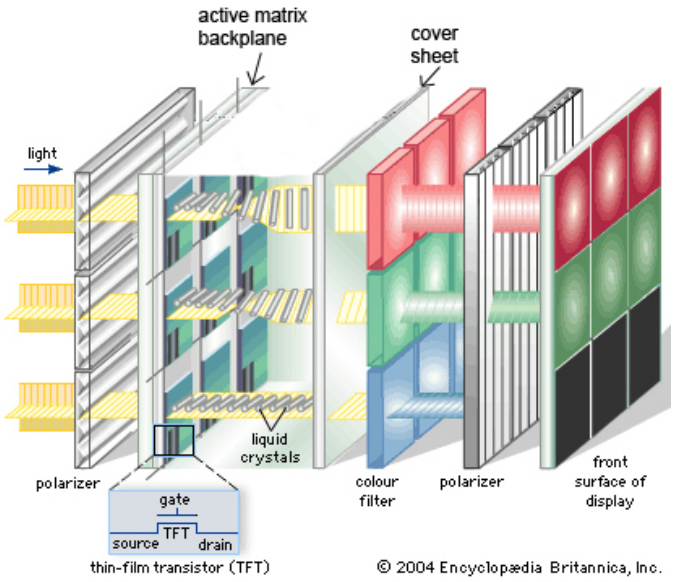

Figure 1.1. Schematic cross section of a liquid crystal display [5].

direction of light polarization. The light passes through the liquid crystal and is filtered to allow only red, green or blue light to reach the second polarizing film, which is typically oriented perpendicular to the first polarizing film.

A circuit schematic of the active matrix backplane is shown in Fig. 1.2. Here, the pixels are driven systematically row by row, by applying a voltage pulse to the row lines (which run horizontally across the backplane) to turn on the gates of the TFTs one row at a time. The row lines are often referred to as gate lines (denoted by "G" in Fig. 1.2). In this manner, the pixel electrodes are connected through the TFTs to the data lines (which run vertically across the backplane) and charged/discharged to the appropriate voltage for generating the desired image. Before each row is selected, the data voltages are applied to the column lines or data lines (denoted by "D" in Fig. 1.2) which are connected to the TFT drain electrodes. In the case of a twisted nematic liquid crystal display, if no electric field is applied, the liquid crystal molecules are twisted, rotating the direction of polarized light passing through them, so that light passes through the second polarizing film. If a voltage is applied, the liquid crystal molecules become aligned with the electric field, and do not rotate the direction of polarized light. In this case, the second polarizer blocks the

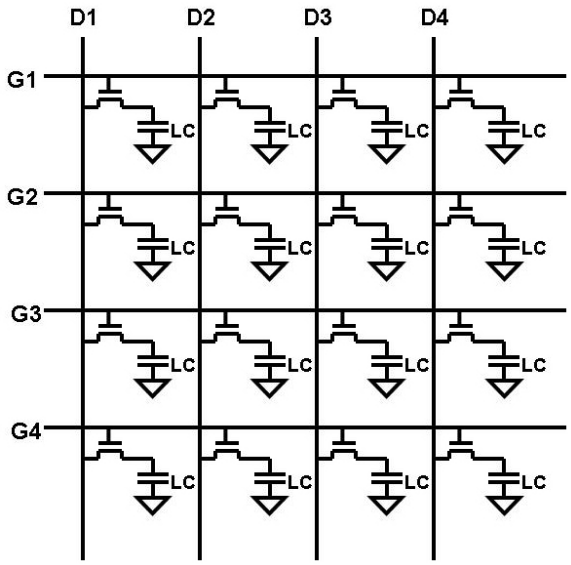

Figure 1.2. Circuit schematic of an active matrix backplane for a liquid crystal display.

light from passing through the front surface of the display [6]. From this description, it can be seen that the TFTs serve simply as pass-gates. Ideally, they should have moderately large on-state drive current, typically achieved with carrier mobility > 1 $\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ (to allow for the pixel electrodes to be charged/discharged with one row address time) and low off-state leakage (to maintain the pixel electrode voltage over one frame time).

1.2.1 Thin Film Transistor Technologies

Many TFT channel materials and structures have been explored for AMLCD technology. Hydrogenated amorphous Si (a-Si:H) is the most widely used for large-area displays such as high-definition LCD televisions. However, this technology is limited to n-type TFTs due to electron mobilities of ~ 3 to 5 $\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ and hole mobilities that are $\sim$100$\times$ lower [7].

Organic TFTs (oTFTs), on the other hand, have been explored as an alternative channel material for fabrication on low-cost, flexible substrates. Though oTFTs can be fabricated at ultra-low fabrication temperatures, the highest reported carrier mobilities are well below 10 $\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ for a pentacene channel material [8]. Organic TFTs are mostly p-type TFTs and complementary TFTs cannot be obtained using a single channel material.

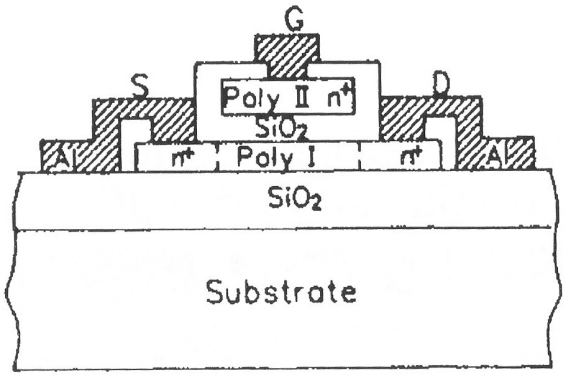

Figure 1.3. Typical top gate, coplanar poly-Si TFT structure [12].

Poly-Si has the highest reported electron and hole carrier mobilities of all TFT materials. Using a conventional pulsed excimer laser crystallization technique to form the poly-Si channel material, electron and hole mobilities of at least 180 $\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ and 120 $\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$, respectively, can be achieved [9, 10]. Both n-type and p-type poly-Si TFTs can be fabricated to implement low-power CMOS display driver circuitry directly on the display panel. By integrating the display driver circuitry directly on the panel, off-panel connections to driver IC chips can be minimized to reduce form factor. The uniformity and reliability of poly-Si TFTs need to be improved in order to enable system-on-panel [11].

A top-gated, coplanar poly-Si TFT structure with self-aligned source and drain regions is usually employed (see Fig. 1.3). Typically, amorphous Si (a-Si) is deposited and crystallized to form the polycrystalline active layer. The active region is patterned and etched, followed by gate dielectric and gate layer deposition (either highly-doped poly-Si or metal). Next, the gate is patterned and etched. The dopants are then implanted by ion shower or ion implantation, forming self-aligned source and drain regions. Dopant activation by furnace annealing or laser annealing is typically performed afterwards. The device is completed by an silicon dioxide layer deposition, contact hole patterning, and lastly metallization deposition and patterning [12].

1.2.2 Challenges for Poly-Si Thin Film Transistor Technology

Poly-Si is a heterogeneous material that consists of small crystalline grains that are randomly distributed throughout the film. The crystalline sizes range from tens of nanometres to several micrometres, depending on deposition and crystallization process conditions. Between the poly-Si grains exist grain boundaries, which are rich in Si dangling bonds. These dangling bonds create carrier trap sites that introduce localized energy states in the Si bandgap. The density and location of the dangling bond defects have significant impact on the electrical properties of the resulting poly-Si films.

Three crystallization methods are typically used in the fabrication of poly-Si TFTs: solid phase crystallization (SPC), excimer laser annealing (ELA) and metal-induced crystallization (MIC) or metal-induced lateral crystallization (MILC). In an SPC process, an a-Si film is furnace annealed at temperatures ranging from 550 to 600°C for up to 24 hours. The resulting film has moderate grain sizes with electron mobilities of $\sim$40 $\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ [13]. Its process thermal budget is the highest of the three crystallization techniques.

In the MIC process, a metal deposited on top of an a-Si film decreases the crystallization temperature [14]. A thin metal film, such as nickel (Ni), is deposited on the a-Si film and the film stack is annealed. The metal promotes crystallization which occurs at lower temperatures and shorter anneal times compared to SPC. Metal traces in the channel region of a poly-Si TFT can be reduced by selectively depositing Ni only in the TFT source and drain regions and performing MILC. Longer anneals (*e.g.* 500°C, 5 hours) allow the Ni to move laterally across the channel, creating poly-Si films with large grain sizes and lower metal contaminants in the channel region. High performance poly-Si TFTs have been fabricated with reported electron mobilites of 120 $\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$, but at the trade-off of high leakage currents [15].

The most common crystallization method is pulsed ELA in which the a-Si film is exposed to an excimer laser beam of wavelength λ=193, 248 or 308 nm. The light is absorbed well

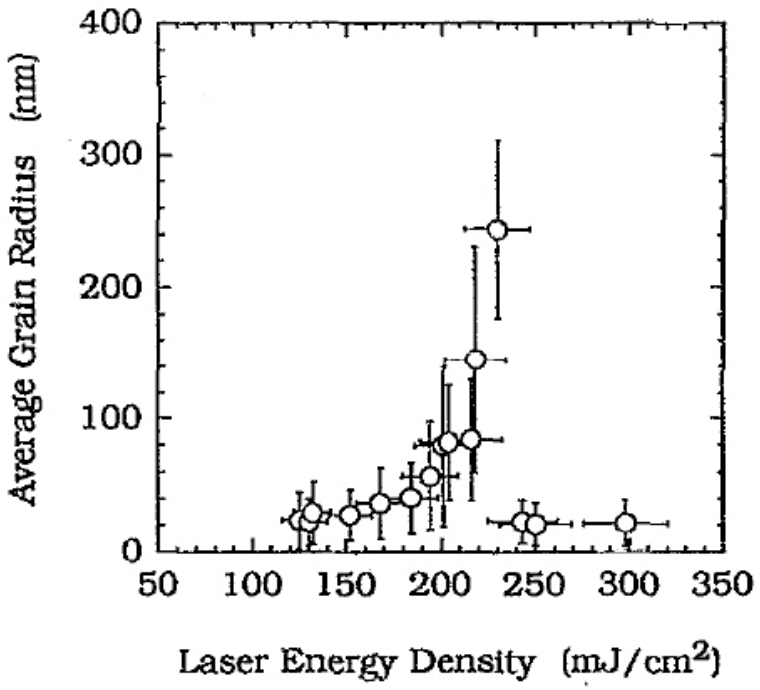

Figure 1.4. Dependence of the average Si grain size as a function of pulsed excimer laser fluence, from [16].

in Si at these wavelengths, causing the Si film to melt and resolidify in a polycrystalline state.

As shown in Fig. 1.4, the average grain radius size in a 100-nm thick Si film has a strong dependence on the laser energy density. At low laser energy densities, the film grain size slightly increases with increasing laser energy density. However, at some point, small increases in energy density result in much larger grain size due to the super lateral growth (SLG) phenomenon. In the SLG regime, the Si film is nearly completely melted. Most of the Si film melts upon the laser pulse, leaving isolated unmelted Si islands to nucleate grain growth, allowing considerable lateral grain growth. For laser fluences above the SLG regime, the Si film fully melts. Many nucleation sites are created upon super cooling, which results in poly-Si films with fine grains. The poly-Si TFTs with the best performance can be achieved when crystallized in the SLG regime [16]; however ELA has a narrow process window. Slight deviations in laser fluence and Si film thickness vary the average poly-Si grain size, contributing to device nonuniformity [16, 17]. Further improvements in carrier

mobilities can be achieved by advanced laser crystallization techniques such as solid lateral solidification (SLS) to achieve larger Si grain sizes [18, 19].

Further TFT performance improvements can be made by defect passivation. Conventionally, TFTs are passivated by atomic hydrogen (H) from hydrogen plasma. At moderate temperatures (*e.g.* 350°C to 425°C), the H diffuses through the Si film and bonds with Si at the dangling bond defect sites. Defect passivation is easily integrated into the poly-Si TFT process after source/drain dopant activation and improves the performance and device uniformity across the large substrate [20]. However, weak Si-H bonds can break under electrical stress, which affects the device reliability [21].

1.3 Three-Dimensional Integrated Circuit Technology

Three-dimensional integration of active devices on top of CMOS electronics has been explored as the performance of devices has improved with scaling, so that interconnect RC delay can limit system performance. A schematic cross-section is shown in Fig. 1.5. Vertical integration can improve the device packing density, decrease interconnect resistance and capacitance (by using short vertical interconnects instead of long horizontal ones), or enhance functionality [22].

Many devices have been explored for vertical integration, such as poly-Si TFTs for high density SRAM cells [23, 24], MEMS inertial sensors [4], and transistors for 3-D nonvolatile memory [25] and logic applications [26, 27]. From Saraswat *et al.*'s analysis, variation in poly-Si TFTs due to grain boundary defects are too large to fulfill the requirements for 3-D ICs [22]. Of all the potential low-thermal-budget devices, microelectromechanical (MEM) relays have ideal switching behaviour, such as almost zero off-state current and steep subthreshold slope. Various relay designs for logic and memory applications have been proposed by several groups [28, 29, 30, 31, 32] which show ideal switching characteristics. However, it is necessary to form a high-quality structural material with excellent mechanical properties for integration on top of CMOS electronics.

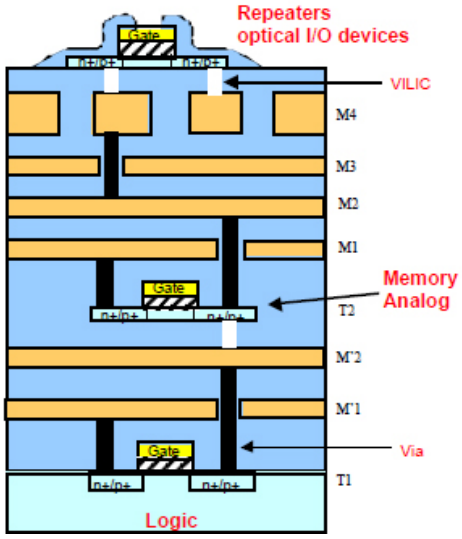

Figure 1.5. Schematic cross-section of a 3-D integrated circuit with low-temperature transistors fabricated over CMOS electronics for memory applications, from [22].

1.3.1 Low-Thermal-Budget Structural Materials for MEMS

Silicon has excellent mechanical properties for MEMS devices. However, the process of depositing poly-Si by low pressure chemical vapor deposition (LPCVD) requires temperatures too high for post-CMOS integration. The deposition of a-Si is possible at low temperatures by sputtering or plasma enhanced chemical vapor deposition (PECVD) and a low-thermal-budget crystallization technique can be employed if it yields acceptable mechanical properties.

To date, poly-$Si_{1-x}Ge_x$, where $x < 0.6$, is a promising material for MEMS integration with CMOS technology. Poly-$Si_{1-x}Ge_x$ can be deposited at temperatures down to 410°C. However, lower deposition temperatures lead to worse mechanical properties such as high strain gradient and high compressive residual stress [33]. Thus, there is a need to develop a suitable structural material that can be formed at low process temperatures with better mechanical properties.

1.4 Thesis Organization

This thesis is first motivates low-thermal-budget device structures and processes. Improvements that can be made to poly-Si TFT technology are then described. Then the mechanical properties of low-thermal-budget materials is investigated for MEMS integration with CMOS electronics.

In chapter 2, an ultra-low-temperature gate dielectric formation process is investigated for compatibility with flexible plastic substrates, with maximum substrate temperature $\leq$ 150°C. At such low temperatures, conventional gate oxide formation processes result in a high density of interface traps and oxide charge. A UV-enhanced oxidation process is introduced to form an ultrathin high-quality gate dielectric interfacial layer between the semiconductor and the gate dielectric.

In chapter 3, ion implantation of selenium (Se) into the a-Si channel layer prior to ELA is investigated as a means for defect passivation. The Se is shown to successfully passivate defects in the poly-Si film and improve the performance of the TFT. In comparison with a conventional hydrogen plasma passivation treatment, Se passivation yields improvement in TFT reliability.

Further improvements to minimize the TFT performance sensitivity to grain boundaries is examined in chapter 4, where an alternative TFT design is proposed. The accumulation-mode TFT employs higher channel doping which is the same type as the source and drain regions to decrease the effects of grain boundary defects. Two-dimensional device simulations are performed to optimize and assess the advantages of the design.

In chapter 5, a poly-Si tunneling field effect transistor (TFET) structure is fabricated to explore the possibility of enhancing TFET on-state performance. The presence of a large lateral electric field at the drain junction allows band-to-band tunneling and trap-assisted tunneling components. Large on-state current can be achieved as compared to a control TFT.

In chapter 6, the mechanical properties of low-thermal-budget materials are investigated

for post-CMOS MEMS integration. Both sputtered metals and poly-Si crystallized at low-temperatures are examined and compared to state-of-the-art polycrystalline silicon-germanium technology.

Lastly, chapter 7 summarizes the contributions of this research and proposes future work that builds upon this work.

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Chapter 2

Ultra-Low-Temperature Gate Oxide Interface Formation

2.1 Introduction

High-performance polycrystalline silicon thin film transistors (poly-Si TFTs) fabricated on plastic substrates have been demonstrated by several groups [1, 2, 3, 4]. Due to the low strain point of plastic substrates, the maximum substrate process temperature is limited to $\sim 150°C$. At ultra-low deposition temperatures, it is difficult to obtain a dense silicon dioxide (SiO_2) gate dielectric with a high-quality Si/SiO_2 interface. Since thermal oxidation is incompatible with low-temperature processing, typical methods for poly-Si TFT oxide formation have been plasma-enhanced chemical vapor deposition (PECVD) [1, 2] and physical vapor deposition (PVD) by reactive sputtering [5]. High-density-plasma chemical vapor deposition processes, including electron cyclotron resonance chemical vapor deposition (ECR-CVD) [3] and inductively-coupled plasma chemical vapor deposition (ICP-CVD) [4], have achieved improved gate oxide characteristics.

Gate oxides can be deposited by PECVD at low temperatures compatible with plastic substrates; however, common parallel-plate PECVD systems cause damage at the Si/SiO_2

interface from ion bombardment. Attempts to decrease the damage of PECVD SiO_2 films have succeeded by decreasing the deposition rate and increasing the inert gas flow rates, but the resultant films still require a subsequent anneal to achieve interface characteristics comparable to that seen for ECR-CVD and ICP-CVD oxides [6]. Alternatively, SiO_2 films can be formed by reactive sputtering at room temperature [7, 8, 9]. In this process, a solid Si target is exposed to an oxygen (O_2) and argon (Ar) environment. The Si target reacts with oxygen gas and an SiO_2 film can be deposited. One benefit of a PVD process over a PECVD process is that sputtered films are free of hydrogen, which provide for improved device stability [10]. However, reactively sputtered films also exhibit damage at the interface due to high-energy ion bombardment [5]. ECR-CVD and ICP-CVD have an advantage due to the reduction in ion bombardment during deposition. The resulting films exhibit low interface defect density, higher density, and a smooth Si/SiO_2 interface [11, 12, 13]. However, high-density-plasma systems cannot be scaled to accomodate large-area substrates, due to the difficulty of creating a large uniform plasma sheath, for manufacturing large displays [6, 14].

Ultraviolet (UV)-enhanced oxidation (also known as photo-oxidation) has been shown to form SiO_2 films at ultra-low temperatures. Nakata *et al.* and Zhang *et al.* demonstrated that low interface state density in the range of 3×10^{10} - $4 \times 10^{10} \frac{cm^2}{eV}$ can be achieved with this process [15, 16]. In this study, the effects of UV oxidation pressure and temperature on the interface properties of the resulting SiO_2 films are investigated. Then, metal-oxide semiconductor (MOS) capacitors are fabricated with and without an optimized interfacial UV oxide to assess the benefits of a UV oxide/PECVD oxide or UV oxide/PVD oxide for the TFT gate insulator.

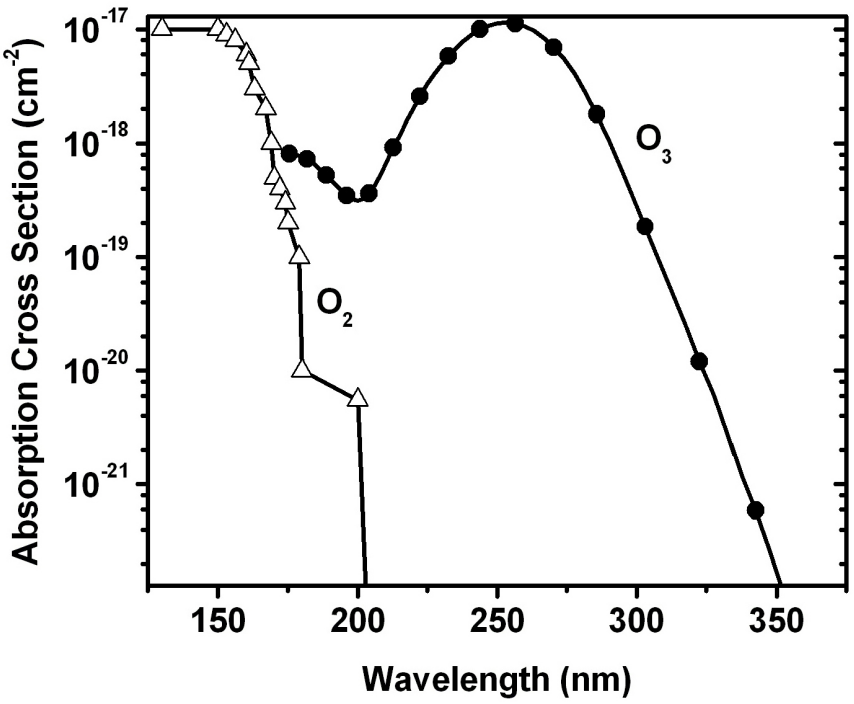

Figure 2.1. Absorption of oxygen (O_2) and ozone (O_3) in silicon for various wavelengths of light, from [20] and [21].

2.2 Oxide Growth by UV-Enhanced Oxidation

The UV light source used in the process is a Xenon (Xe) excimer light source (λ=172 nm). When oxygen flows into the chamber, the Xe excimer light dissociates the gas, creating atomic oxygen radicals. The following reaction takes place [17]:

$$O_2 + h\nu(172\text{ nm}) \longrightarrow O(^3P) + O(^1D)$$
$$Si + 2O(^1D) \longrightarrow SiO_2$$

The $O(^1D)$ radicals are highly reactive and promote oxygen absorption in Si without requiring a high-temperature process. As shown in Fig. 2.1, the absorption of O_2 at 172 nm exceeds that of oxygen or ozone (O_3) at 185 nm, which has been previously studied [18, 19].

An initial assessment of UV oxidation was conducted using p-type Si(100) substrates with resistivity in the range 10-30 Ωcm. Prior to the UV oxidation, the Si wafers were

cleaned in a piranha (H_2SO_4:H_2O_2) bath at 120°C for 10 minutes. Then the wafers were cleaned in a 25:1 HF solution to remove native oxide. It is important to note that the HF sink was cleaned in RCA-1 solution (5:1:1 DI water:H_2O_2:NH_4OH) prior to the HF clean to remove any organic contaminants from the bath. The RCA-1 clean reduces the interface trap density by an order of magnitude. After the HF clean, the wafers are immediately placed under vacuum to prevent native oxide growth. The wafers are exposed to the UV light source with λ=172 nm in a controlled oxygen environment under various pressures and temperatures. The films for different UV oxidation conditions are then characterized to determine the optimal conditions for yielding good interface properties.

2.3 UV Oxidation Process Optimization

2.3.1 Interface Characterization by Surface Charge Analysis

The interface properties of the UV oxide films were characterized by SemiTest Inc.'s Surface Charge Analyzer (SCA-2500). This non-destructive characterization technique brings an electrode covered with a 10-μm thick Mylar film in contact with the dielectric. As the electrode comes in contact with the sample, modulated green light (λ=510 nm) is applied and the alternating current (AC) surface photo-voltage, which is proportional to the Si substrate depletion width (W_{DEP}), is measured. The probe bias (V_{BIAS}) is applied, to sweep the Si surface from inversion to depletion to accumulation conditions. Leakage current is negligible, and the induced charge ($Q_{IND} = C_{BIAS} \times V_{PROBE}$) is measured against W_{DEP}, similarly to a *C-V* measurement. From the W_{DEP} versus Q_{IND} plot, the charge and interface trap densities can be extracted. Important properties include the flatband charge (Q_F), which corresponds to fixed oxide interface charge, assuming the mobile and fixed bulk charges are negligible, and interface trap density (D_{IT}). The resolution limit for these parameters in the SCA is $1 \times 10^{10}\text{cm}^{-2}$. Significant tunneling can occur in ultrathin dielectrics, so D_{IT} is overestimated since the surface states at the gate/gate oxide interface

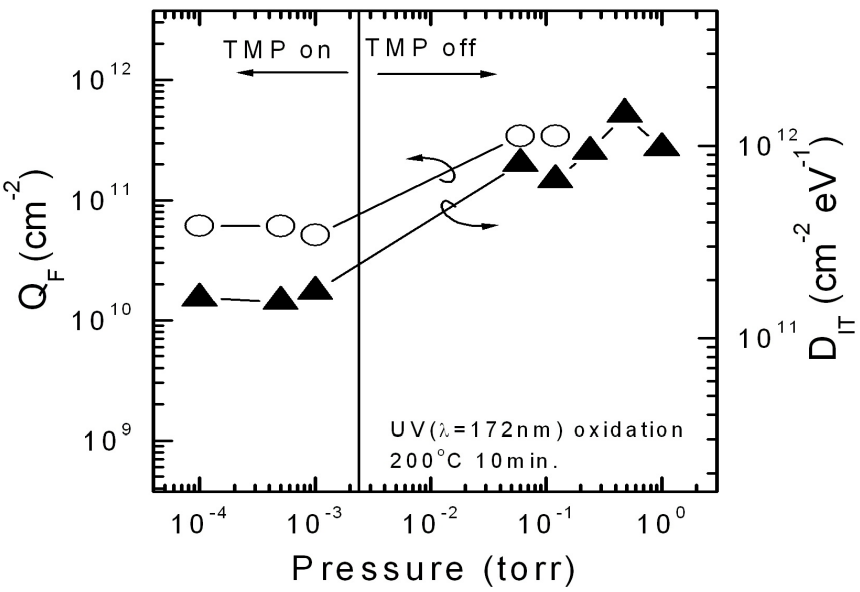

Figure 2.2. Interface trap density and fixed oxide charge of UV-enhanced oxide films for various oxidation process pressures [24].

are not passivated by the gate electrode in the SCA as they would be in MOS capacitors, and so they contribute to the D_{IT} term [22, 23].

2.3.2 Pressure and Temperature Dependence of Interface Properties

The optimization of pressure and temperature is described herein for UV oxide. The oxidation was done under vacuum with process pressure down to 5×10^{-2} T. Lower pressure is achieved by turning on a turbo-molecular-pump (TMP) that pumps the process chamber pressure down to below 1 mT. All samples were oxidized at 200°C for 10 minutes. Better interface quality was seen at lower pressures with the TMP on, as shown in Fig. 2.2 [24].

The wafer chuck temperature was varied between 25°C and 500°C, at a low process pressure of 0.5 mT, for 10 minutes. The best quality interface (lowest D_{IT} and Q_F values) is achieved at a chuck temperature of 150°C, as shown in Fig. 2.3.

Nakata *et al.* [25] show the UV oxidation thickness with time in Fig. 2.4 for a constant temperature of 300°C and O_2 pressure of 0.5 T. The film growth follows the Deal-Grove

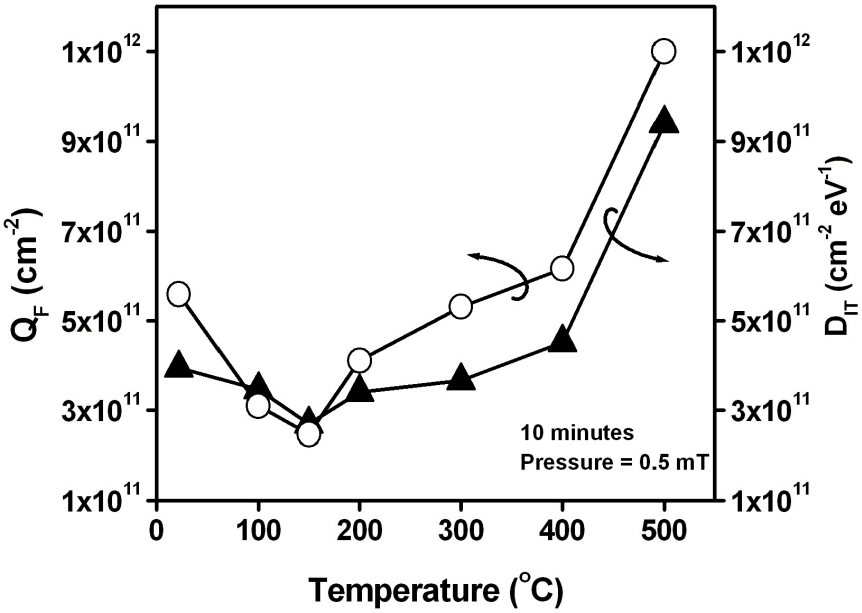

Figure 2.3. Interface trap density and fixed oxide charge in UV-enhanced oxide films for various oxidation process temperatures.

model, indicating that the oxidation occurs at the Si/SiO_2 interface. (The oxide thickness has a square root dependence on oxidation time). At a pressure of 0.5 mT, there is less reactive gas present, so the growth reaction rate is slower. For a 10 minute exposure to oxygen, and the thickness of the resulting SiO_2 film is $\sim$ 1-nm.

2.4 Metal-Oxide-Semiconductor Capacitor Study

Capacitors were fabricated using an ultra-low-temperature process to assess the benefits of a UV-enhanced oxide film as an interfacial layer for poly-Si TFT gate insulator applications. Four types of metal-oxide-semiconductor (MOS) capacitors were fabricated with a maximum thermal budget of 150°C. One set of control samples was fabricated with a 40-nm thick oxide deposited by PECVD. Another set of control samples was fabricated with a 40-nm thick oxide deposited by a reactive sputtering process. Lastly, two sets of samples were fabricated, one with a film stack of a thin UV oxide interfacial layer and PECVD oxide, the other with a film stack of a thin UV oxide interfacial layer and a reactive sputtered oxide.

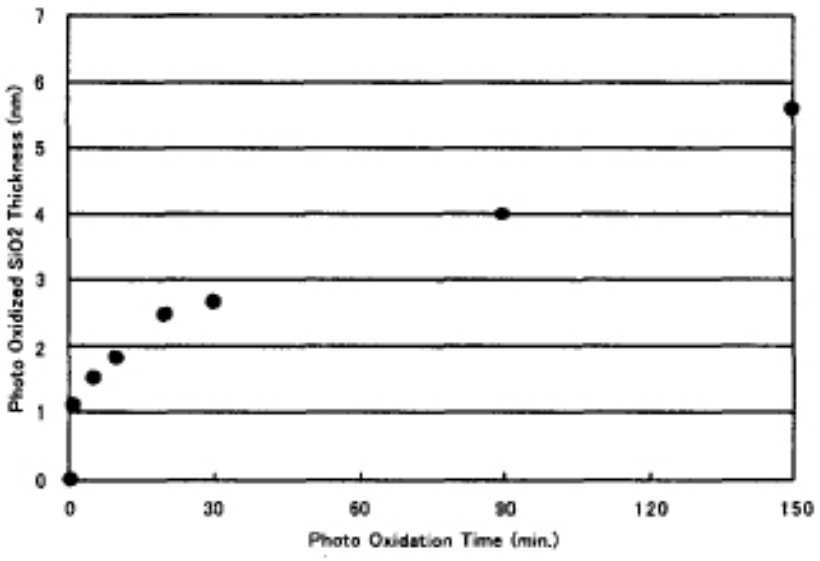

Figure 2.4. UV-enhanced oxide growth follows the Deal-Grove model for oxidation at constant temperature and pressure, from [25].

2.4.1 Ultra-Low-Temperature Gate Oxide by PECVD and PVD Processes

An ultra-low-temperature SiO_2 reactive sputtering process is established in a Novellus M2i direct current (DC) magnetron sputtering tool. In this process, a SiO_2 film is formed with a high purity Si target in the presence of a reactive gas (O_2) and inert gas (Ar) gas mixture. In a reactive sputtering process, the mole fraction of O_2 in the O_2-Ar gas mixture determines the oxidation rate of the Si target and the sputtering rate of the target material. As shown by Ohwaki *et al.* [7], if the mole fraction of O_2 in the O_2-Ar gas mixture is greater than 6%, the oxidation rate overcomes the sputtering rate of the target, so that SiO_x is sputtered instead of Si. Increasing the O_2 mole fraction above 10% ensures that the films are stoichiometric SiO_2, which is desirable. Lower O_2 mole fractions result in sputtered films with composition of SiO_x, where $1.4 \leq x \leq 1.8$. To ensure that the target is fully oxidized before sputtering, the partial pressures of Ar and O_2 are both 3 mT (corresponding to 50% O_2 mole fraction) [5]. Damage from high energy ion bombardment is minimized by inserting a plasma charge trap (PCT) between the Si target and the wafer, shown in Fig. 2.5. The PCT is a stainless steel collimator made from a 1.66-mm thick stainless steel disc

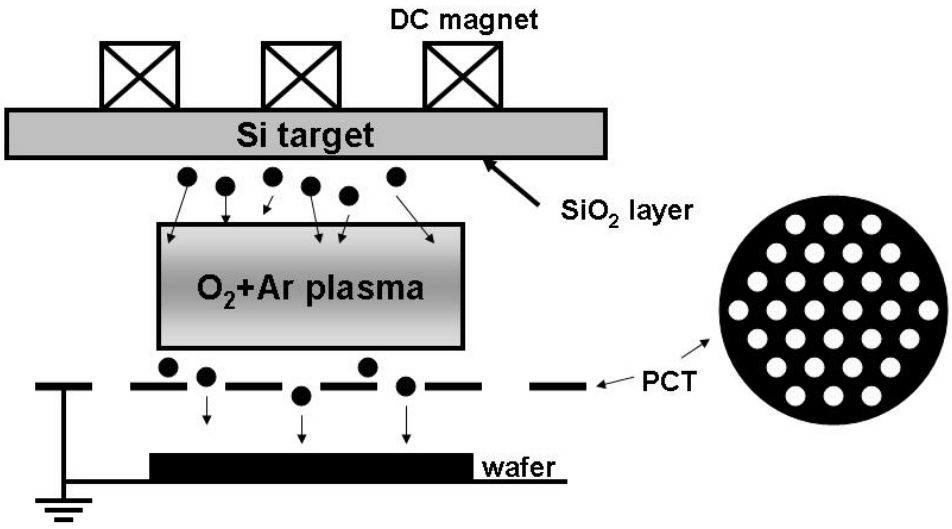

Figure 2.5. Diagram of sputtering chamber with a PCT inserted between the Si target and wafer. The PCT collects high-energy ions, preventing damage to the wafer surface. This diagram is adapted from [26, 27].

with perforated 3.32-mm diameter holes, resulting in 40.3% of the aperture ratio. The PCT is biased electrically at ground to collect high energy Ar^+ ions and electrons, preventing them from reaching the wafer surface [26, 27]. With the PCT, the sputtering power must be kept low to prevent arcing. A 40-nm thick SiO_2 film is deposited at 150°C at 360 W, which is the optimal power [5]. Between each SiO_2 deposition, a Si deposition is performed to ensure that the PCT is conductive before the next SiO_2 deposition.

An SiO_2 PECVD process is established in a Oxford plasmalab 80plus system. PECVD films can be deposited at lower temperatures compared to low pressure chemical vapor deposition (LPCVD) since a plasma source provides additional energy to increase the gas dissociation rate and promote chemical reaction at the wafer surface. In the plasma, the reactant gases easily dissociate and form ionized molecules and free radicals which are very reactive. However, films deposited by PECVD can result in nonstoichiometric films with byproducts, such as hydrogen, oxygen or nitrogen, incorporated in these films. The byproducts can adversely affect the film stability by outgassing during further processing or electrical testing [28]. A typical parallel-plate PECVD chamber is shown in Fig. 2.6.

An SiO_2 film is deposited with RF power of 25 W and pressure of 0.9 T at 150°C. The

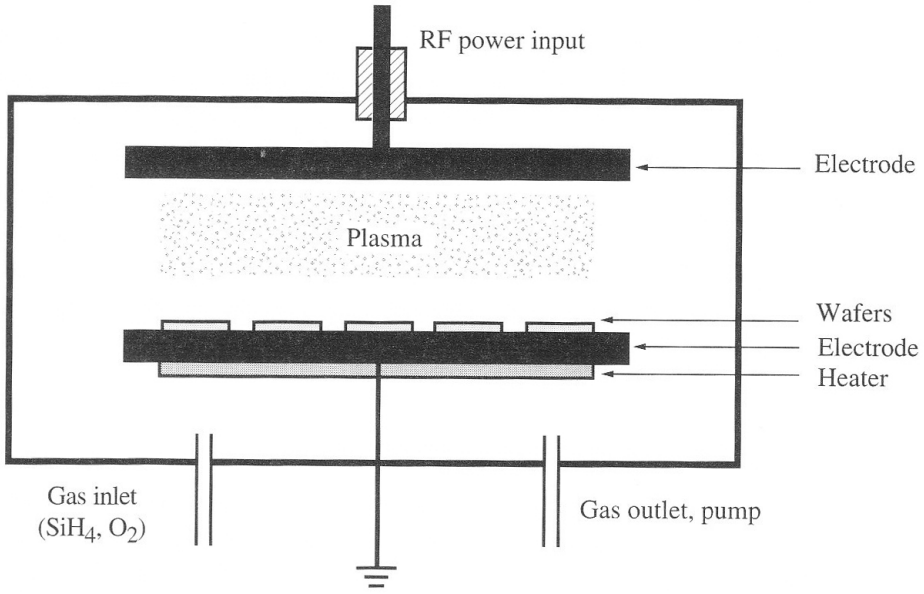

Figure 2.6. Configuration of a typical parallel plate PECVD chamber [28].

gases used are silane (SiH_4), nitrous oxide (N_2O) and argon (Ar), where SiH_4 and N_2O react to form the SiO_2 film. During deposition, 100 sccm of SiH_4, 800 sccm of N_2O and 100 sccm of Ar flow into the chamber.

2.4.2 MOS Capacitor Fabrication

Metal-oxide-semiconductor (MOS) capacitors were fabricated for four different gate oxide stacks on p-type Si(100) substrates with resistivity between 10 and 30 Ωcm. After piranha and HF cleaning, two wafers were subjected to the optimized UV oxide treatment at a temperature and pressure of 150°C and 0.5 mT for 10 minutes. Without breaking vacuum, a 40-nm thick SiO_2 film was deposited on one of the wafers at 150°C by reactive sputtering. The other wafer with UV oxide was subjected to a 40-nm thick PECVD oxide deposition at 150°C. Two control wafers were processed with only the PECVD oxide or PVD oxide (*i.e.,* with no UV oxide interfacial layer). A 200-nm thick aluminum (Al) film was then evaporated onto all four wafers and patterned to form capacitor electrodes with

Table 2.1. Parameters extracted from HFCV and IV measurements for the four oxides.

	Q_F (cm^{-2})	D_{IT} ($cm^{-2}eV^{-1}$)	E_{BD} ($\frac{MV}{cm}$)
PVD SiO2	4.39 $\times 10^{12}$	4.47 $\times 10^{10}$	7.53
UV/PVD SiO2	1.99 $\times 10^{12}$	3.72 $\times 10^{10}$	9.40
PECVD SiO2	2.34 $\times 10^{12}$	2.96 $\times 10^{10}$	11.38
UV/PECVD SiO2	1.98 $\times 10^{12}$	7.47 $\times 10^{9}$	11.81

W=L of 50-μm, 100-μm and 200-μm. A wet Al etchant was used to minimize etch damage to the gate dielectric.

2.4.3 Experimental Results

Degradation of a gate dielectric occurs in the presence of current or high electric field. The gate oxide eventually breaks down under sufficiently high electric field or integrated current. Many degradation mechanisms have been proposed, including trap creation [29], hole-induced degradation [30] and electron trapping [31]. Though it is not clear which mechanism is responsible for oxide breakdown, a high number of defects or trap states in the bulk of the oxide and at the interface worsens the reliability [32].

The dielectric strength of the various low-temperature gate insulators were measured by time-zero dielectric breakdown (TZDB) tests [33]. The substrate is grounded and the gate voltage on 100-μm $\times$ 100-μm capacitor gates is ramped up. The current density is monitored while increasing voltage (hence electric field) across the dielectric, shown in Fig. 2.7. The steep rise in current density indicates a hard breakdown of the gate dielectric. The current compliance is set to 100 nA (or current density of $10^{-3}\frac{A}{cm^2}$). The electric field at breakdown (E_{BD}) is overestimated since the substrate is biased from the back side and the series resistance from the lightly doped substrate is not accounted for in the calculation. The samples with the UV interfacial oxide have larger breakdown fields compared to the corresponding control samples. The E_{BD} values are compared in Table 2.1, along with other key parameters characterizing the four oxides.

A high frequency capacitance-voltage (HFCV) measurement is performed on the 200-

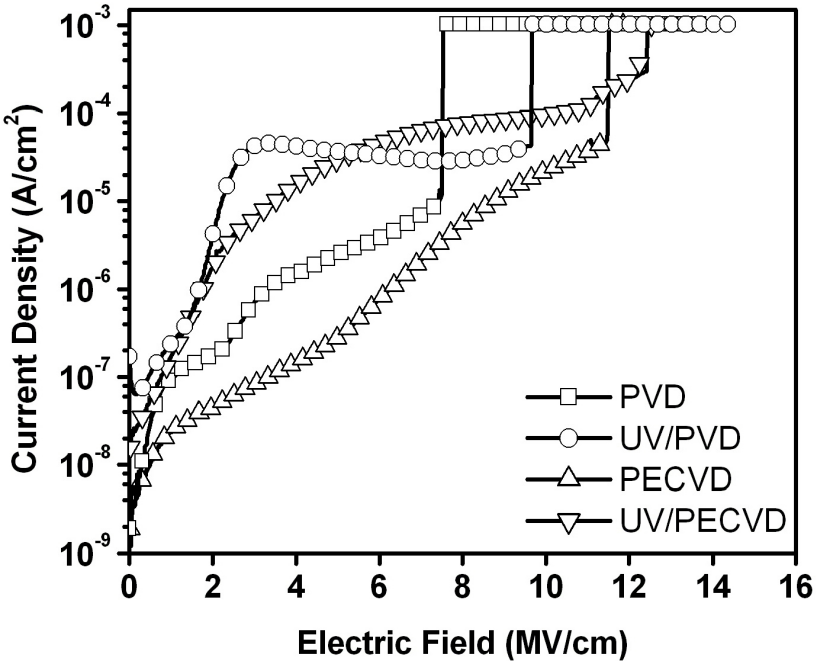

Figure 2.7. Electric field breakdown versus current density for four gate dielectrics.

μm $\times$ 200-μm capacitors for the four oxides at 100 kHz with 25 mV oscillations. Fig. 2.8 shows the measured capacitance, normalized to $C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}$, versus the gate voltage. All samples show considerably negative flat band voltage (V_{FB}) shift indicative of fixed charge in the oxide. The UV/PVD and UV/PECVD oxides have less fixed charge compared to the corresponding control samples.

The interface trap density is extracted from the HFCV measurement in the region where the surface is in depletion. The Berkeley Quantum Mechanical CV (QMCV) simulator was used to obtain the expected theoretical capacitance [34] for comparison against the measured capacitance. D_{IT} is extracted following the methodology in [35]. Because the capacitors are measured at 100 kHz, the D_{IT} numbers extracted underestimate the trap density since a fraction of interface traps do not respond at this frequency.

The two samples with PECVD oxide have lower interface trap density, as expected. This confirms that the reactive sputtering process causes damage at the Si/SiO_2 interface due to ion bombardment. The minimum midgap D_{IT} is tabulated in Table 2.1. Slight

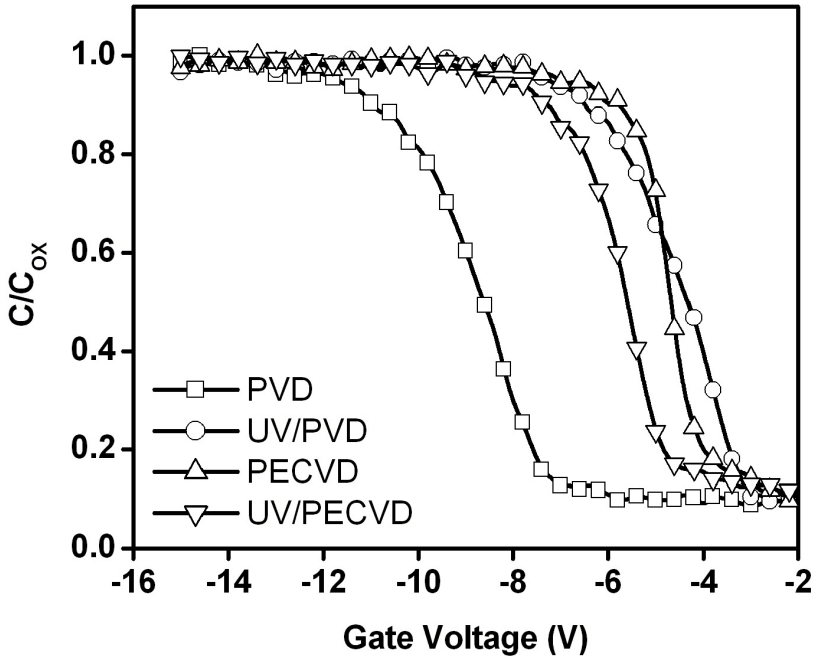

Figure 2.8. Normalized gate capacitance versus gate voltage for four ultra-low-temperature gate dielectric samples.

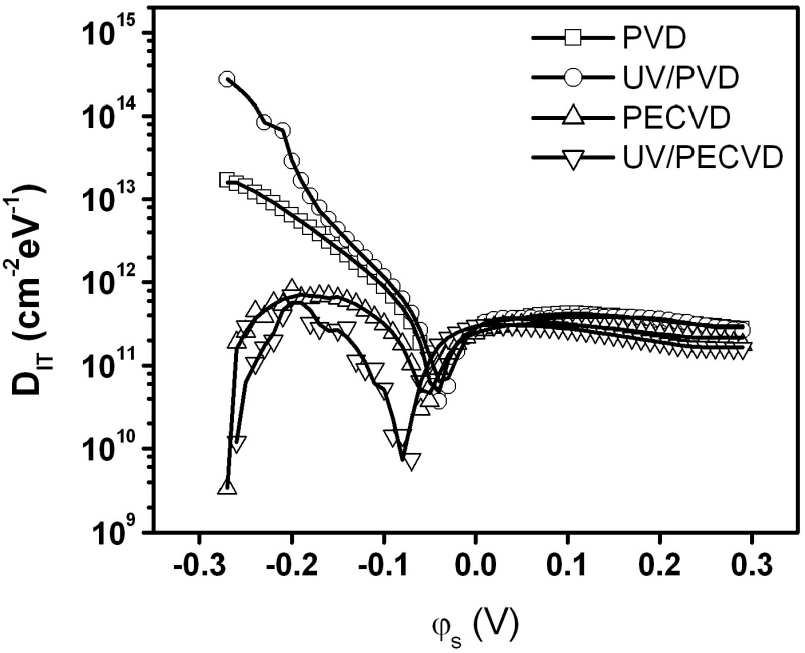

Figure 2.9. Interface trap density versus Si surface potential for four oxide samples. The surface potential is measured relative to the flat band potential (φ_s=0 at flat band).

improvement in D_{IT} is seen for the samples that have the UV oxide interface compared to the corresponding control samples.

2.5 Summary

A UV-enhanced oxidation process is established to form a thin interfacial oxide layer for ulta-low-temperature deposited dielectrics. For process pressures below 1 mT, the interface properties improve but the oxidation rate is greatly decreased. The optimal temperature for this process is found to be 150°C. The best UV oxide sample gives interface trap density and fixed charge density of $D_{IT} = 2.69 \times 10^{11} cm^{-2} eV^{-1}$ and $Q_F = 2.47 \times 10^{11} cm^{-2}$, respectively. These values are overestimated (*i.e.* pessimistic) because they include surface states from the top surface of the UV oxide.

MOS capacitors were fabricated with and without the UV oxide interfacial layer for PECVD and reactively sputtered bulk oxide films. The reactively sputtered films cause damage to the Si/SiO_2 interface due to ion bombardment, so the measured D_{IT} are high. The oxide also breaks down at lower electric fields, indicative of higher oxide trap density. On the other hand, the PECVD oxides have fewer traps and break down at higher electric fields. The interface charge is the lowest for PECVD oxide with UV oxide interfacial layer, slightly better than for the control PECVD oxide. The UV oxide layer lowers fixed interface charge for both PVD and PECVD oxides.

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Chapter 3

Defect Passivation by Selenium Ion Implantation for Poly-Si Thin Film Transistors

3.1 Introduction

Formation of high quality polycrystalline silicon (poly-Si) films with large grain sizes and minimal defect density is important to achieve uniform and reliable thin film transistor (TFT) performance. Defects in poly-Si come from dangling bonds at the grain boundaries and strained bonds in poly-Si grains, which adversely affect the TFT performance by introducing charge trap states in the Si bandgap. An approximate distribution of trap states within the bandgap for poly-Si films is shown in Fig. 3.1, by Jacunski *et al* [1]. The different types of traps (either tail states near the conduction and valence bands or midgap states near the middle of the bandgap) affect different TFT performance parameters. The threshold voltage (V_T) and subthreshold slope (S) are strongly influenced by the density of midgap states; whereas tail states influence the leakage (off-state) current I_{OFF} and carrier mobilities in the on-state (μ_{eff}) [2].

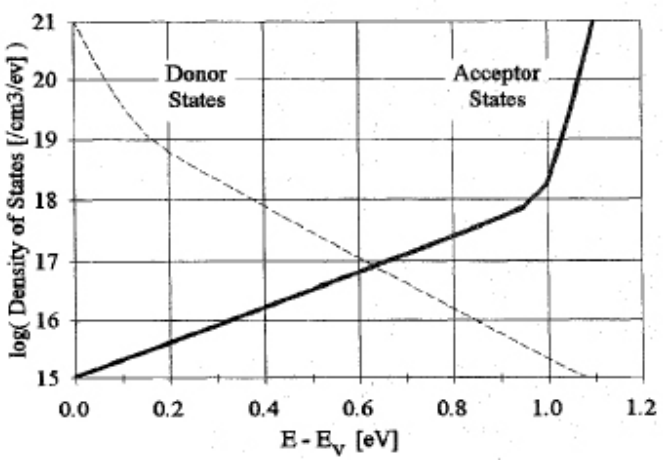

Figure 3.1. Density of states in the Si bandgap due to presence of grain boundaries in a poly-Si film [1].

These defects can be passivated by introducing a passivation species, usually hydrogen (H), to terminate Si dangling and strained bonds by methods such as plasma treatment [3, 4, 5] or ion implantation [6, 7]. After hydrogenation, TFT characteristics show improvements with decreases in threshold voltage and subthreshold slope and increases in mobility [5].

Hydrogen plasma treatment is the conventional approach to defect passivation, wherein poly-Si TFTs are exposed to hydrogen plasma at elevated substrate temperatures ($\sim$ 350-425°C) so that hydrogen can diffuse into the channel and passivate defects [3, 8]. Though performance improvements are seen after hydrogenation, hydrogenated poly-Si TFTs show significant shifts in threshold voltage with electrical stress. It is believed that the dominant degradation mechanism arises due to the relatively weak Si-H bond, which breaks under electrical stress, generating additional midgap trap states [9].

Ion implantation of any passivation species has a lower associated process thermal budget compared to plasma treatment, and is more suited for a plastic substrate compatible process. Defect passivation by ion implantation has been studied for several passivation species such as deuterium [10], fluorine [11, 12], nitrogen and oxygen [12] since they have stronger bond strengths with Si compared to H. In the case of [10] and [11], the implantation of passivation species is not integrated into a TFT fabrication process utilizing poly-Si crystallized by laser annealing. In Good *et al.* [12, 13], the hydrogenated TFTs showed

better reliability compared to fluorine, nitrogen or oxygen passivated TFTs despite reported stronger Si bond strengths with the larger atoms.

A monolayer of selenium (Se) is known to effectively passivate Si surfaces by terminating dangling bonds and relaxing strained bonds [14, 15]. Selenium and sulfur are group-VI atoms which can bond with Si(100) surfaces to terminate broken Si covalent bonds. However, Se is preferable since it introduces less strain at the surface. Se is of particular interest because, in bulk form, it exhibits similar local bonding geometry, bond length and bond angle with Si. The restoration of the Si(100) surface with Se is an exothermic process with a small amount of energy released to prevent undesirable chemical reactions [16].

In this chapter, the effect of Se passivation by ion implantation is investigated for poly-Si TFTs. Se is implanted into the Si film prior to crystallization by pulsed excimer laser annealing (ELA). Aside from the control (unpassivated) sample, two samples are implanted, one with a low Se dose of 10^{13}cm^{-2} and one with a high Se dose of 10^{14}cm^{-2}. The three samples are passivated in hydrogen plasma at 350°C for 1 hour to compare defect passivation techniques on the performance and reliability of poly-Si TFTs.

3.2 Process Flow

Self-aligned top-gated TFTs were fabricated on Si(100) 6-inch p-type wafers using a glass-compatible process with maximum substrate temperature of 600°C. First, a 1-μm thick buffer layer of silicon dioxide (SiO_2) is deposited by low-pressure chemical vapor deposition (LPCVD) at 450°C. Then, a 50-nm thick amorphous Si (a-Si) layer is deposited by LPCVD at temperature and pressure of 530°C and 400 mT, respectively, using silane (SiH_4) as a precursor gas. A 10-nm thick SiO_2 layer is deposited by LPCVD to act as an implant capping layer. A Se implant is then performed with dose of 10^{13}cm^{-2} or 10^{14}cm^{-2} and energy of 25 keV (see Fig. 3.2(a)). The projected range of Se is halfway into the a-Si film, according to SRIM data [17]. The control device regions are masked with thick

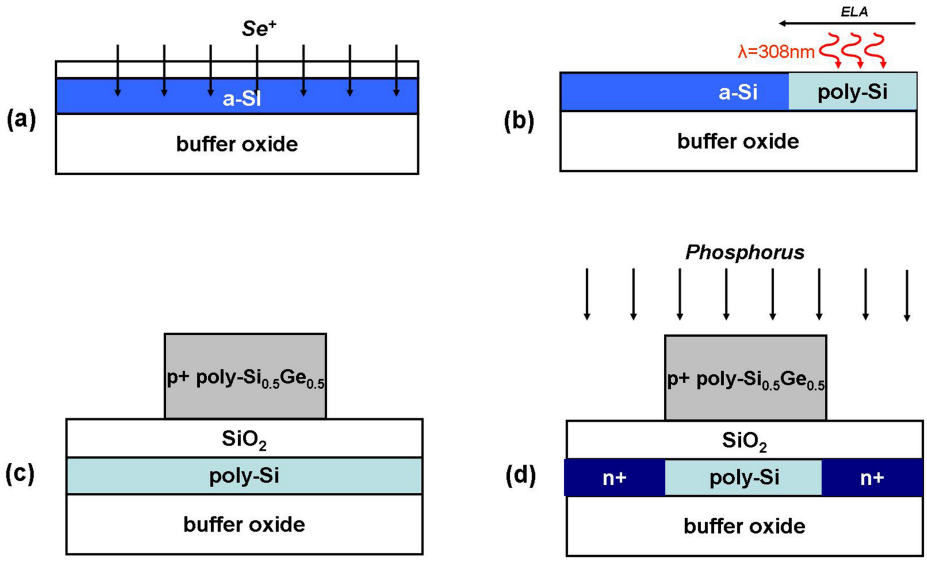

Figure 3.2. Fabrication process flow for Se-implanted poly-Si TFTs.

photoresist to block the Se implant from reaching the Si layer. Afterwards, the photoresist and capping SiO_2 layer are selectively removed.

The a-Si film is crystallized by pulsed (30 ns) XeCl excimer laser (λ=308 nm), annealing with 4 laser shots at various fluences of $250, 275, 300, 325 \frac{\text{mJ}}{\text{cm}^2}$ (see Fig. 3.2(b)). After the poly-Si film is patterned by lithography and reactive ion etching (RIE), a 50-nm thick SiO_2 gate dielectric layer is deposited by LPCVD at temperature and pressure of 450°C and 300 mT, respectively, using SiH_4 and oxygen (O_2) precursor gases, then densified in N_2 at 600°C for 4 hours. A 200-nm thick *in-situ* doped p+ poly-$Si_{0.5}Ge_{0.5}$ gate layer is then deposited by LPCVD at 550°C and 400 mT with diborane (B_2H_6), SiH_4 and germane (GeH_4) precursor gases. P+ poly-$Si_{0.5}Ge_{0.5}$ is advantageous over poly-Si as a gate material since it has lower resistivity and can be formed at lower temperatures than poly-Si [18]. After the gate electrodes are patterned by lithography and RIE (see Fig. 3.2(c)), phosphorus is implanted at dose and energy of $2 \times 10^{15}\text{cm}^{-2}$ and 40 keV, respectively, to form self-aligned n+ source and drain regions (see Fig. 3.2(d)).

Next, a 100-nm thick SiO_2 passivation layer is deposited by LPCVD at 450°C, then the implanted dopants are activated at 600°C for 4 hours in N_2. Device fabrication is completed

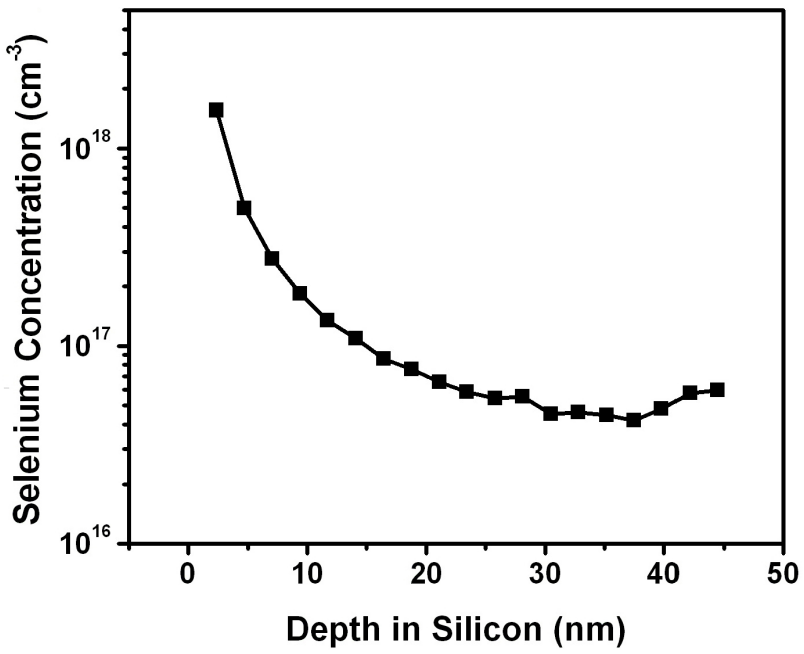

Figure 3.3. Selenium concentration profile in a poly-Si film formed with a Selenium implant dose of 10^{13}cm^{-3} and ELA laser fluence of $300\frac{\text{mJ}}{\text{cm}^2}$.

with contact hole formation and aluminum (Al) metal layer deposition by direct current (DC) sputtering at 300°C. The metal is patterned and etched in wet Al etchant. Lastly, a forming-gas anneal at 350°C for 30 minutes in $90\%\text{N}_2/10\%\text{H}_2$ is performed. Half of the control and Se-implanted devices were exposed to hydrogen plasma at 350°C for 1 hour to assess benefits of Se passivation versus hydrogenation.

Secondary ion mass spectrometry (SIMS) analysis was performed on poly-Si formed with low dose Se implantation and ELA at laser fluence of $300\frac{\text{mJ}}{\text{cm}^2}$, 4 laser pulses. From this analysis, the average concentration of selenium in the film was found to be $1.84 \times 10^{17}\text{cm}^{-3}$. The Se concentration profile in the poly-Si film is shown in Fig. 3.3.

Table 3.1. Average and standard deviation for effective mobility (in $\frac{cm^2}{V \cdot s}$) for unpassivated, Se-passivated and H-passivated TFTs. The standard deviation is noted in parentheses on the second line.

Laser fluence	control	Se(10^{13})	Se(10^{14})	H	Se(10^{13})+H	Se(10^{14})+H
250	29.4	34.2	29.4	16.7	42.0	38.9
	(14.7)	(7.1)	(13.7)	(10.5)	(15.5)	(35.8)
275	52.2	63.8	41.5	61.9	65.0	46.4
	(14.0)	(15.3)	(20.5)	(7.2)	(28.2)	(33.6)
300	68.8	85.4	50.5	77.7	90.9	90.8
	(13.5)	(21.5)	(19.5)	(25.2)	(7.1)	(13.4)
325	50.1	64.1	42.2	46.6	76.3	51.7
	(33.0)	(42.2)	(29.1)	(57.2)	(18.1)	(40.6)

3.3 Effects of Selenium on TFT Performance

3.3.1 Optimal ELA Process Condition

Typical TFT device parameters were extracted from measured transfer characteristics for devices with gate dimensions of W=10 μm and L=5 μm for the various passivation techniques. The highest mobility was achieved with a laser fluence of $300\frac{mJ}{cm^2}$ for control and Se-passivated devices, shown in Fig. 3.4. The effective mobility is calculated from the maximum transconductance for V_{DS}=0.5 V by the equation $\mu_{eff} = \frac{g_{max} \cdot L}{Cox \cdot W \cdot V_{DS}}$. For the hydrogenated devices, the optimal effective mobility is seen at the same laser fluence of $300\frac{mJ}{cm^2}$, shown in Fig. 3.5. In Table 3.1, the average and standard deviation of the mobility for all passivation techniques is tabulated.

The hydrogen-passivated samples demonstrate improvements in mobility, as expected. For near-optimal laser fluences (275 to 300 $\frac{mJ}{cm^2}$), there is smaller variation in mobility for various Se implant doses since hydrogenation successfully passivates a large fraction of the tail states in the poly-Si film which affects mobility. At laser fluences which give finer grained poly-Si, at 250 and 325 $\frac{mJ}{cm^2}$, the variation in mobility is greater, possibly due to slow

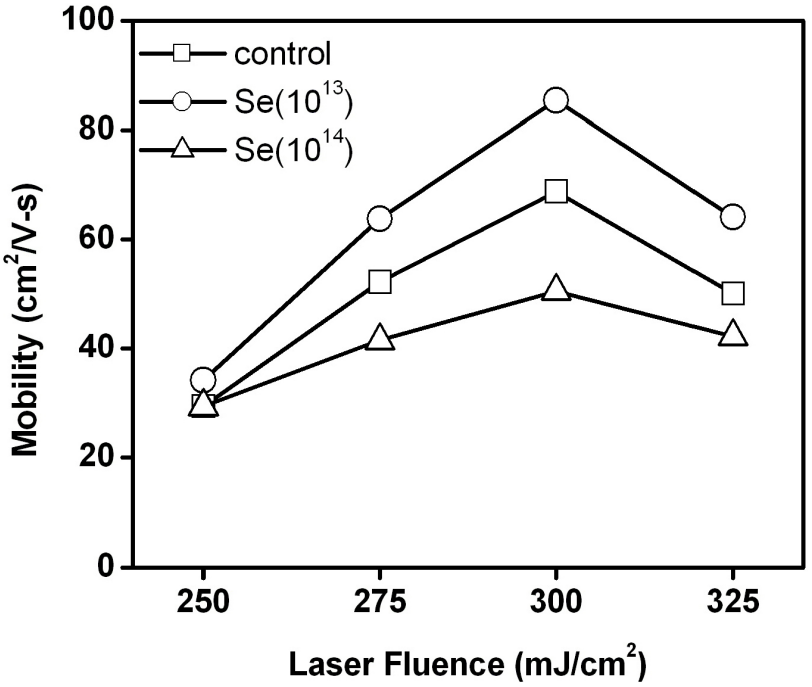

Figure 3.4. Dependence of effective mobility (μ_{eff}) on excimer laser fluence for control and Selenium-passivated TFTs. Optimal laser fluence is evident at $300\frac{\text{mJ}}{\text{cm}^2}$.

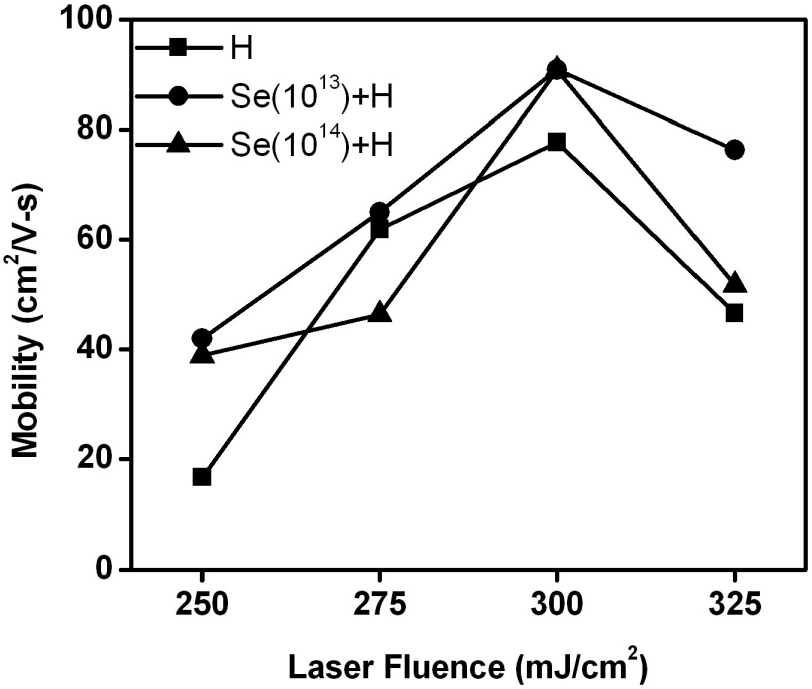

Figure 3.5. Dependence of effective mobility (μ_{eff}) on excimer laser fluence for hydrogenated samples with and without Selenium passivation. Optimal laser fluence is evident at $300\frac{\text{mJ}}{\text{cm}^2}$.

Table 3.2. Average and standard deviation for various performance parameters for control and Selenium-passivated TFTs.

	V_T (σV_T) V	S (σS) V/dec	I_{ON} (σI_{ON}) $\mu A/\mu m$	I_{OFF} (σI_{OFF}) $pA/\mu m$
control	6.22 (0.13)	0.69 (0.10)	3.9 (0.8)	105 (18.6)
Se(10^{13})	6.15 (0.18)	0.56 (0.08)	3.8 (0.4)	35 (13.5)
Se(10^{14})	3.33 (0.24)	1.73 (0.12)	7.9 (1.6)	785 (529)

hydrogen diffusion within poly-Si films with high defect density. The incomplete passivation of the defects is evidenced by the higher threshold voltages seen in these devices.

3.3.2 Impact of Selenium Dose

Typical measured transfer characteristics and transconductance for control and Se-passivated TFTs at the optimal laser fluence with gate dimensions of W=10 μm and L=5 μm are shown in Figs. 3.6 and 3.7 for a drain bias of V_{DS}=5 V.

The average values and standard deviation for key device performance parameters (V_T, S, I_{ON}, I_{OFF}) are tabulated in Table 3.2. The threshold voltage (V_T) is extracted using the constant current method, where $V_T = V_{GS}$ at $\frac{I_{DS}}{W} = 10^{-7}\frac{A}{\mu m}$. Subthreshold slope (S) is extracted at the maximum slope of log(I_{DS}) versus V_{GS} when V_{DS}=5 V. I_{ON} is defined as I_{DS} when $V_{GS} = V_T$+8V and I_{OFF} is defined as the minimum I_{DS} for V_{DS}=5 V.

The low-dose Se-passivated TFTs (denoted by Se(10^{13})) exhibit improved on and off-state performance compared to the control (unpassivated) devices. It appears that the Se introduced has successfully passivated some of the defects and has not doped the channel (since only a small shift appears in threshold voltage). In comparison, the high-dose Se TFTs (denoted by Se(10^{14})) demonstrate degraded S and a V_T shift in the negative direction. The higher Se implant dose shows evidence that Se is diffusing into the poly-Si grains, and doping the channel. Since Se is a group-VI atom, it can act as a double n-type donor in Si films. For moderate-doped body concentrations, the n+-n-n+ structure cannot be effectively turned off by the gate bias (since the channel cannot be fully depleted). This explains the decrease

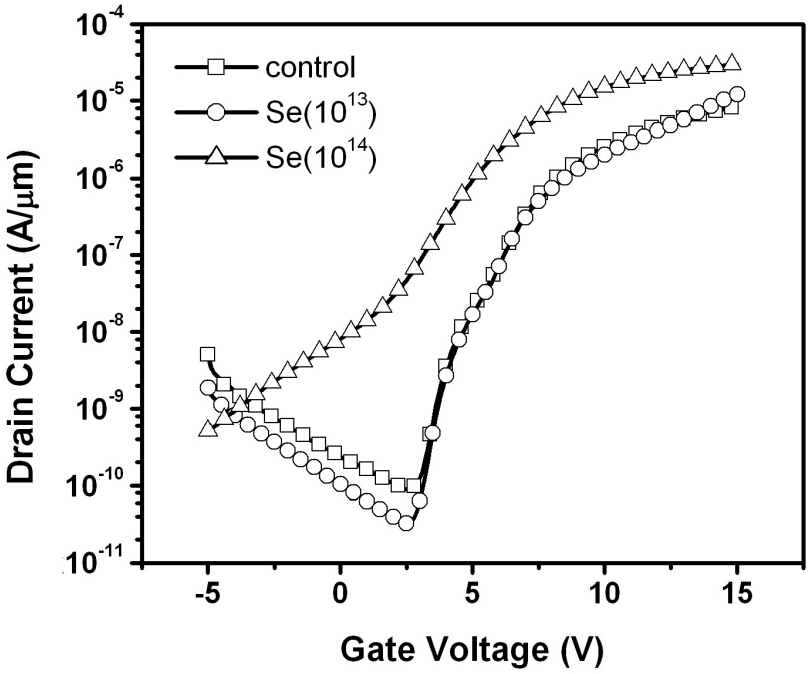

Figure 3.6. Transfer characteristics of control and Se-passivated TFTs of W/L=10μm/5μm, crystallized at laser fluence of 300 $\frac{\text{mJ}}{\text{cm}^2}$. The drain current is normalized to the transistor width.

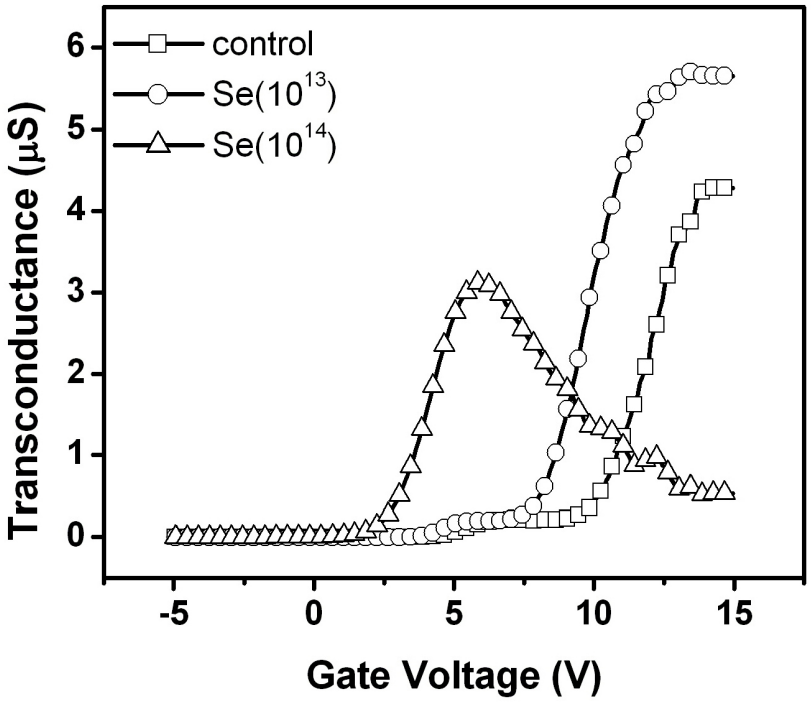

Figure 3.7. Transconductance of the corresponding control and Se-passivated TFTs.

in V_T, increase in I_{OFF} and degradation in S. The humps seen in the transfer characteristics are due the mesa structure of the active region, which causes conduction at the active region edges to have a lower threshold voltage due to sidewall gating.

The low-dose Se passivation provides for lower leakage current (I_{OFF}) and higher effective mobility (μ_{eff}), suggesting that it is more effective at passivating intra-grain strained-bond defects in poly-Si which gives rise to band-tail states. However, Se passivation is not effective for reducing V_T and S, suggesting that Se does not readily segregate or diffuse to grain boundaries during the laser crystallization process or subsequent thermal treatments. Dangling bond defects predominant at grain boundaries give rise to mid-gap states which more strongly affect V_T and S [2].

3.4 Comparison of Hydrogen and Selenium Passivation Techniques

3.4.1 Effects of Hydrogenation on Control and Se-passivated TFTs

The transfer characteristics and transconductance of hydrogenated TFTs of gate dimensions W=10 μm and L=5 μm for V_{DS}=5 V are shown in Figs. 3.8 and 3.9. The average and standard deviations for key device parameters are tabulated in Table 3.3. Hydrogen is effective for reducing dangling bond defects that lower V_T and S for short anneal times, as expected. However, the hydrogen plasma treatment is not long enough to fully passivate strained-bond defects that degrade μ_{eff} and I_{OFF}. Usually, hydrogenation for times $>$ 4 hours is required before passivating strained-bond defects [2]. Interestingly, the Se(10^{13})+H passivated TFTs exhibit higher transconductance at higher gate voltages (V_{GS} >10 V) compared to H-passivated TFTs, which may be indicative of field-enhanced ionization of Se atoms within the channel. Since Se is a deep-level donor in Si, a high gate voltage can induce a sufficiently high electric field for the Se atoms in the poly-Si grains to ionize and contribute conduction electrons in the channel.

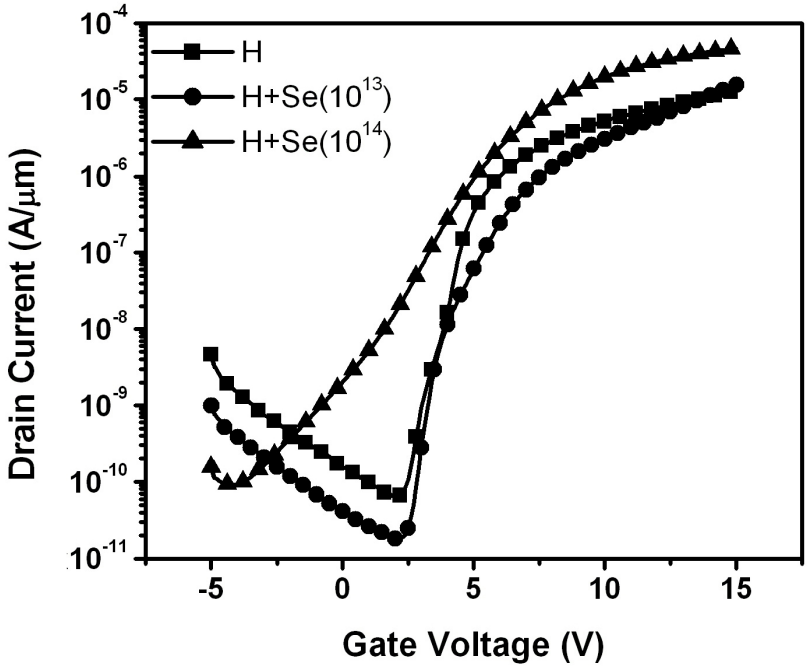

Figure 3.8. Transfer characteristics of hydrogenated control and Se-passivated TFTs of W/L=10μm/5μm, crystallized at laser fluence of 300 $\frac{\text{mJ}}{\text{cm}^2}$. The drain current is normalized to the transistor width.

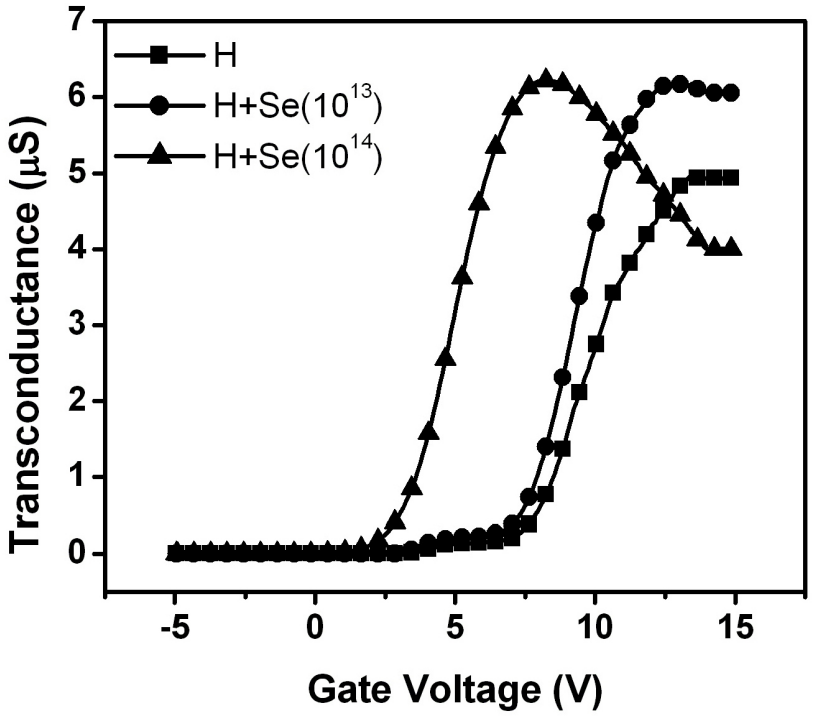

Figure 3.9. Transconductance of the corresponding hydrogenated control and Se-passivated TFTs.

Table 3.3. Average and standard deviation for various device parameters for hydrogenated control and Selenium-doped TFTs.

	V_T (σV_T) V	S (σS) V/dec	I_{ON} (σI_{ON}) $\mu A/\mu m$	I_{OFF} (σI_{OFF}) $pA/\mu m$
H	4.78 (0.70)	0.45 (0.13)	4.0 (1.2)	42 (18.0)
H+Se(10^{13})	5.19 (0.30)	0.42 (0.04)	3.8 (0.5)	16 (5.2)
H+Se(10^{14})	3.49 (0.13)	1.54 (0.12)	10.1 (1.2)	98 (96)

3.4.2 Effect of Passivation Technique on Short Channel Effects

Scaling down of the TFT gate length provides for improvements in performance and device density; however short channel effects are more pronounced in poly-Si TFTs at relatively large gate lengths (≤ 8 μm) compared to monocrystalline Si MOSFETs [19, 20]. Short channel effects arise since at shorter gate lengths, the drain has stronger capacitive coupling to the channel, especially for large drain biases. Avalanche-induced short channel effects drastically reduce V_T at large drain biases. The high lateral electric fields cause impact ionization which generates additional electron-hole pairs that are added to the channel. Steeper subthreshold slope and a kink in the output characteristics are evidence of avalanche generation in the channel [20, 21]. The effect is amplified in poly-Si since it has a higher carrier concentration (in the charge neutral regions around the grain boundaries) in the subthreshold regime that causes more avalanche generation [22].

The effect of Se(10^{13}) and hydrogen passivation on short channel effects is examined. The V_T dependence on transistor gate length is shown in Fig. 3.10, in the average V_T shift from that of L=10 μm TFTs. The threshold voltage is defined using the constant current method, where $V_T = V_{GS}$ at $\frac{I_{DS} \cdot L}{W} = 5 \times 10^{-7}$A when V_{DS}=5 V, consistent with the previous definition. Hydrogenation results in significant V_T reduction, whereas Se passivation does not. The large reduction is attributed to enhanced phosphorus dopant activation near the gate edges, resulting in shorter effective channel length [8]. Se passivation does not significantly impact the activation of other dopants in the poly-Si film.

Drain-induced barrier lowering (DIBL) is also more prominent in poly-Si TFTs. Due to

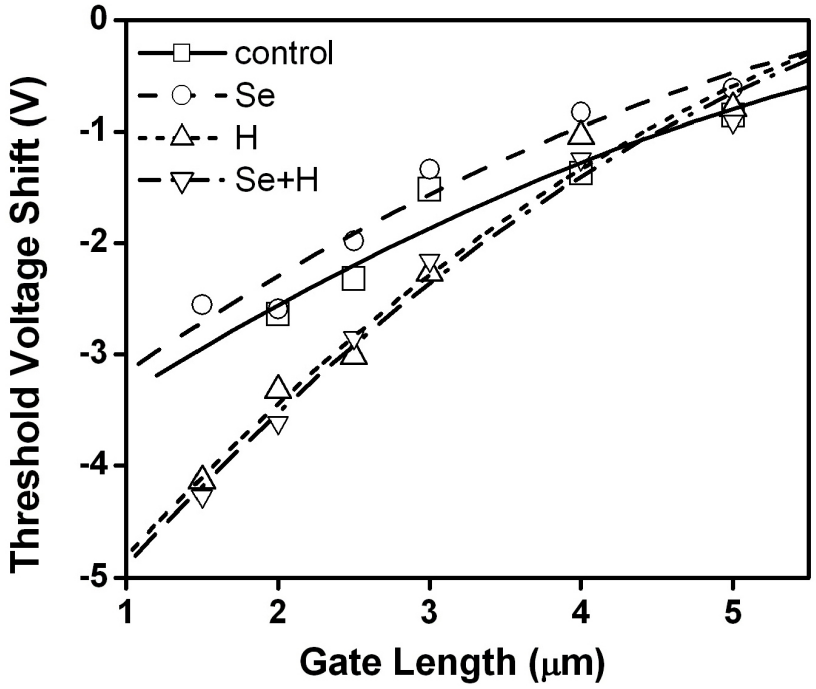

Figure 3.10. Comparison of threshold voltage reduction vs. transistor gate length for various defect passivation techniques.

additional carrier generation during impact ionization at high drain biases, the difference between the threshold voltages at low and high drain biases is expected to be large. Also, high lateral fields from the drain junction will decrease the barrier height at the grain boundaries [23], an effect called drain-induced grain barrier lowering (DIGBL). The DIBL parameter is measured by taking the threshold voltage difference between low (V_{DS}=0.5 V) and high drain biases (V_{DS}=5 V), normalized to the drain bias difference, shown in Fig. 3.11. The avalanche generation and DIGBL effects are not isolated in this parameter, but both effects are amplified with decreasing gate lengths, and particularly affect poly-Si films with large trap state density.

The Se(10^{13})-passivated TFTs exhibit the lowest amount of DIBL compared to the control and hydrogenated TFTs, as expected. Since hydrogenated devices have shorter effective channel length, their DIBL effect is more prominent as the gate length scales down. The control devices have a higher density of trap states and therefore more prominent

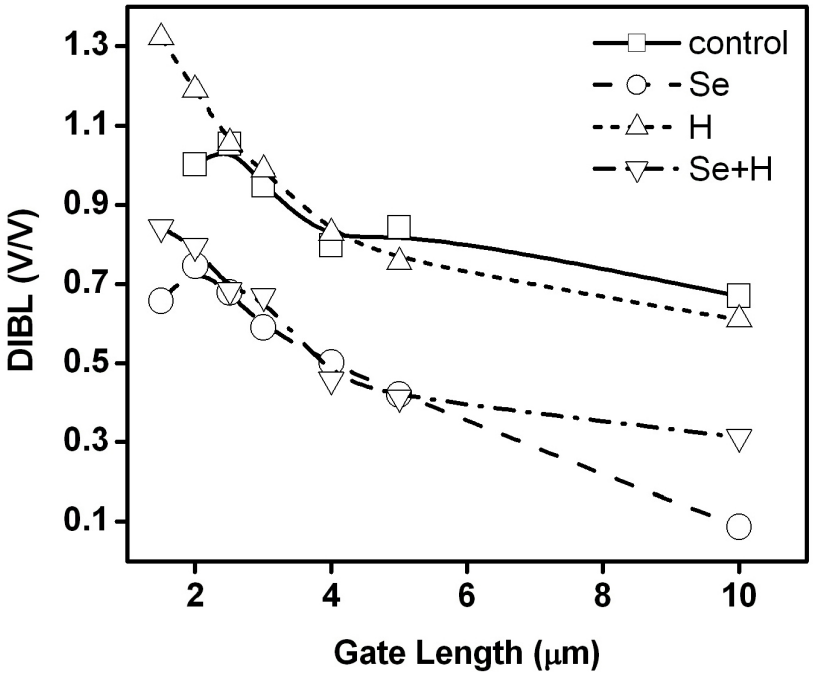

Figure 3.11. Comparison of DIBL for different transistor gate lengths for each defect passivation technique.

avalanche effects, thus worsening the DIBL parameter. In comparison, the Se-passivated TFTs show superior short channel behaviour due to lower trap state density.

3.5 TFT Hot Carrier Reliability for Different Passivation Techniques

TFTs with gate dimensions W=20 μm and L=5 μm, for each of the defect passivation techniques, were subjected to hot carrier reliability testing. The Se(10^{14}) TFTs were not subjected to reliability tests due to their poor performance. The devices were stressed with a DC bias condition of $V_{DS} = V_{GS}$=7 V for durations of 1, 10, 100, 1000, 10000 seconds (s), corresponding to the saturation region of operation. The evolution of V_T is tracked for forward mode (with source and drain electrodes the same as used for stressing) as well as reverse mode (with source and drain electrodes interchanged for stressing) operation. The

threshold voltage shift (ΔV_T) due to hot carrier stress is shown in Figs. 3.12 and 3.13, respectively.

During DC bias stress, defects are formed near the drain due to depassivation. The reverse-mode V_T is much more sensitive than the forward-mode V_T to charge trapped near the drain. This is because in the forward mode, the damage near the drain junction is shielded by the drain depletion region during measurement. In reverse mode, the damage is at the source end (which is the drain end during stress), and the mobile carrier density is strongly affected. The Se-passivated TFTs show more stable operation than hydrogenated TFTs, indicating that the Se has passivated a significant fraction of dangling bond defects in the poly-Si due to the stronger Si-Se (548 $\frac{kJ}{mol}$) bond compared to Si-H (299 $\frac{kJ}{mol}$) [24]. The impact of broken Si-H bonds is evident in reverse mode measurements for both H and Se+H passivated devices.

3.6 Summary

Low dose ($10^{13}cm^{-2}$) Se ion implantation prior to crystallization by ELA is an effective, low-thermal-budget technique for passivating dangling and strained bond defects to improve the performance of poly-Si TFTs. On the other hand, high dose ($10^{14}cm^{-2}$) Se implantation degrades the off-state performance (resulting in high I_{OFF}, degraded S).

The effects of Se passivation (lower I_{OFF} and higher μ_{eff}) are complementary to those of conventional plasma hydrogenation for short anneal times (lower V_T and steeper S), so optimal performance can be achieved with a combination of both techniques. TFTs with Se passivation are less susceptible to short channel effects such as V_T roll off and DIBL. The Se in the poly-Si film does not affect the activation of other dopants within poly-Si, and provides for more stable TFT operation under hot carrier reliability stressing.

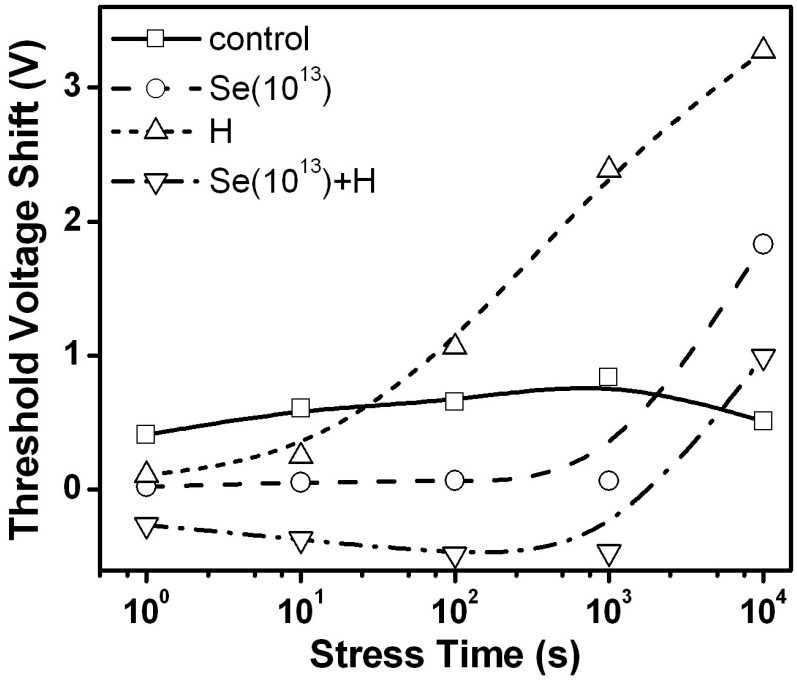

Figure 3.12. V_T shift with DC bias stress duration in the forward mode.

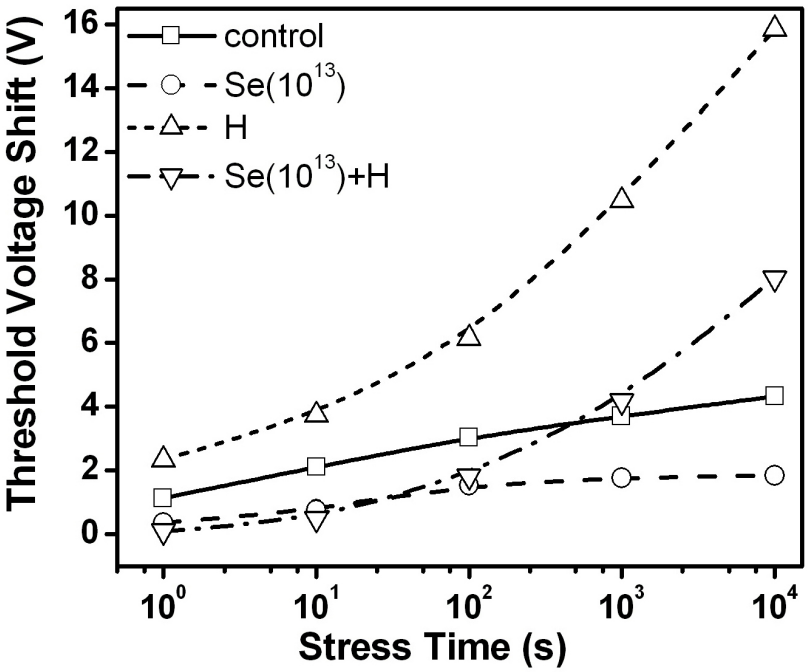

Figure 3.13. V_T shift with DC bias stress duration in the reverse mode

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Chapter 4

Accumulation-Mode Poly-Si Thin Film Transistors

4.1 Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs) are the highest performace devices for active-matrix liquid crystal displays (AMLCDs) due to their relatively high carrier mobilities. However, poly-Si films have many grain boundary and intragrain defects, degrading the electrical characteristics and causing device-to-device variation. The main challenge for conventional enhancement-mode TFT technology is large sensitivity to the number and location of grain boundary defects in the undoped or lightly doped body [1]. Based on Seto's charge trapping model [2], grain boundaries in a lightly doped film form large and wide potential barriers that appear in the channel, as shown in Fig. 4.1. Defects in the grain boundaries act as traps that can immobilize carriers and become charged. Once charge is trapped, depletion regions form around the trapped charge to maintain charge neutrality. At low channel doping concentrations, large TFT bias voltages are required to supply carriers with enough energy to travel over or tunnel through the resultant potential barriers. Thus, large threshold voltages are typically seen [2, 3, 4].

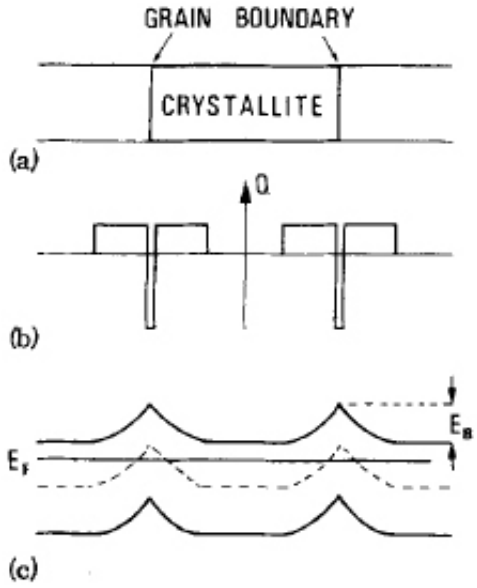

Figure 4.1. A film with two grain boundaries is shown in (a). Large density of trapping sites (N_T) at the grain boundaries are able to capture carriers, shown in the charge-density diagram in (b). Large energy barriers appear at the grain boundaries, shown in the energy band diagram in (c). The curvature of the energy bands are a result of the depletion regions. For undoped or lightly doped films, large and wide potential barriers are seen by the carriers [3].

The height of the potential barrier at a grain boundary in a poly-Si film increases with the doping concentration until it exceeds a critical concentration $N^*=\frac{N_T}{L}$, where N_T is the areal trap density and L is the length of the grain. Once the doping levels exceed N^*, the density of trapped carriers remains at a constant $\frac{N_T}{L}$ and the remaining carriers are mobile in the neutral regions of the grain. As the carrier concentration increases, the depletion regions next to the grain boundaries narrows, thus the potential barrier at the grain boundary decreases in height and width, as shown in Fig. 4.2 [2, 4]. For high quality poly-Si films with low grain boundary trap densities, carrier transport is not degraded significantly by grain boundaries, at dopant concentrations above $\sim 10^{18}\text{cm}^{-3}$ [3].

Another problem seen in conventional enhancement-mode TFTs is large leakage currents that exhibit an exponential dependence on gate and drain bias. The leakage mechanism is attributed to the large lateral electric field in the off-state that exists in the drain depletion region due to the steep dopant gradient between the undoped channel and highly-doped

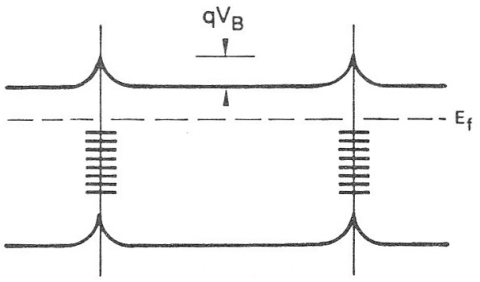

Figure 4.2. Potential barriers in a poly-Si film with doping greater than the critical concentration. All trap sites are filled leading to a reduction in barrier height and width [4].

drain. In the off-state, leakage occurs due to field-enhanced tunneling and trap-assisted tunneling. Leakage currents can be reduced by decreasing the electric field at the drain junction [1].

The accumulation-mode MOSFET design has been proposed for silicon-oxide-insulator (SOI) devices for CMOS applications [5]. It is proposed here for polycrystalline-Si devices to alleviate sensitivity to channel defects and to reduce leakage current. In this chapter, the accumulation-mode TFT is investigated via 2-dimensional device simulation. The effect of a grain boundary defect on the electrical characteristics of an accumulation-mode TFT is investigated. Lastly, a fabrication process for the accumulation-mode TFT is proposed.

4.2 Accumulation-Mode TFT Operation

The accumulation-mode TFT operates differently from conventional enhancement-mode TFTs. This structure takes advantage of a moderately doped (above N*) body to minimize sensitivity to grain boundaries. The structure employs a uniformly doped channel of the same dopant type as the source and drain (S/D) regions (*i.e.* a p-type accumulation-mode TFT has highly-doped p+ S/D regions and moderately p-type channel; an n-type accumulation-mode TFT has highly doped n+ S/D regions and moderately n-type channel). The work function of the gate electrode and channel film thickness are chosen so that the Si channel under the gate is fully depleted at a gate bias (V_G) of 0 V. For an

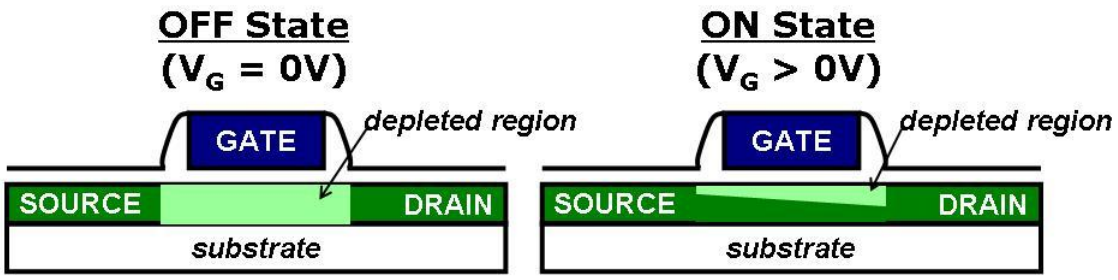

Figure 4.3. Schematic cross-section of an n-channel accumulation-mode TFT operation in the on- and off-states.

n-type accumulation-mode TFT, the gate workfunction must be high, corresponding to materials such as p+ poly-Si or molybdenum (Mo). Symmetric operation requires a p-type accumulation-mode TFT to have a low workfunction gate, such as n+ poly-Si or aluminum (Al). An n-type device is turned on by applying a gate voltage above 0 V, whereas a p-type device is turned on by negative V_G. With an applied gate bias that is greater than the threshold voltage, the channel region becomes only partially depleted, so that current can flow through the undepleted portion of the channel, as illustrated in Fig. 4.3.

Due to the buried channel operation, the device is less sensitive to defects at the gate/dielectric interface. Thus operation of the accumulation-mode TFT may be superior by eliminating the possibility that free carriers can be trapped at the interface or in the gate dielectric, causing reliability problems. Reliability is also improved from the reduction in lateral electric field between the channel and S/D regions, decreasing leakage currents.

4.3 Simulation-based Design Study

An n-type accumulation-mode TFT device is simulated and optimized using the Taurus Device simulator by Synopsys Incorporated [6]. In this study, a TFT of gate length L_G=2 μm is simulated with varying channel doping, silicon dioxide (SiO_2) gate dielectric thickness and Si film thickness. For this initial study, the channel material is assumed to be monocrystalline Si; at the simulated body dopant concentrations, the mobilities of carriers in the polycrystalline and monocrystalline forms are comparable. A schematic cross-section

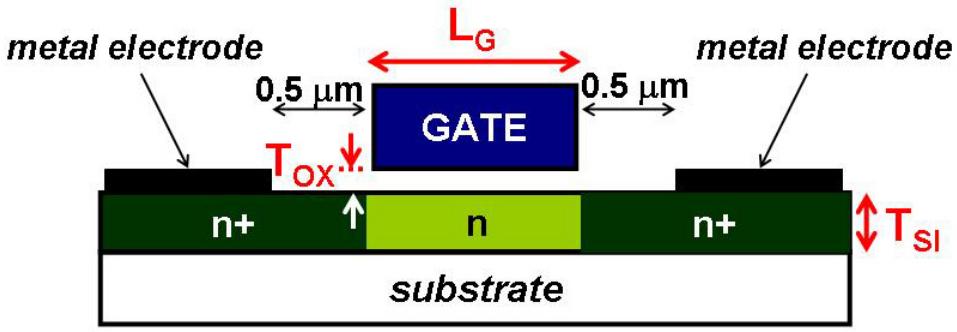

Figure 4.4. Schematic cross-section of simulated accumulation-mode TFT.

Table 4.1. Simulation parameters for n-type accumulation-mode TFT device.

Parameter	Value
Channel length (L_G)	2 μm
Silicon film thickness (T_{SI})	10-50 nm
Gate oxide thickness (T_{OX})	5-50 nm
Body doping (N_{CH})	10^{17}cm^{-3}-10^{19}cm^{-3}
Source/drain doping ($N_{S/D}$)	10^{21}cm^{-3}
Gate workfunction (Φ_M)	5.0 eV
Gate edge to S/D electrode spacing ($L_{S/D}$)	0.5 μm

of the simulated device is illustrated in Fig. 4.4. No contact resistance is assumed between the metal electrodes and the heavily-doped source and drain regions ($N_{S/D} = 10^{21}$cm^{-3}). The source/drain doping profiles are assumed to be abrupt junctions but a more gradual S/D doping profile does not greatly affect the device characteristics. The gate workfunction is chosen to be that of Mo (Φ_M=5.0 eV). Table 4.1 shows the range of simulation parameters explored in this study.

4.3.1 Optimization of TFT Dimensions

Accumulation-mode TFTs require thin gate oxide thickness (T_{OX}) and silicon film thickness (T_{SI}). To find the range of T_{OX} and T_{SI} that can provide for high on/off current ratio, a large range of T_{OX} and T_{SI} are simulated for constant body doping of $N_{CH} = 10^{18}$cm^{-3} and gate length of L_G=2 μm. In Figs. 4.5 and 4.6, the effect of oxide and

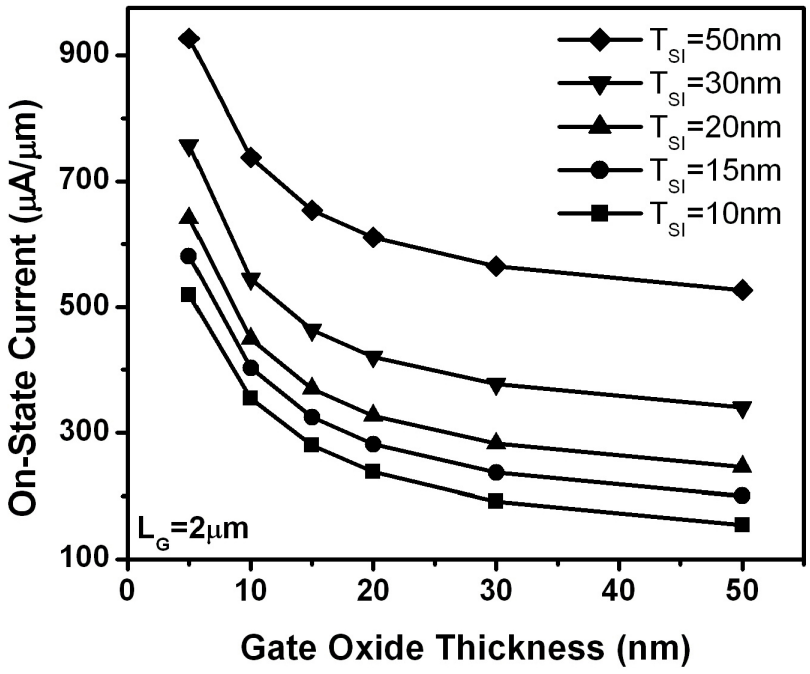

Figure 4.5. Dependence of on-state current on gate oxide and silicon film thicknesses.

Si film thicknesses on the on-state current (I_{ON}) and off-state current (I_{OFF}) is illustrated. For this simulation, I_{ON} is defined as the drain current for the bias condition $V_{GS} = V_{DS}$=5 V and I_{OFF} is the drain current when V_{GS}=0 V and V_{DS}=5 V.

For thick oxide or thick Si films, the I_{OFF} is large ($> 10^8 A/\mu m$) since the device cannot fully turn off (*i.e.* the channel cannot be fully depleted). Thus, thin T_{OX} and T_{SI} films $\sim$ 10 nm are necessary to turn off the device. It is important to note that TFTs with dimensions such as T_{OX}=10 nm and T_{SI}=15 nm can turn off if negative gate biases are used. The threshold voltage (V_T) of this device is -0.89 V, extracted from the transfer characteristics in the saturation region (since $V_{DS} > V_{GS} - V_T$) from the plot of $\sqrt{I_D} - V_G$. The transfer and output characteristics of a device with T_{OX}=10 nm and T_{SI}=15 nm are shown in Figs. 4.7 and 4.8, respectively.

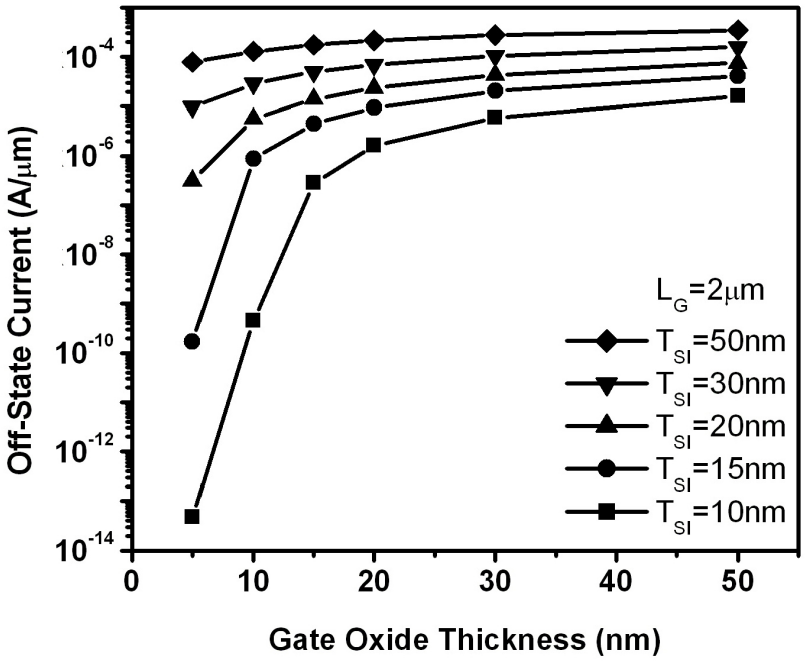

Figure 4.6. Dependence of off-state current on gate oxide and silicon film thicknesses.

4.3.2 Optimization of Body Dopant Concentration

Channel on-state resistance is dependent on the quality of the poly-Si film, the number and location of the grain boundaries and the areal trap density of the charge traps. As shown in Fig. 4.9, the resistivity is very sensitive around the critical dopant concentration (N*), and varies across several orders of magnitude, for doping in the range from 10^{17} to 10^{18}cm^{-3}. This critical concentration decreases with an increasing grain size [7]. Above N*, the resistivity of poly-Si approaches that of monocrystalline Si and exhibits lower sensitivity to doping levels. Thus, the optimal body doping concentration for an accumulation-mode TFT lies slightly above N*.

Larger body dopant concentrations are favourable to minimize the device variation due to grain boundaries. However, films with higher body doping concentration have narrower depletion width, and at concentrations higher than $N_{CH} = 5 \times 10^{18}\text{cm}^{-3}$ they can no longer be fully depleted for oxide and Si film thicknesses of 10-nm and 15-nm, respectively. In Fig. 4.10, the I_{OFF} and the I_{ON}/I_{OFF} current ratio are shown for various

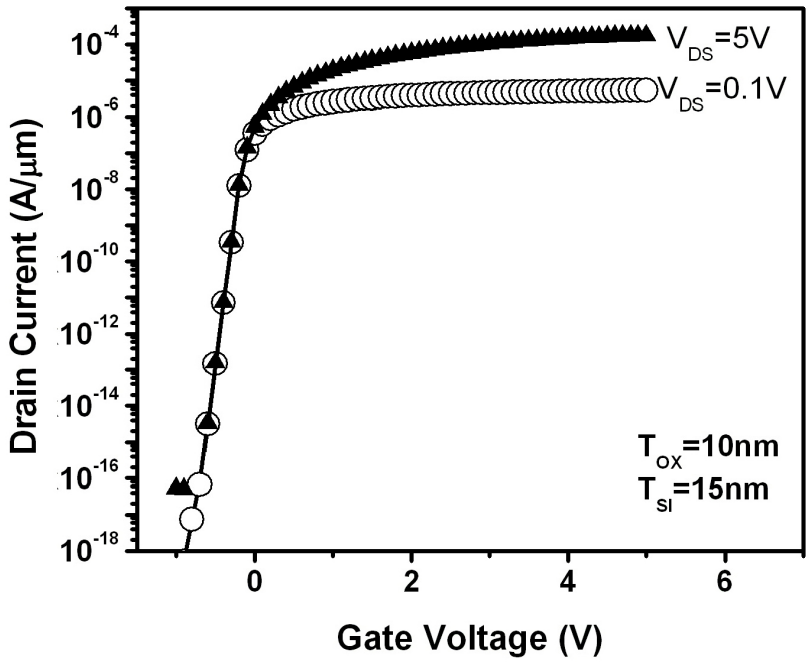

Figure 4.7. Transfer characteristics for an optimized accumulation-mode MOSFET for drain bias of V_D=0.1 V and 5 V.

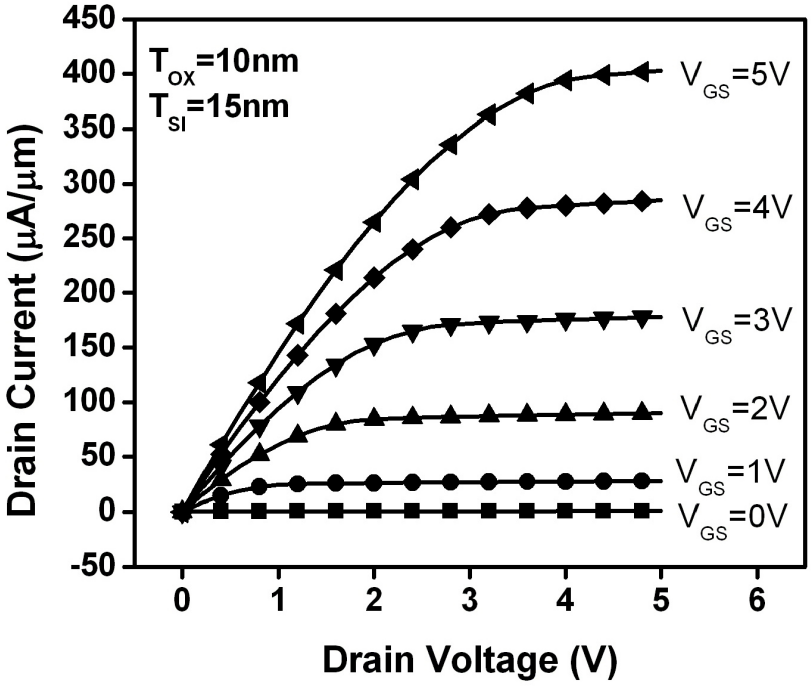

Figure 4.8. Output characteristics for an optimized accumulation-mode MOSFET for gate bias of V_G=0, 1, 2, 3, 4, 5 V.

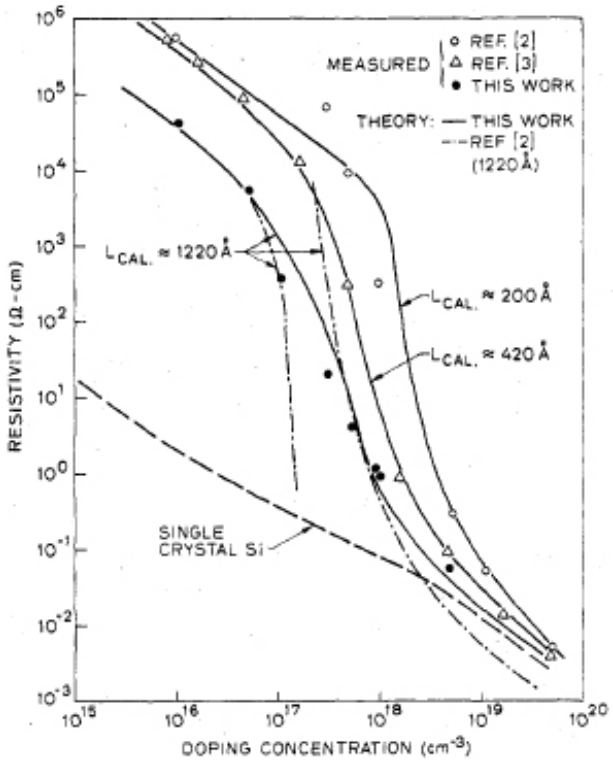

Figure 4.9. Dependence of polycrystalline and single crystal Si resistivity on dopant concentration for various grain sizes [7].

body doping concentrations with TFT dimensions of T_{OX}=10 nm and T_{SI}=15 nm and L_G=2 μm. Accumulation-mode TFT designs with higher body dopant concentrations will require even thinner oxide and Si thin film depositions, which are not easy to manufacture. In considering the N_{CH} in the accumulation-mode TFT design, trade-offs are made between decreasing sensitivity to grain boundaries (with higher N_{CH}) and lowering leakage currents (with lower N_{CH}). With advancements in laser crystallization methods, poly-Si grain sizes up to 200-μm can be obtained [8, 9]. For poly-Si films with large grain sizes, the critical concentration decreases. If the accumulation-mode TFT is designed with lower body dopant concentration, thicker oxide and Si films can be deposited (which is easier for manufacturing).

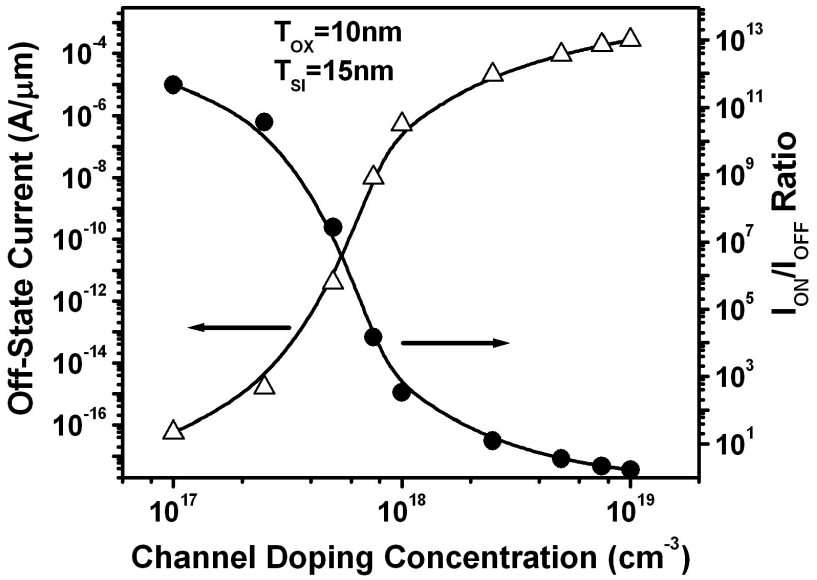

Figure 4.10. Off-state current and I_{ON}/I_{OFF} ratio of accumulation-mode MOSFETs of 2-μm gate length with variable body doping.

4.3.3 Effect of Grain Boundaries on Accumulation-Mode TFTs

Walker *et al.* [10, 11] investigated the role of a single grain boundary on the subthreshold behaviour of TFTs using a 2-dimensional device simulator. At zero or low gate biases, the potential barrier height at the grain boundary is at or close to the maximum, inhibiting carrier transport. An increase in gate bias decreases the barrier height, an effect known as gate-induced grain barrier lowering (GIGBL). The transistor shows a second turn-on, when the barrier height is decreased sufficiently to allow for thermionic emission over the barrier. This subthreshold behaviour is seen if band-to-band tunneling and band-to-trap tunneling currents are not simulated, since these tunneling leakage currents mask the GIGBL effect in fabricated TFTs [10]. In this section, the effect of a grain boundary on the electrical characteristics of an accumulation-mode MOSFET and enhancement-mode MOSFET are examined and compared.

The simulated accumulation-mode and enhancement-mode TFT structures with a single grain boundary in the centre of the channel are illustrated in Fig. 4.11. A 4-nm grain boundary region is introduced in the centre of the channel throughout the entire Si film

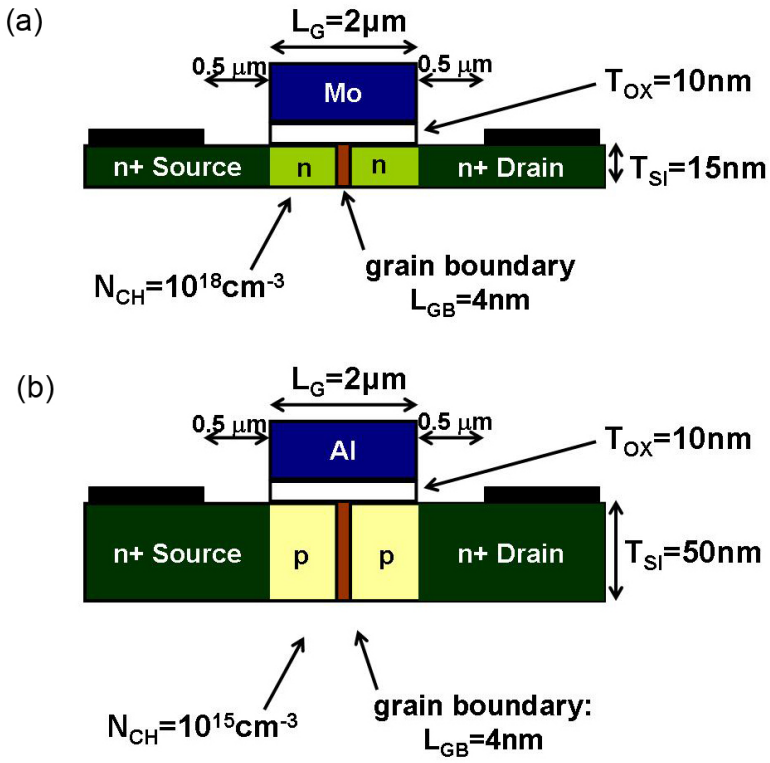

Figure 4.11. Schematic cross-section of simulated (a) accumulation-mode TFT and (b) enhancement-mode TFT with a 4-nm long single grain boundary.

depth, with a defined areal trap density. To stay consistent with Walker, the electron and hole capture rates are $C_N = C_P = 10^{-8}$cm^3/s and the trap energy level relative to the conduction band is 0.51 eV. Table 4.2 shows the parameters used in the device simulations.

The transfer characteristics for an accumulation-mode TFT and an enhancement-mode TFT with a single grain boundary in the centre of the channel are shown in Fig. 4.12 for different areal trap densities. For reference, the transfer characteristics for TFT structures with no grain boundaries are also shown (N_T=0). Similar to Walker, the band-to-band and trap-to-band tunneling currents are not simulated to isolate the effect of the grain boundary in the subthreshold region from large tunneling leakage currents. For the high areal trap densities shown, large barrier heights are seen since the both enhancement-mode TFT and accumulation-mode TFT body dopant concentrations are below N* [10]. The effect of GIGBL is seen and large increases in TFT threshold voltage are seen. In addition,

Table 4.2. Simulation parameters for single grain boundary accumulation-mode and enhancement-mode TFT devices.

Parameter	Acc TFT	Enh TFT
Channel length (L_G)	2 μm	2 μm
Silicon film thickness (T_{SI})	15 nm	50 nm
Gate oxide thickness (T_{OX})	10 nm	10 nm
Body doping (N_{CH})	$10^{18}cm^{-3}$	$10^{15}cm^{-3}$
Source/drain doping ($N_{S/D}$)	$10^{21}cm^{-3}$	$10^{21}cm^{-3}$
Gate workfunction (Φ_M)	5.0 eV	4.1 eV
Distance of grain boundary from centre of the channel	-0.9 μm to 0.9 μm	
Areal density of traps (N_T)	$10^{12}cm^{-2}$ to $10^{13}cm^{-2}$	
Trap energy level relative to conduction band (δE_c)	0.51 eV	
Capture rate for holes (C_P)	$10^{-8}cm^{-3}/s$	
Capture rate for electrons (C_N)	$10^{-8}cm^{-3}/s$	

the simulated on-state current of an accumulation-mode TFT is not greatly degraded by the grain boundary compared to an enhancement-mode TFT.

From the transfer characteristics for areal trap density $N_T = 10^{13}cm^{-2}$, the presence of a grain boundary in the centre of the channel causes large shifts in the threshold voltage. However, the threshold voltage difference (ΔV_T) is dependent on the location of the grain boundary. The threshold voltage differences between the monocrystalline and single grain boundary TFT for both accumulation-mode and enhancement-mode TFTs are shown for various grain boundary locations in Fig. 4.13. The grain boundary location is defined as the centre of the grain boundary with respect to the centre of the TFT channel. A negative x value represents a grain boundary located towards the source side; a positive value represents a grain boundary located towards the drain. For grain boundaries closer to the drain, the drain bias helps decrease the potential barrier at the grain boundary, an effect known as drain-induced grain barrier lowering (DIGBL) [12]. The enhancement-mode TFTs exhibit a greater range of threshold voltage variation with the grain boundary location. As expected, the accumulation-mode TFT exhibits less V_T increase for a single grain boundary near the source side due to the smaller potential barrier height. However, enhancement-mode TFTs

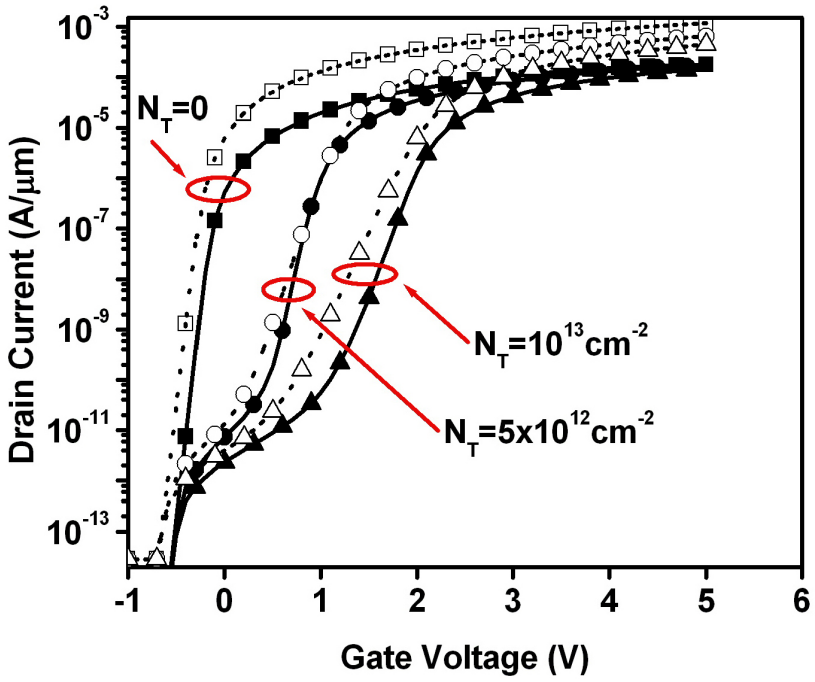

Figure 4.12. Transfer characteristics of an accumulation-mode TFT and an enhancement-mode TFT with a grain boundary midway between the source and drain with drain bias of V_D=5 V for different areal trap densities. The transfer characteristics for enhancement-mode TFTs are shown by dashed lines and open symbols; the transfer characteristics for accumulation-mode TFTs are shown by solid lines and closed symbols.

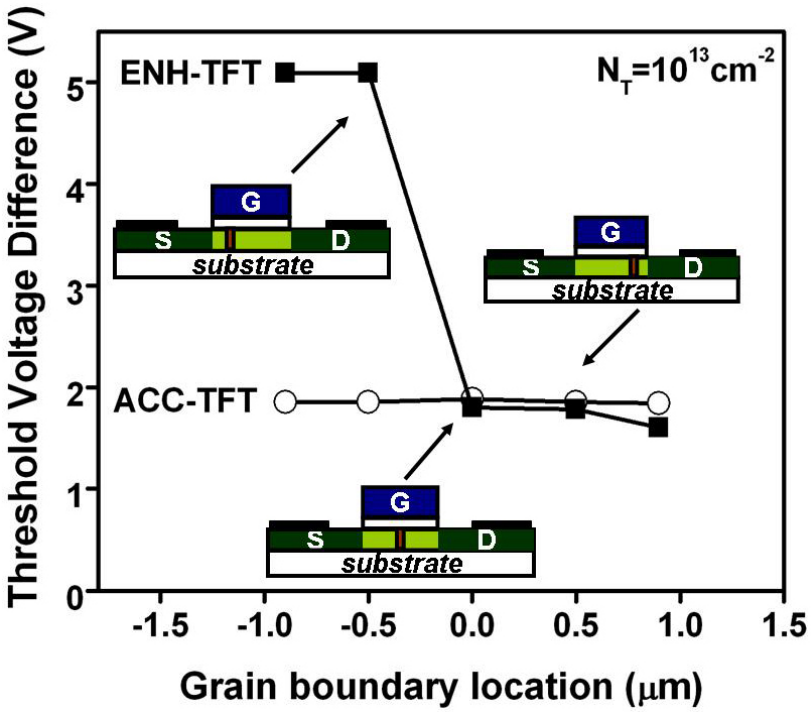

Figure 4.13. Increase in threshold voltage due to a single grain boundary.

show a smaller impact of a grain boundary for a grain boundary near the drain side. This is because a large depletion region at the drain side shields the grain boundary. In conclusion, the accumulation-mode TFT is less sensitive to grain boundary location in the channel, and hence should provide for improved uniformity in TFT performance.

4.4 Proposed Vertical Accumulation-Mode TFT Fabrication Flow

Crystallization of thin amorphous Si (a-Si) films of thickness T_{SI} <20 nm is required to fabricate accumulation-mode poly-Si TFTs. However, formation of large grains in thin Si films challenging. To obtain large poly-Si films across the transistor Si thickness (T_{SI}), a FinFET-like device structure is proposed, shown in Fig. 4.14. In this process flow, the deposited film thickness corresponds to the transistor width, not channel thickness.

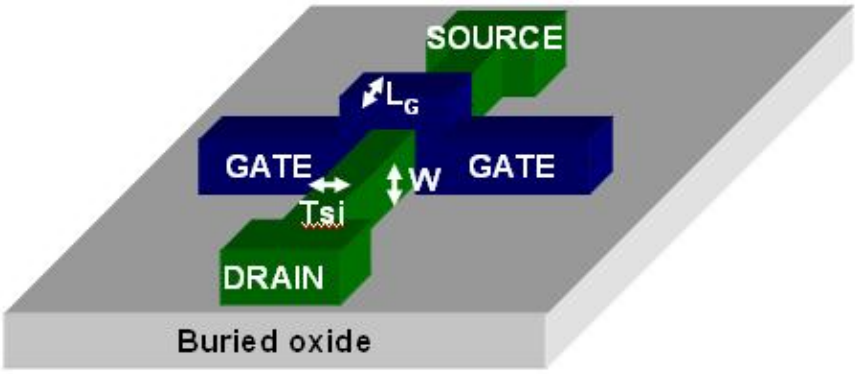

Figure 4.14. Proposed structure for accumulation-mode TFT. The transistor gate length (L_G), width (W) and thickness (T_{SI}) are labelled.

Multiple parallel fins can be used to achieve large effective transistor width. The Si film width determines the channel thickness (T_{SI}).

The proposed n-channel accumulation-mode TFT can be fabricated as shown in Fig. 4.15. A spacer lithography patterning method is suggested for TFT fin formation, as it was previously demonstrated for FinFET fabrication [13, 14]. The processing temperature is kept below 600°C for a glass-compatible process. First, a 1-μm thick SiO_2 buffer layer is deposited by low pressure chemical vapor deposition (LPCVD) on the substrate at 450°C using SiH_4 and O_2 precursor gases. Then, a 50-nm thick a-Si film is deposited at 530°C by LPCVD using SiH_4 as a precursor gas, followed by a 5-nm thick LPCVD SiO_2 capping layer. The channel is implanted with phosphorus ions to obtain an average channel doping of $N_{CH} = 10^{18}cm^{-3}$. The oxide implant capping layer is then removed by a dilute 100:1 HF liquid wet etch. The blanket 50-nm thick a-Si film is crystallized by excimer laser annealing, similar to conventional enhancement-mode TFTs to form large poly-Si grains and to activate the channel dopants (see Fig. 4.15(a)).

The active regions are patterned similarly to the FinFET fins in a spacer lithography process. A 50-nm thick poly-$Si_{0.4}Ge_{0.6}$ sacrificial layer is deposited by LPCVD at 450°C. This material is chosen for its high etch selectivity to poly-Si in a (5:1:1) H_2O:NH_4OH:H_2O_2 etchant. This sacrificial $Si_{0.4}Ge_{0.6}$ layer is then patterned and etched, to support the subsequent spacer deposition (see Fig. 4.15(b)). A 25-nm phosphosilicate glass (PSG) film

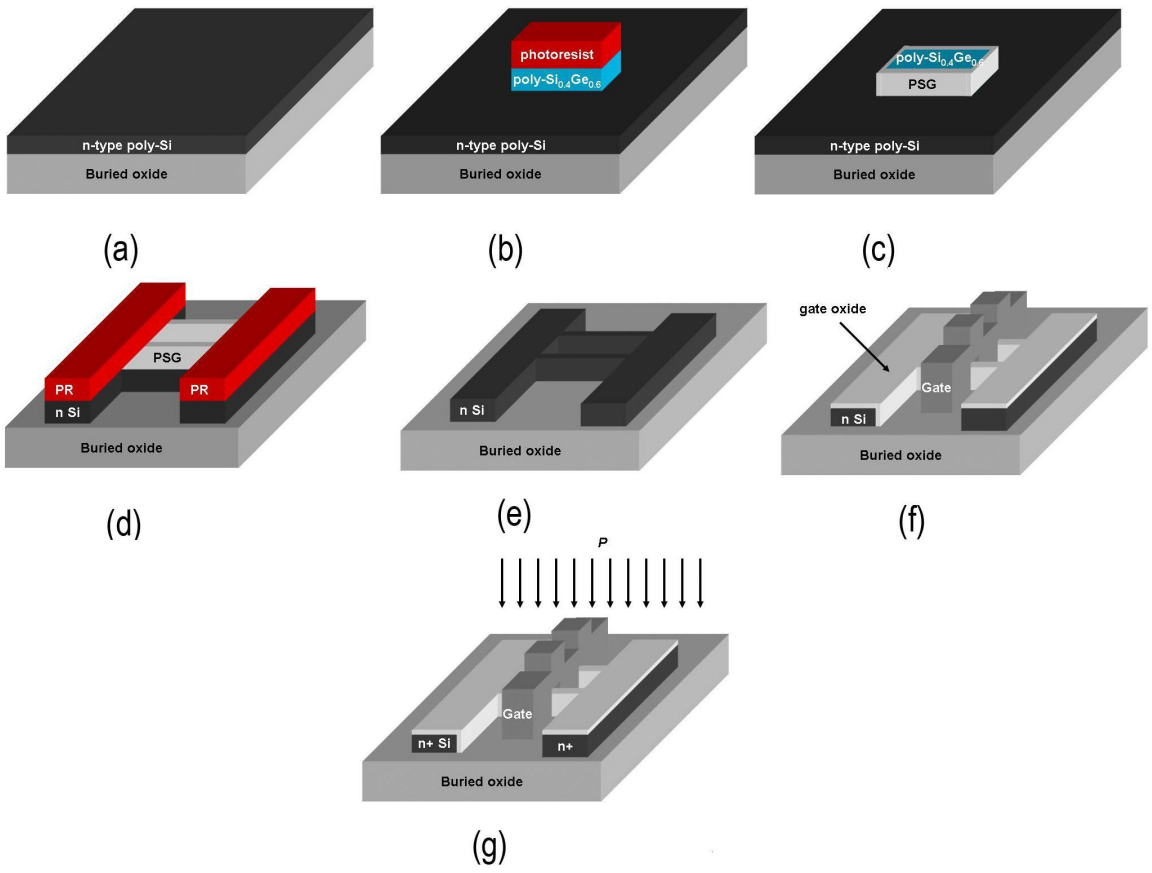

Figure 4.15. Process flow for vertical accumulation-mode TFT.

is deposited conformally, defining the critical T_{SI} thickness of the TFT. PSG is chosen due to its low etch rate during the later Si fin formation. The PSG layer is etched anisotropically, leaving spacers that will define the poly-Si fins (see Fig. 4.15(c)). The sacrificial $Si_{0.4}Ge_{0.6}$ layer is partially etched by dry etching, followed by a selective wet etch (5:1:1 H_2O:NH_4OH:H_2O_2) to fully remove the remaining sacrificial layer. The source/drain pads are defined by conventional lithography whereas the poly-Si fins are already defined by the PSG spacers; next, the poly-Si active region is patterned by dry etching (see Figs. 4.15(d) and (e)). In this process, each TFT has an even number of fins.

Next, a 10-nm thick SiO_2 gate dielectric is deposited by LPCVD at 450°C, then densified in a 550°C anneal for 4 hours in N_2. A 200-nm thick p+ *in-situ* doped poly-$Si_{0.8}Ge_{0.2}$ gate layer is deposited at 550°C by LPCVD with GeH_4, SiH_4 and BCl_3 precursor gases. The gate

is patterned and etched by RIE (see Fig. 4.15(f)). The p+ poly-$Si_{0.8}Ge_{0.2}$ gate material is chosen due to its high workfunction, conformal deposition for the highly topographic fin structure, and low process temperature. A 50-nm thick SiO_2 sidewall spacer is deposited by LPCVD at 450°C to protect the gate edge from damage during the subsequent heavily-doped n+ source and drain ion implantation. Phosphorus ions are implanted to create highly-doped self-aligned source and drain regions (see Fig. 4.15(g)), followed by an N_2 anneal at 600°C for 4 hours to activate the source and drain dopants. To finish, a 200-nm thick interlayer SiO_2 dielectric is deposited and contact holes are patterned and etched. Lastly, a 200-nm Al metal layer is sputtered, patterned and wet etched. A forming gas anneal can be performed at 400°C for 30 minutes to sinter the contacts. The device can be further annealed in hydrogen plasma at 350°C for 1 hour to passivate defects in the poly-Si grain boundaries.

4.5 Summary

The accumulation-mode TFT design utilizes a moderately-doped poly-Si active layer to reduce the impact of a grain boundary in the channel. However, due to higher body doping concentrations, thinner oxide and Si film thicknesses should be employed to achieve low off-state leakage. The novel TFT design requires precise manufacturing control of Si film thickness, dopant concentration and gate dielectric thickness to control V_T variability. Simulations with a single grain boundary in the channel show the effect of trap density on the accumulation-mode and enhancement-mode TFT subthreshold characteristics. The threshold voltage variation due to grain boundary location is worse in enhancement-mode TFT compared to accumulation-mode TFT. If a high-quality channel film can be achieved, it should be easier to manufacture uniform, high-performance TFTs using the accumulation-mode design.

A TFT fabrication process flow is proposed using spacer lithography to form sublithographic channels to achieve high-quality poly-Si films for accumulation-mode

designs. With this process, high-quality poly-Si films can be achieved using the same excimer laser crystallization methods developed for enhancement-mode TFTs while integrating thinner gate oxide and poly-Si film thicknesses. By adopting this approach, high-performance TFTs can be manufacturable with improved uniformity and reliability for system-on-glass products in the future.

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Chapter 5

Polycrystalline Silicon Tunneling Field Effect Transistors for Enhanced On-State Performance

5.1 Introduction

The tunneling field effect transistor (TFET) is considered a promising candidate for low-power applications. The TFET structure consists of a gated p-i-n diode that is reverse biased. Unlike conventional metal-oxide-semiconductor field effect transistors (MOSFETs), band-to-band tunneling current is the main carrier injection mechanism. TFETs can achieve low off-state current [1], steep subthreshold slope below 60 mV/decade [2, 3] and are less sensitive to temperature [4, 5]. However, reported TFET on-state current levels are well below that of MOSFETs with similar dimensions. Many TFET designs have been proposed to increase the band-to-band tunneling current in the on-state by using smaller bandgap materials [6], heterojunction channels [7], optimized doping profiles [8], and novel transistor structures [3, 9].

Polycrystalline silicon (poly-Si) films are rich with grain boundaries. At the grain

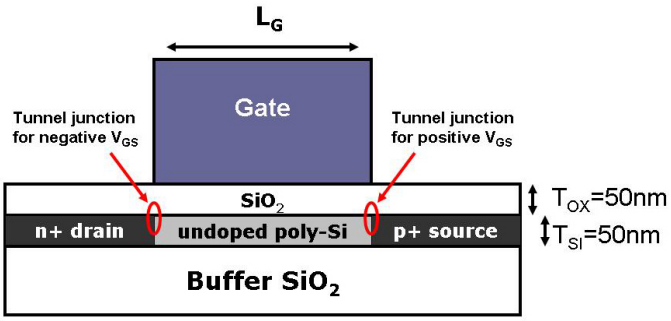

Figure 5.1. Poly-Si tunneling field effect transistor structure.

boundaries, localized charge traps exist, which lead to high leakage currents in conventional TFTs. Under high lateral electric fields, tunneling occurs not only due to band-to-band tunneling, but trap-assisted tunneling current [10]. In a poly-Si TFET structure, the trap-assisted tunneling currents can enhance the on-state current.

In this chapter, poly-Si TFETs and conventional n-type poly-Si TFT (nTFTs) are fabricated with a maximum process temperature that is compatible with glass substrates ($\leq 600°C$). The TFET operation is verified and its performance is compared to the nTFT.

5.2 TFET Operation

The poly-Si TFET device structure consists of an undoped channel. There is a highly doped n+ drain junction and a p+ source junction, with an abrupt doping profile which is essential to the operation of a TFET, as shown in Fig. 5.1.

The transistor is biased so that the p+-i-n+ diode in the channel is reverse biased (e.g. $V_{DS} > 0$ V). In the off-state (V_{GS}=0 V, $V_{DS} > 0$ V), the gate voltage is biased at 0 V. With the transistor channel under reverse bias, off-state current is suppressed (see Fig. 5.2(a)). As the gate voltage increases positively ($V_{GS} > 0$ V, $V_{DS} > 0$ V), electrons form an inversion layer in the channel and the energy band bending in the channel at the p+ source junction is steep enough to allow band-to-band tunneling (see Fig. 5.2(b)). As the gate voltage increases more negatively ($V_{GS} < 0$ V, $V_{DS} > 0$ V), holes form an inversion

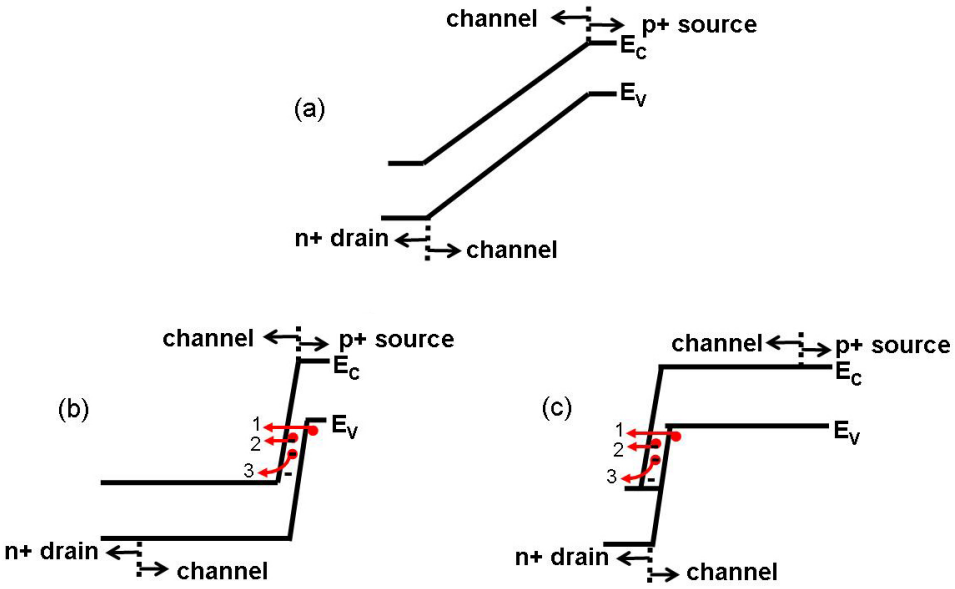

Figure 5.2. Energy band diagrams in (a) off-state, (b) on-state at the source junction with a positive V_{GS} bias and (c) on-state at the drain junction with a negative V_{GS} bias.

layer in the channel and the band bending in the channel at the n+ drain junction is steep (see Fig. 5.2(c)) so that band-to-band tunneling occurs at the drain end. Three different tunneling current paths in poly-Si TFETs are illustrated in Figs. 5.2(b) and (c), namely band-to-band tunneling, trap-assisted tunneling, and field emission from traps.

5.3 Poly-Si TFET Study

5.3.1 Process Flow

Poly-Si TFET and n-channel control TFTs were fabricated using a process with a maximum substrate temperature of 600°C. A 1-μm silicon dioxide (SiO_2) buffer oxide layer is deposited by low-pressure chemical vapor deposition (LPCVD) at 450°C. Afterwards, a 50-nm amorphous silicon (a-Si) film is deposited by LPCVD at 530°C at 300 mT with silane (SiH_4) precursor gas (see Fig. 5.3(a)). Then the a-Si film is crystallized by solid phase crystallization (SPC) using a nitrogen (N_2) anneal at 600°C for 12 hours to form the

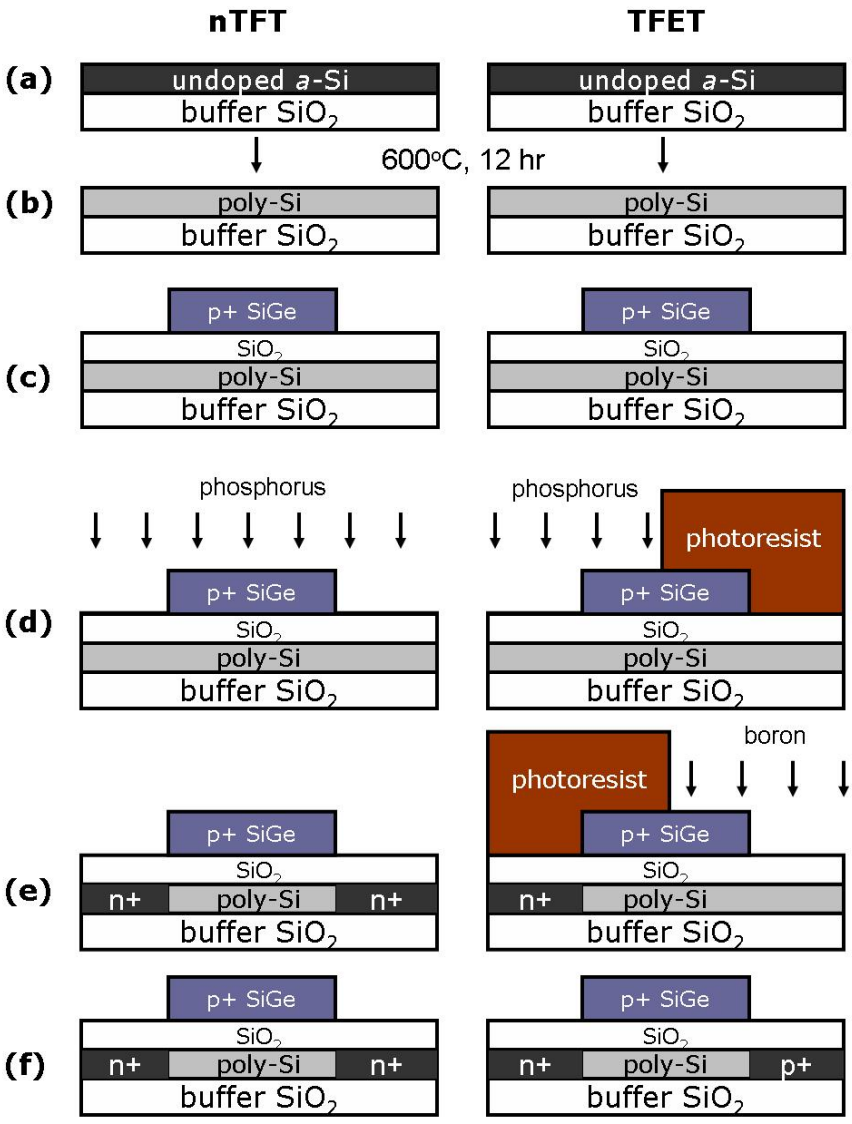

Figure 5.3. Fabrication process for control n-type poly-Si TFT (left) and poly-Si TFET (right).

poly-Si active layer (see Fig. 5.3(b)). The active region is masked by conventional optical lithography and etched by reactive ion etching (RIE).

Next, a 50-nm SiO_2 gate dielectric is deposited by LPCVD at 450°C, then densified in an N_2 anneal for 4 hours at 600°C. An *in-situ* doped p+ polycrystalline silicon-germanium (poly-$Si_{0.5}Ge_{0.5}$) gate layer is deposited at 550°C with SiH_4, germane (GeH_4) and boron trichloride (BCl_3) precursor gases, then patterned and etched (see Fig. 5.3(c)). For the wafer with TFET devices, a photoresist implant mask is then used to mask the source region. A phosphorus implant is performed at an energy and dose of 40 keV and $2 \times 10^{15}cm^{-2}$, respectively, to create highly-doped n+ regions for both TFET and nTFTs (see Fig. 5.3(d)). Then, the photoresist is ashed and a second photoresist layer is used to mask the TFET drain region. Boron is implanted in the TFET devices at energy and dose of 15 keV and $2 \times 10^{15}cm^{-2}$, respectively, to create highly-doped p+ source regions (see Fig. 5.3(e)). Afterwards, the photoresist is ashed off the TFET devices. The dopants for both TFETs and nTFTs are activated in N_2 at 600°C for 12 hours (see Fig. 5.3(f)). A 300-nm thick SiO_2 passivation layer is deposited and contact holes are patterned. An aluminum (Al) metal layer is sputter deposited and patterned for metallization. Lastly, the devices are sintered in 90%N_2/10%H_2 forming gas anneal at 400°C for 30 minutes.

5.3.2 Experimental Results

Measured transfer and output characteristics of nTFTs and TFETs are shown in Figs. 5.4 and 5.5, for L_G=2 μm and L_G=10 μm, respectively. The ambipolar operation is evident in the TFETs and can be suppressed for only one type of carrier conduction by decreasing the electric field at the unwanted tunnel junction (*e.g.* by adding a lightly-doped drain to suppress tunneling current at the drain junction). For a 10-μm channel length, the on-state current (I_{ON}) of the TFET is less than the control nTFT, by a factor of about 3×. The I_{ON} in these devices are defined as the drain current when V_{DS}=7 V and V_{GS}=10 V. As gate lengths scale, the overall TFET current levels increase. The off-state current (I_{OFF}), defined as the minimum drain current when V_{DS}=7 V, can be orders of magnitude larger than that

of the nTFTs, especially as the gate lengths scale, so that the drain has stronger capacitive coupling to the channel. Thus, the increase in current levels is caused by multiplication of channel carriers from impact ionization, or avalanche breakdown, in the kink seen in the output characteristics for L_G=2 μm at high drain biases.

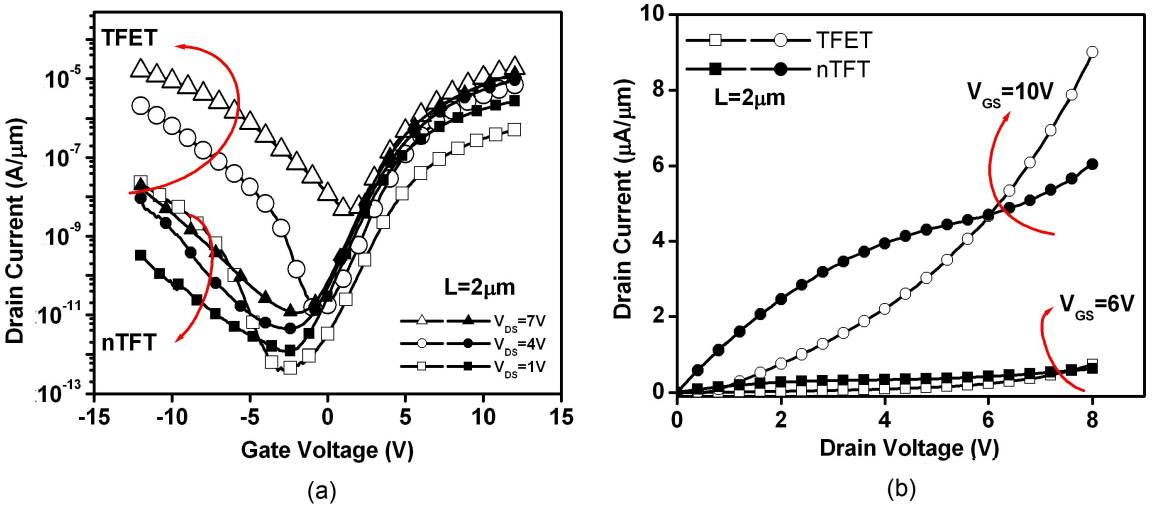

Figure 5.4. (a) Transfer characteristics for V_{DS}=1, 4, 7 V and (b) output characteristics for V_{GS}=6, 10 V for TFET (open symbols) and nTFT (closed symbols) of L_G=2 μm.

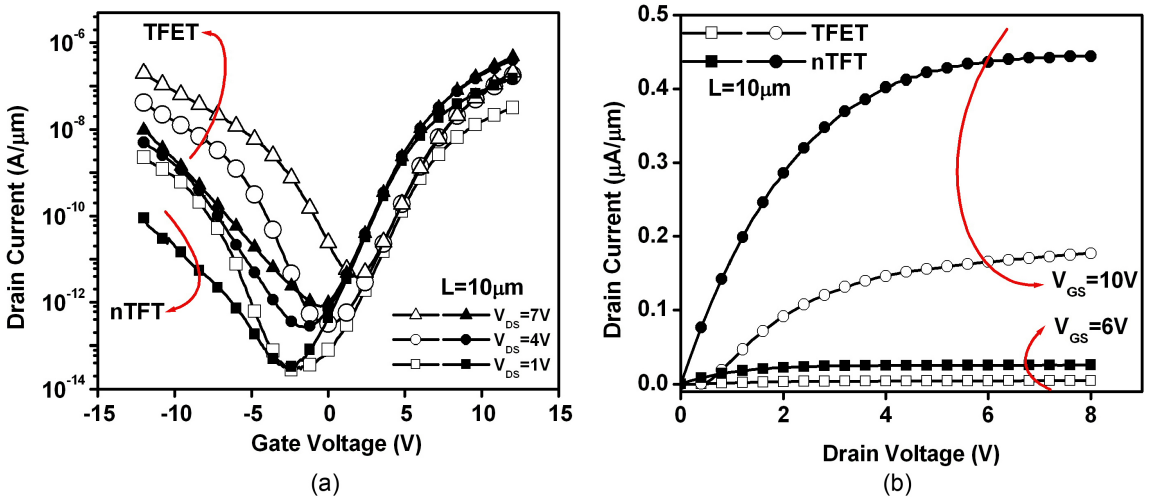

Figure 5.5. (a) Transfer characteristics for V_{DS}=1, 4, 7 V and (b) output characteristics for V_{GS}=6, 10 V for TFET (open symbols) and nTFT (closed symbols) of L_G=10 μm.

The average and standard deviation of key performance parameters are shown in Table 5.1. The threshold voltage (V_T) is defined by the constant current method, where $V_T = V_{GS}$

Table 5.1. Average and standard deviation for various device parameters for control poly-Si nTFTs and TFETs for 2 μm and 10 μm gate lengths.

	V_T (σV_T) V	S (σS) V/dec	I_{ON} (σI_{ON}) $\mu A/\mu m$	I_{OFF} (σI_{OFF}) $pA/\mu m$
nTFT (L_G=2 μm)	4.04 (0.32)	1.10 (0.02)	5.7 (0.94)	15.9 (4.6)
TFET (L_G=2 μm)	3.51 (0.42)	1.55 (0.23)	8.7 (2.14)	8740 (6260)
nTFT (L_G=10 μm)	5.14 (0.20)	1.23 (0.03)	0.51 (0.06)	9.16 (1.07)
TFET (L_G=10 μm)	6.75 (0.12)	1.27 (0.07)	0.18 (0.019)	7.06 (3.54)

when $\frac{I_D \cdot L}{W} = 10^{-7} \frac{A}{\mu m}$ at V_{DS}=7 V. The I_{OFF} and I_{ON} are defined above. The subthreshold slope (S) is extracted at the maximum slope of $\log(I_{DS})$ versus V_{GS} for V_{DS}=7 V.

Bhuwalka *et al.* has shown that the I_{ON} and V_T for nanoscale ($L_G \leq 100$ nm, $T_{OX} \leq$ 2nm) monocrystalline Si TFETs are almost independent of L_G since tunneling current dominates the TFET characteristics [13]. However, in the case of poly-Si TFETs, the on-state current has a stronger dependence on L_G compared to nTFTs, as shown in Fig. 5.6. The TFETs at shorter channels are expected to exhibit higher I_{ON} due to carrier multiplication in the channel. However, I_{ON} of long channel devices that do not exhibit impact ionization characteristics ($L_G \geq 4\mu$m) still show dependence on gate length. Thus, the on-state current is limited by the resistance in the undoped channel of the poly-Si active layer. The TFETs also exhibit larger variation in on-state current at shorter channel lengths, since impact ionization is sensitive to the location of grain boundary defects [14].

The fabricated poly-Si TFETs have gate oxide thickness of 50 nm, thicker than that of reported Si TFETs proposed for CMOS low power applications. Poly-Si TFT manufacturers are aiming to fabricate reliable, thinner gate oxide films at low temperatures for performance benefits [15]. The performance of poly-Si TFETs would also improve from gate oxide scaling. A monocrystalline Si TFET and MOSFET are simulated using the Taurus Device simulator by Synopsys Incorporated [16], with a gate length of 1-μm, Si active layer film thickness of 50-nm, for various gate oxide thicknesses. In Fig. 5.7, the S shows strong dependence on

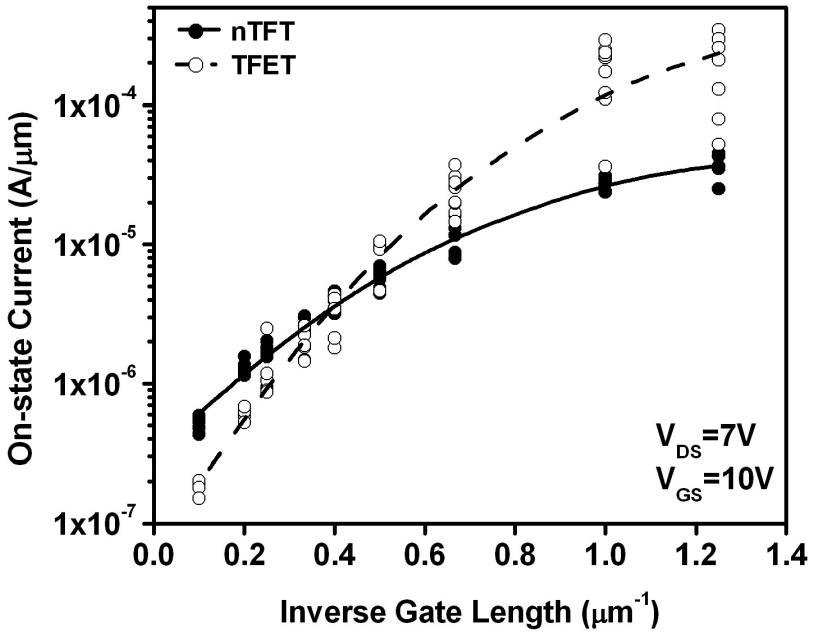

Figure 5.6. Average on-state current vs. inverse gate length of control nTFTs and TFETs.

the oxide thickness. A subthreshold slope below 60mV/decade can only be obtained in this TFET structure if $T_{OX} \leq 10$ nm.

The TFETs were subjected to hydrogen passivation at 350°C for 1 hour, which is sufficient for passivating Si dangling bonds at the grain boundaries [11, 12]. The transfer characteristics of hydrogenated and unhydrogenated TFETs are shown in Fig. 5.8, for a drain bias of 4 V. The current levels show significant increases in both on and off-state, indicating that hydrogen has successfully passivated grain boundary defects, thus decreasing channel resistance. Though the trap-assisted tunneling current should decrease after hydrogenation, this effect is not evident due to large changes in channel resistance.

5.4 Summary

Poly-Si TFETs have been fabricated with a low-temperature process. The devices exhibit ambipolar operation expected for the TFET design. Compared to conventional

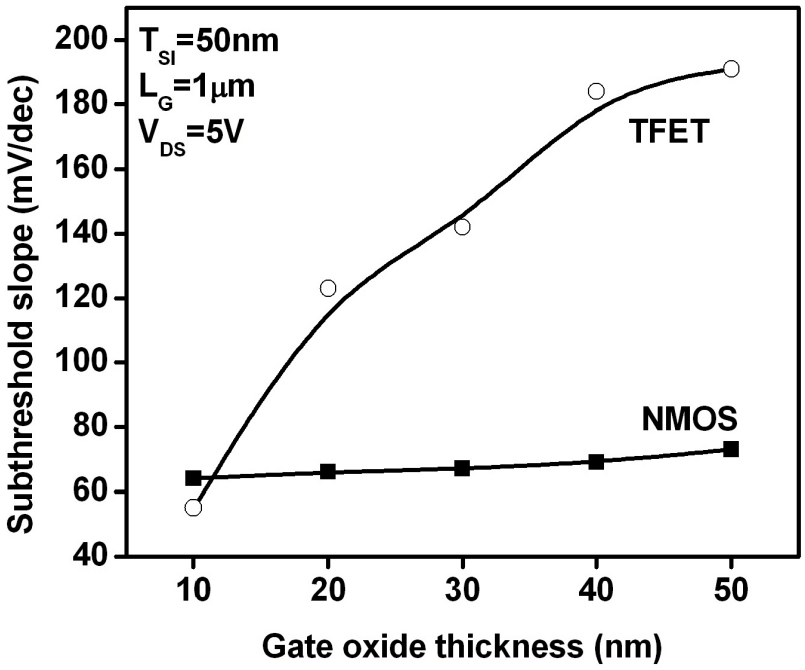

Figure 5.7. Simulation data showing subthreshold slope scaling as T_{OX} decreases for a single crystalline TFET and n-channel MOSFET.

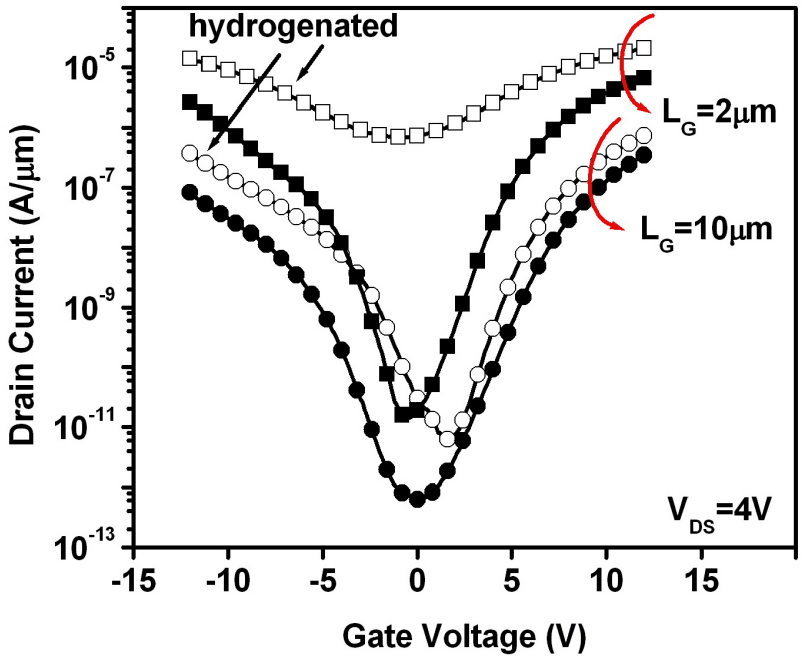

Figure 5.8. Transfer characteristics for hydrogenated (open symbols) and non-hydrogenated (closed symbols) TFET with gate length of 2-μm and 10-μm for V_{DS}=4 V.

nTFTs, enhancement in on-state current is possible for short channel TFETs. However, enhancement in I_{ON} is obtained at the cost of degraded S and higher I_{OFF}.

The current levels of the TFETs in this work, are limited by the channel resistance of the undoped channel. This is evident in the strong dependence of on-state current with the gate length, even for long-channel devices that do not exhibit impact ionization. Further increases in I_{ON} at short channel lengths occur due to carrier multiplication from impact ionization, which is shown in the output characteristics in short channel TFETs. The TFET structure would benefit from scaling down the gate length and gate oxide thickness. It is shown via device simulations that the subthreshold slope is more sensitive to T_{OX} in a TFET structure compared to conventional MOSFETs.

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Chapter 6

Low-Thermal-Budget Materials for Integrated Microelectromechanical Systems

6.1 Introduction

The monolithic integration of microelectromechanical systems (MEMS) with complementary metal-oxide-semiconductor (CMOS) electronics is beneficial for enhancing system functionality and performance, and lowering packaging cost. A MEMS-last approach is desirable because it allows for the electronics to be manufactured using a standard CMOS process in a semiconductor foundry. However, it imposes severe constraints on the thermal process budget for MEMS fabrication. For a foundry 0.25-μm CMOS technology, the maximum thermal budget is limited to 425°C for 6 hours or 450°C for 1 hour [1].

Polycrystalline silicon (poly-Si) is the conventional structural material used for surface-micromachined MEMS devices. Typically formed by low-pressure chemical vapor deposition (LPCVD) at temperatures above 600°C followed by annealing at temperatures above 900°C, it is not suited for post-CMOS integration of MEMS.

Potential materials for low-temperature structural films include polycrystalline silicon-germanium (poly-$Si_{1-x}Ge_x$, $x \leq 0.6$), since these films can be formed at much lower temperatures and therefore has been investigated recently for MEMS applications [2]. However, low-thermal-budget poly-$Si_{1-x}Ge_x$ films have large strain gradient [3] which is undesirable for large micromachined structures such as those used in inertial sensors.

In this chapter, metal and poly-Si films formed at process temperatures $\leq 350°C$ are investigated as potential structural materials for low-thermal-budget MEMS devices. The mechanical properties such as Young's modulus (E), strain gradient (Γ) and residual stress (σ) are investigated to assess their potential for MEMS application.

6.2 Extraction of Mechanical Properties

Residual stress and non-zero strain gradient each can adversely affect the operation of MEMS devices. Clamped-clamped beams with high compressive stress can buckle upon release, whereas beams with high tensile stress can fracture. Ideally, residual stress should be zero, or slightly tensile (< 100 MPa), to avoid any significant effect on the elastic spring constant of a beam. A strain gradient (change in stress through the thickness of the beam) can result in significant out-of-plane deflection which in the best case affects the beam actuation voltage and in the worst case causes device failure; hence it should be minimized. In this section, the methods for extracting these mechanical properties of thin films are described.

6.2.1 Residual Stress Measurement by Wafer Curvature

The residual stress of thin films can be extracted from wafer curvature measurements using a Tencor Flexus-2320 thin film stress measurement tool. This tool measures the substrate radius of curvature before and after a blanket thin film deposition on one side of the wafer. Using the Stoney formula [4], $\sigma = \frac{E}{1-\nu}\frac{h^2}{6Rt}$, the film residual stress σ is calculated knowing the Young's modulus (E) and Poisson's ratio (ν) of the substrate,

substrate thickness (h), film thickness (t) and measured radius of curvature due to the film deposition (R). This method is beneficial for measuring σ due to quick fabrication throughput.

6.2.2 Mechanical Properties Extraction using Analytical Model

Electrostatic pull-in voltage (V_{PI}) measurements of cantilever and clamped-clamped beams test structures are an excellent method to extract the mechanical properties (E, Γ, σ) of potential structural films. Voltage is applied to a moveable cantilever or clamped-clamped beam while keeping a stationary bottom electrode or plane grounded. At a critical voltage (V_{PI}), the beam pulls into the ground plane, creating a current short. This voltage is dependent on the beam geometry, structure and material properties. Using the sharp and accurate V_{PI} measurements, extraction of Young's modulus and residual stress has been experimentally verified by Osterberg *et al.* [5]. The schematics of the cantilever and clamped-clamped beam test structures are shown in Fig. 6.1. A plan view scanning electron micrograph (SEM) of a fabricated cantilever two-terminal relay (of 1-μm width and 20-μm length) is shown in Fig. 6.2.

Analytical models developed by Kam *et al.* [6] incorporate the effect of strain gradient for cantilever beams and the effect of residual stress for clamped-clamped beams on V_{PI} in the Euler-Bernoulli beam equations. In the case of two-terminal switches where the beam and bottom electrode have different workfunctions (Φ), the workfunction difference ($\Delta\Phi = \Phi_{beam} - \Phi_{electrode}$) is incorporated in the pull-in voltage term. In other words, the V_{PI} term in the analytical model is replaced with $V_{PI} + \Delta\Phi/q$.

Young's modulus and strain gradient can be extracted from measured values of V_{PI} when plotted as a function of cantilever beam length (L). From simple beam theory (not accounting for the presence of a strain gradient), V_{PI} is proportional to $\frac{1}{L_2}$: $V_{PI} = \sqrt{\frac{8Eh^3g^3}{27\epsilon_0 L^4}}$, where h is the thickness of the beam, g is the thickness of the air gap and ϵ_0 is the vacuum permittivity. Following the methodology in [5], the value of Young's modulus can be extracted from the slope.

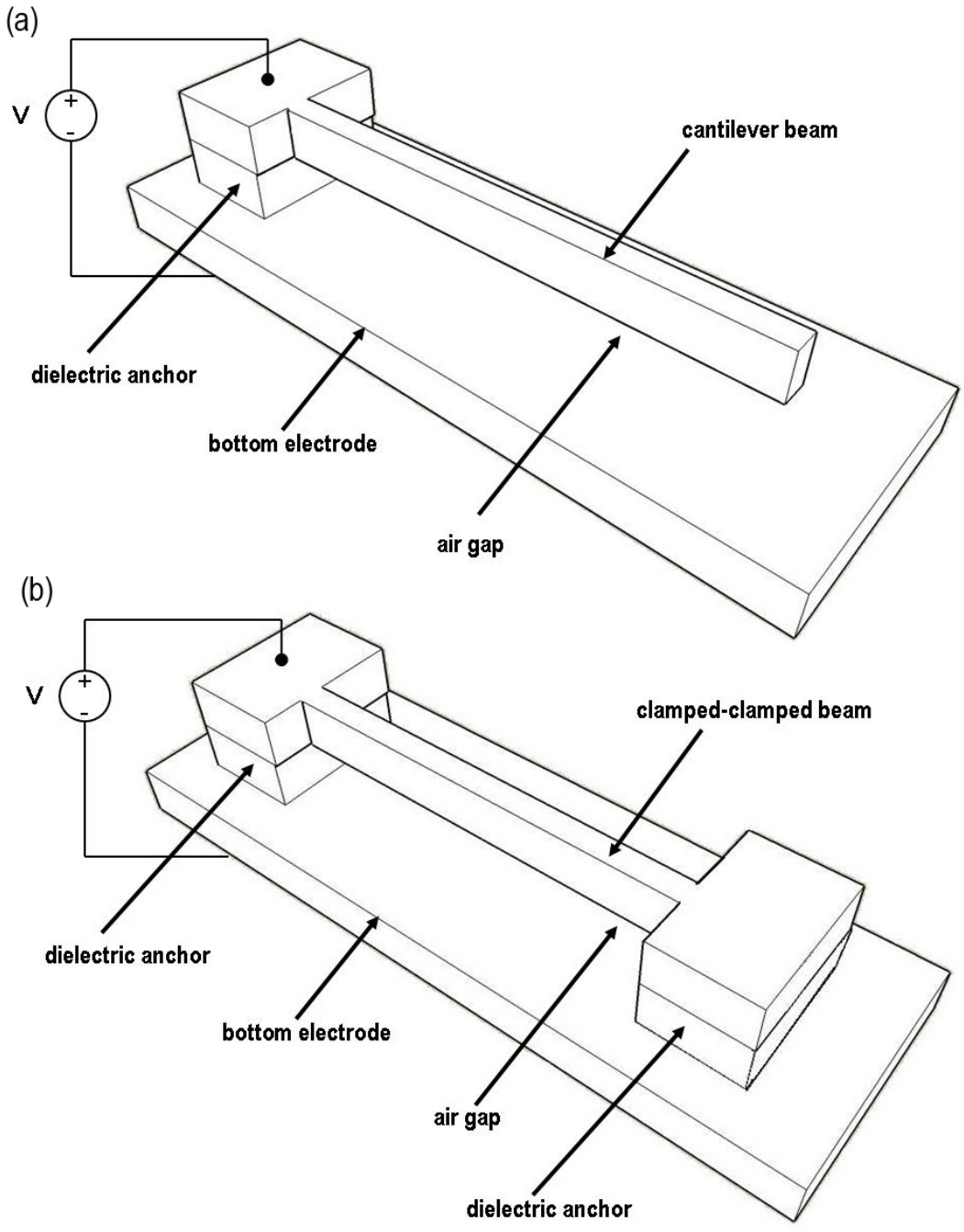

Figure 6.1. Schematics of two-terminal (a) cantilever beam and (b) clamped-clamped beam relays.

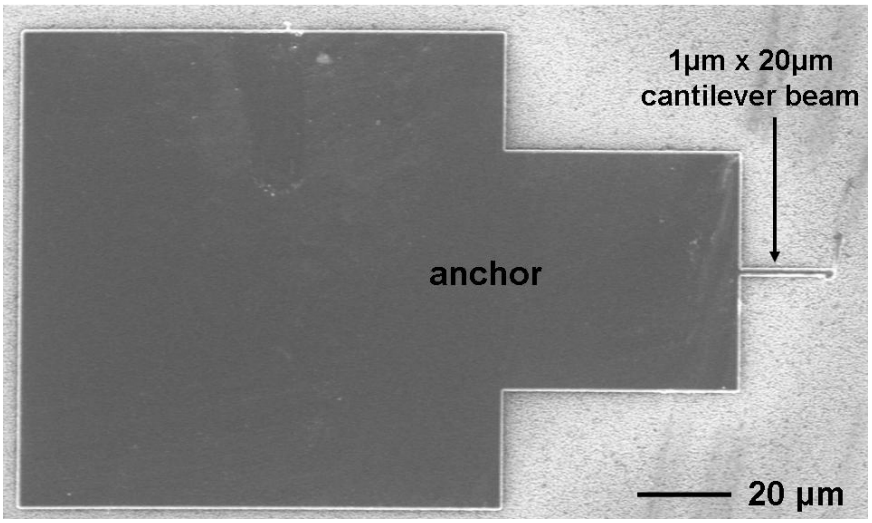

Figure 6.2. Plan view scanning electron micrograph of an unreleased 1-μm $\times$ 20-μm cantilever beam.

Accounting for a non-zero strain gradient Γ, V_{PI} for a cantilever beam is given by the following equation [6]: $V_{PI} = 1.2965\sqrt{\frac{2EIg^3}{\epsilon_0 WL^4}} + 0.64825\Gamma\sqrt{\frac{2EIg}{\epsilon_0 W}}$ where $I = \frac{h^3 W}{12}$ is the area moment of inertia. Since V_{PI} is a linear function of $\frac{1}{L^2}$, Γ can be extracted from the slope and y-intercept of the least-squares linear fit of this equation.

Residual stress affects the pull-in voltage of a clamped-clamped beam according to the following equation [6]: $V_{PI} = \sqrt{3.567\frac{\sigma h g^3}{\epsilon_0 L^2} + 11.70\frac{Eh^3 g^3}{\epsilon_0 L^4}}$. Note that V_{PI}^2 is a quadratic function of $\frac{1}{L^2}$), and σ can be extracted by the best fit to this equation.

Using this method, two-terminal switches of high-temperature as-deposited poly-Si and low-temperature as-deposited poly-$Si_{0.4}Ge_{0.6}$ of 1-μm thickness were fabricated on $\sim$ 500-nm thick sacrificial SiO_2. The strain gradients of the poly-Si and poly-$Si_{0.4}Ge_{0.6}$ films are $\Gamma_{Si} = -2.25 \times 10^{-5}\mu m^{-1}$ and $\Gamma_{SiGe} = 3.74 \times 10^{-4}\mu m^{-1}$, respectively, which are confirmed by optical interferometry [6].

6.3 Candidate Structural and Sacrificial Materials

The candidate structural materials considered are metal films and poly-Si films that are formed at temperatures $\leq$ 350°C. In this study, the mechanical properties of the

following four metals are investigated: Nickel (Ni), Titanium (Ti), Titanium nitride (TiN) and Aluminum (Al) are investigated. Poly-Si films crystallized by aluminum-induced-crystallization (AIC) are also considered.

In this study, the candidate sacrificial material is released by a dry chemical etch. The surface tension from the liquid in a wet chemical etch processes can cause stiction, and the adhesion forces between the beams and ground plane can be too strong to overcome. Thus, two dry chemical release processes are considered: hydrofluoric acid in vapor phase (HF vapor) and xenon difluoride (XeF_2). Both processes exhibit slow etch rates for some of the candidate structural materials [7]. Since the two terminal relay fabrication process requires an insulating sacrificial layer, SiO_2 is an excellent candidate that can be released by HF vapor. XeF_2 dry releases can etch Molybdenum (Mo) and Si films, but Mo and monocrystalline or polycrystalline Si films are too conductive to act as the sacrificial layer. However, amorphous Si (a-Si) is a good candidate as a sacrificial material due to the quick etch rates in XeF_2 and high reported resistivities (10^8 Ωcm to 10^{12} Ωcm) [8, 9]. The choice of sacrificial layer is determined by two requirements: the structural material must be etch resistant to the release process and the structural material etching must be selective to the sacrificial material.

To assess the good pairings of structural and sacrificial materials, the etch rates of these materials are measured using a Lam Research Corporation Autoetch 690 reactive ion etcher. A standard chlorine-based etch is performed at a pressure and power of 250 mT and 250 W, respectively. The gas flows in this recipe are 50 sccm of boron trichloride (BCl_3), 50 sccm of nitrogen (N_2), 30 sccm of chlorine (Cl_2) and 20 sccm of chloroform ($CHCl_3$). The etch rates in the of various candidate materials are shown in Table 6.1. Since a-Si etches faster than any of the candidate structural materials, SiO_2 is determined to be the best candidate sacrificial material.

Table 6.1. Etch rates of candidate structural and sacrificial materials for a chlorine-based etch recipe. The etch is performed at a pressure of 250 mT, power of 250 W and gas flows for Cl_2, N_2, BCl_3 and $CHCl_3$ of 30 sccm, 50 sccm, 50 sccm and 20 sccm, respectively.

Structural Materials	Etch Rate (nm/min)
Aluminum	254
Nickel	142
Titanium Nitride	135
Sacrificial Materials	**Etch Rate (nm/min)**
Amorphous Silicon	825
Thermally grown Silicon dioxide	59
LPCVD Silicon dioxide	176

6.4 Sputtered Metals for MEMS Structural Layer

Physical vapor deposition (PVD) of metallic films fulfill the low-thermal-budget requirements for integrating MEMS on top of CMOS electronics. Sputtering is a PVD technique that is commonly used for metal deposition in microelectronics and can easily be integrated with post-CMOS processing. A schematic of a parallel-plate direct current (DC) sputter deposition chamber is shown in Fig. 6.3, where a solid metal source (the target) is biased by a negative electrode (the cathode) and the wafer sits on a grounded electrode (the anode). An inert gas, typically Argon (Ar), flows in the chamber at low pressures. When a DC voltage is applied across the two electrodes, a plasma is created containing some high-energy positive Ar ions and free electrons. The positive Ar ions are accelerated towards the cathode and dislodges some atoms from the target. These dislodged atoms travel through the plasma in vapour phase and strike the wafer surface, where they condense and form a deposited film [10].

Since ultra high vacuums systems and high purity targets are available, the resulting films exhibit high purity of similar quality as the targets. Fast deposition rates and good uniformity are achievable while keeping the sputtering temperatures well below the melting temperatures of the metal films themselves. By changing the deposition parameters such as pressure and temperature, the microstructure of the sputtered films can be controlled. To

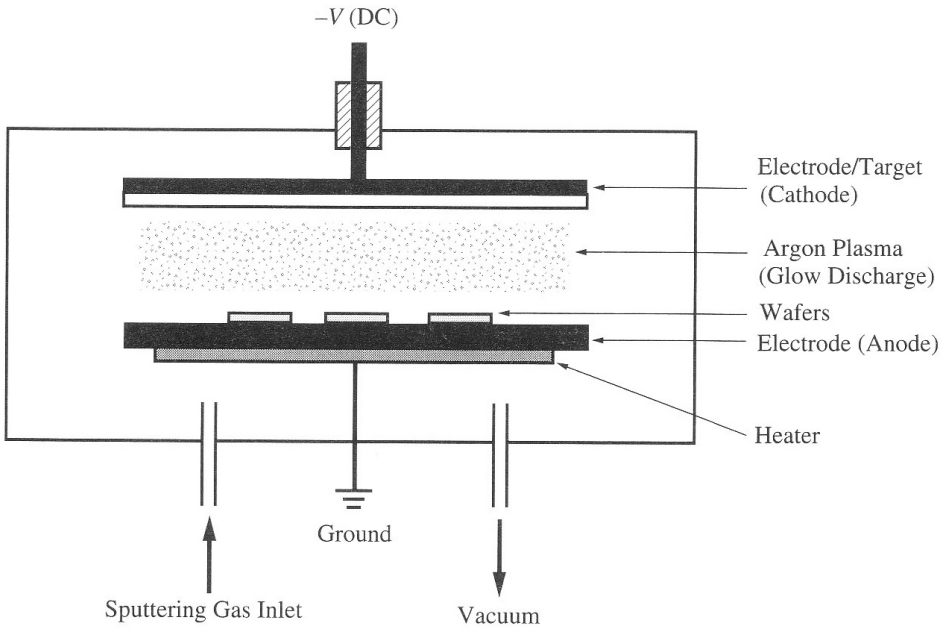

Figure 6.3. Schematic of a parallel plate DC sputter deposition chamber [10].

form a compound or alloy film, reactive sputtering can also be employed. In this process, a metal target is sputtered in the presence of a reactive gas such as oxygen (O_2) or nitrogen (N_2) with the inert working gas (such as Ar). The plasma breaks the O_2 or N_2 molecules into atomic oxygen or nitrogen which reacts with the metal and forms a compound or alloy film on the target and wafer surfaces (*e.g.* Ti target and N_2 gas produce a TiN film). The properties of sputtered thin film are determined significantly by deposition conditions such as total pressure (and partial pressures in the case of reactively sputtered films), substrate temperature and deposition temperature [10, 11].

6.4.1 Deposition Parameters for Sputtered Metal Films

A Novellus M2i DC magnetron sputter deposition system (base pressure $\sim 10^{-8}$ Torr) is used to deposit Al, Ti and TiN films using high purity Al or Ti targets. The chuck temperature during deposition can vary from 20°C to 400°C. TiN films are deposited using a reactive sputtering process with a constant total process pressure. The Ni films are deposited using a CPA 9900 DC magnetron sputtering tool where the chuck temperature

Table 6.2. Sputtering conditions for candidate structural metal films.

Metal	Total Pressure (mT)	Temperature (°C)	Power (kW)	Deposition Rate (Å/s)
Aluminum	4	25 - 250	1.8	40
Nickel	15	25	1.5	38
Titanium	2.75	300	0.9	24
Titanium nitride	8.4 N_2 partial pressure: 1.4 - 7.3	25 - 400	1.2	∼5

remains at room temperature during the sputtering process. The sputtering deposition parameters for the four metals are summarized in Table 6.2.

6.4.2 Residual Stress of Sputtered Metal Films

The residual stress of PVD metals is known to be dependent on the grain size, grain geometry, crystallographic orientation and film thickness [12, 13, 14]. The stress in thin films can be attributed to two sources: intrinsic stress and thermal stress. Intrinsic stress originates during film growth and depends on the grain structure and crystallographic orientation of the film. Thermal stress originates if the film is deposited or annealed at high temperatures, due to the difference in thermal expansion coefficients between the thin film and thick substrate. The thermal stress (σ_{th}) is calculated by $\sigma_{\mathrm{th}} = \mathrm{E_f}(\alpha_{\mathrm{f}} - \alpha_{\mathrm{s}})(\mathrm{T} - \mathrm{T_0})$, where $\mathrm{E_f}$ is the Young's modulus of the film, α_{f} and α_{s} are the film and substrate thermal expansion coefficients, respectively, T is the high deposition temperature and $\mathrm{T_0}$ is the temperature that the sample has cooled down to [12, 13].

Thornton's zone model [15] shows the dependence on the metal microstructure on the Ar pressure and parameter $\frac{\mathrm{T}}{\mathrm{T_m}}$, where T and $\mathrm{T_m}$ are the film deposition temperature and melting point temperature in Kelvin, respectively. As shown in Fig. 6.4, the film grain structures are classified in one of four zones, labelled 1, T, 2 and 3. In zone 1, thin films consist of tapered crystals separated by voids and are too porous to support stress. Zone T films consist of dense fibrous structures that can form large intrinsic stress. Zone 2 films

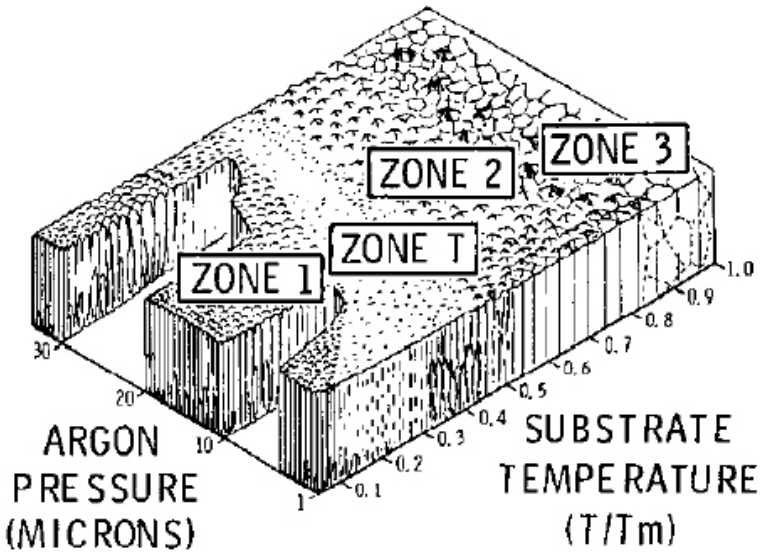

Figure 6.4. The zone model for films deposited by sputtering. The film structures for sputtering pressure and temperatures are illustrated [15].

comprise of columnar grain structures separated by distinct grain boundaries. Lastly, zone 3 exhibits large grain structures due to film recrystallization during deposition. Sputter films tend to fall in zones T or 2 [13, 15].

The effect of sputtering temperature on average residual stress of 500-nm thick Al films is shown in Fig. 6.5. The increase of residual stress with higher deposition temperature is expected due to increasing thermal stress. However, depositions where the parameter $\frac{T}{T_m} > 0.5$, corresponds to zone 2 columnar grain structures, which may explain the jump in residual stress at Al deposition temperature of 250°C.

The effect of Al film thickness on average residual stress is shown in Fig. 6.6 for deposition temperatures of 25°C and 250°C. Very low residual stress, which is desirable, can be achieved by deposition of Al at room temperature since the thermal stress component does not exist in these films.

The Ni film depositions are performed at room temperature, so the residual stress excludes a thermal stress component. The effect of Ni film thickness on residual stress is shown in Fig. 6.7. Ni films of thickness greater than 100-nm exhibit tensile stress between

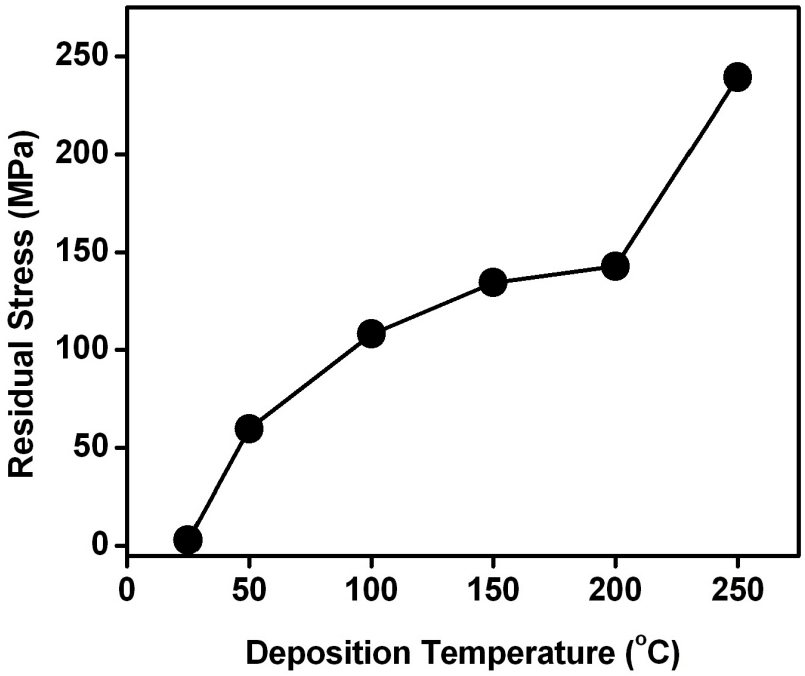

Figure 6.5. Effect of deposition temperature on average residual stress for 500-nm thick Al films.

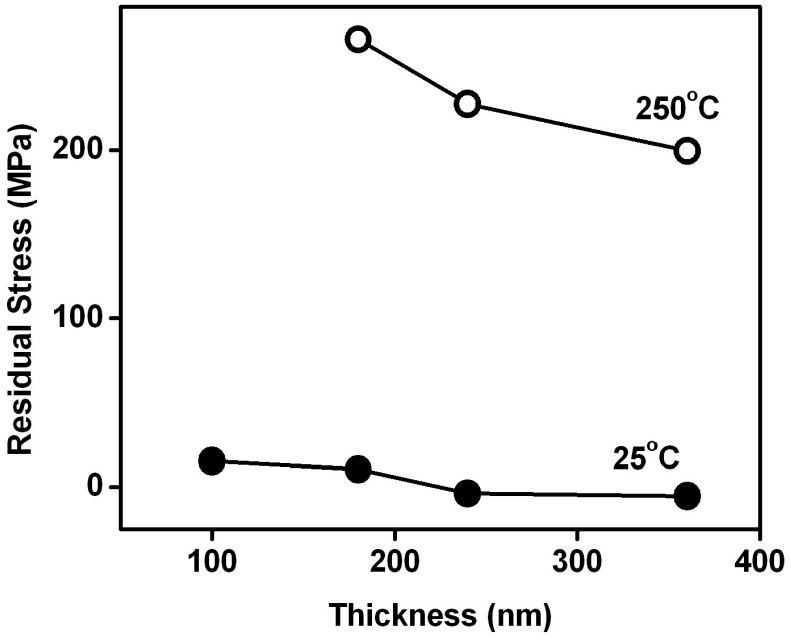

Figure 6.6. Effect of Al film thickness on average residual stress for deposition temperatures of 25°C (lower curve) and 250°C (upper curve).

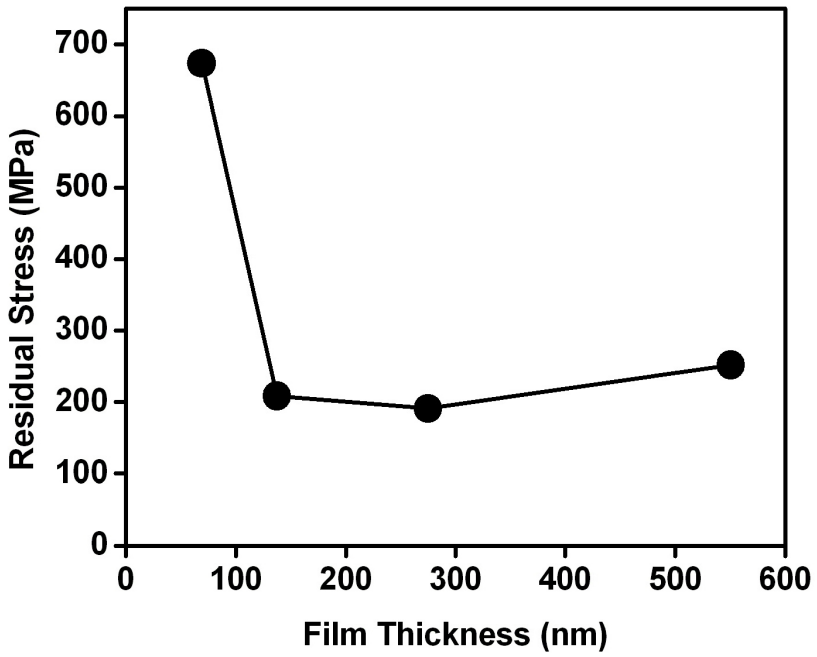

Figure 6.7. Effect of Ni film thickness on average residual stress.

190 to 260 MPa which is consistent with previous reports for Ar process pressure of 15 mT [13]. However, the thin 70-nm Ni film exhibits very large residual stress (673 MPa).

TiN films have been proposed as an excellent MEMS structural material due to its low surface adhesion forces by Seneviratne *et al.* [16]. They demonstrated that as-deposited TiN films exhibit large compressive stress, which can become tensile with a high temperature anneal ($\sim 500°C$). However, anneals at this temperature are incompatible with post-CMOS processing. Thus, the effects of deposition temperature and Ar and N_2 gas flow rates are investigated to minimize compressive stress in TiN films. In Fig. 6.8 [17], the effect of deposition temperature on average residual stress of 250-nm thick TiN films is shown. The gas flow rates of Ar and N_2 during this deposition are 50 sccm and 65 sccm, respectively, corresponding to Ar partial pressure of 3.65 mT and N_2 partial pressure of 4.75 mT. These ratios translate to a 1:1 titanium to nitrogen stoichiometry. The least negative compressive residual stress is demonstrated at deposition temperatures of 300°C. In Fig. 6.9 [18], the influence of the Ar and N_2 gas flow rates on residual stress of 120-nm thick TiN films is shown. The total pressure is kept constant at 8.4 mT while the ratio of Ar to N_2 partial

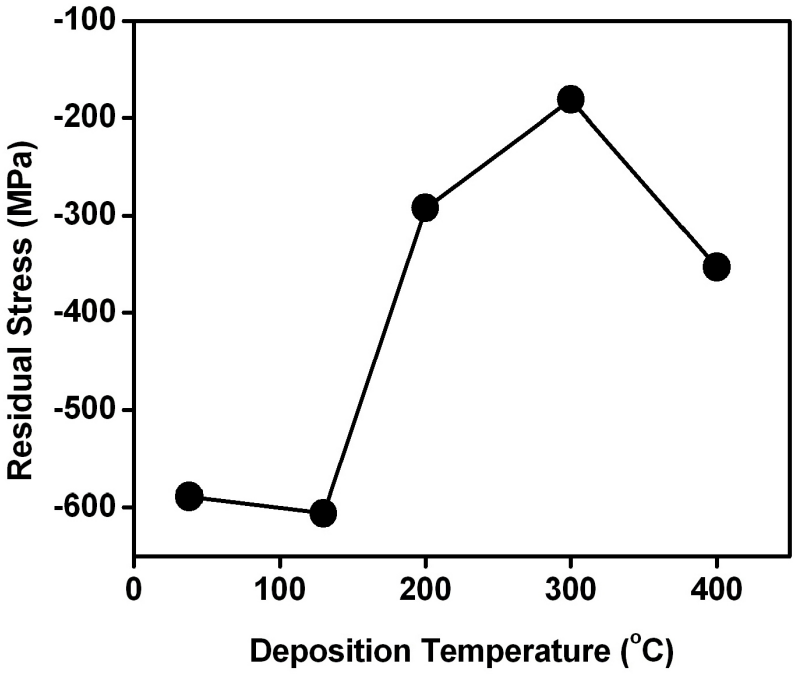

Figure 6.8. Effect of deposition temperature on average residual stress of 250-nm thick TiN films [17].

pressures is varied by adjusting gas flow rates. The deposition temperature is kept at 300°C for all samples. A Ti sample with the same total pressure (where Ar and N_2 partial pressures of 8.4 mT and 0 mT) is included as a reference. As expected, the Ti and TiN films exhibit compressive stress. The residual stress of TiN becomes less compressive with decreasing nitrogen content. Vaz *et al.* reports minimum residual stress in TiN films with 30% nitrogen content, which occurs when N_2 partial pressure is 5% of the total process pressure in their sputtering system [19]. Further characterization of the atomic % of nitrogen of the TiN films in this study is required to validate the results.

Of the four metals investigated, only Al and Ni films exhibit tensile stress. Ti and TiN films exhibit compressive stress despite varying the deposition conditions. Table 6.3 shows a comparison of the optimized residual stress of 150-nm thick films. Only the Al sample exhibits stress below 100 MPa. Further extraction of the Young's modulus and strain gradient in Al films is performed by the analytical method described in section 6.2.2 to evaluate its potential as a structural material.

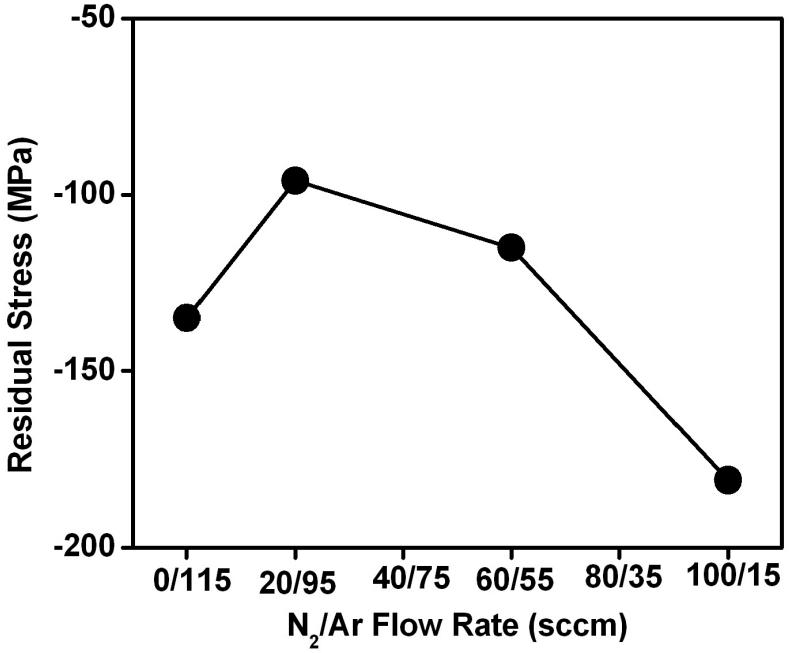

Figure 6.9. Effect of N_2 to Ar gas flow ratios on average residual stress of 120-nm thick Ti and TiN films [18].

Table 6.3. Comparison of residual stress for 200-nm thick metal films.

Aluminum	10 MPa	tensile
Nickel	209 MPa	tensile
Titanium	-113 MPa	compressive
Titanium Nitride	-96 MPa	compressive

6.4.3 Mechanical Properties of Aluminum Thin Films

Two-terminal Al relays were fabricated on heavily n-type doped Si(100) wafer substrates with a 130-nm thick SiO_2 sacrificial layer and a 475-nm thick Al structural layer. Two samples were fabricated with Al beams deposited at 25°C and 100°C. The beams were released by a timed 15-minute HF vapor etch. The pull-in voltages of 1-μm wide cantilever beams of various lengths are plotted in Fig. 6.10. The workfunctions of Al and n+ doped Si are $\sim$ 4.1 eV, so no additional term is added to the pull-in voltage values. The Young's modulus and strain gradient are extracted from the slope and y-intercept of the least-squares linear fit. The extracted Young's modulus of Al thin films are lower than reported bulk values ($E_{bulk} \sim 70$ GPa). The difference in thin film and bulk Young's modulus values has been attributed possibly to Ar incorporation in sputtered films, which has been shown to decrease the Young's modulus in thin films [20]. The Al beams deposited at room temperature exhibit large strain gradient ($\Gamma_{25°C} = 9.2 \times 10^{-3} \mu m^{-1}$) which decreases slightly for higher deposition temperature of 100°C ($\Gamma_{100°C} = 2.9 \times 10^{-3} \mu m^{-1}$).

The residual stress is extracted from pull-in voltage measurements of 1-μm wide clamped-clamped beams of various lengths, as shown in Fig. 6.11. The extracted values are 46 MPa and 58 MPa for Al deposited at 25°C and 100°C, respectively. The measured values from wafer curvature measurements are shown by the dashed lines for comparison.

From the four metals investigated, none have both desirable low tensile residual stress and low strain gradient compared to low-temperature poly-SiGe films. These metals cannot be used to form large MEMS structures such as inertial sensors but may be used for smaller MEMS devices such as nanoscale relays and memories.

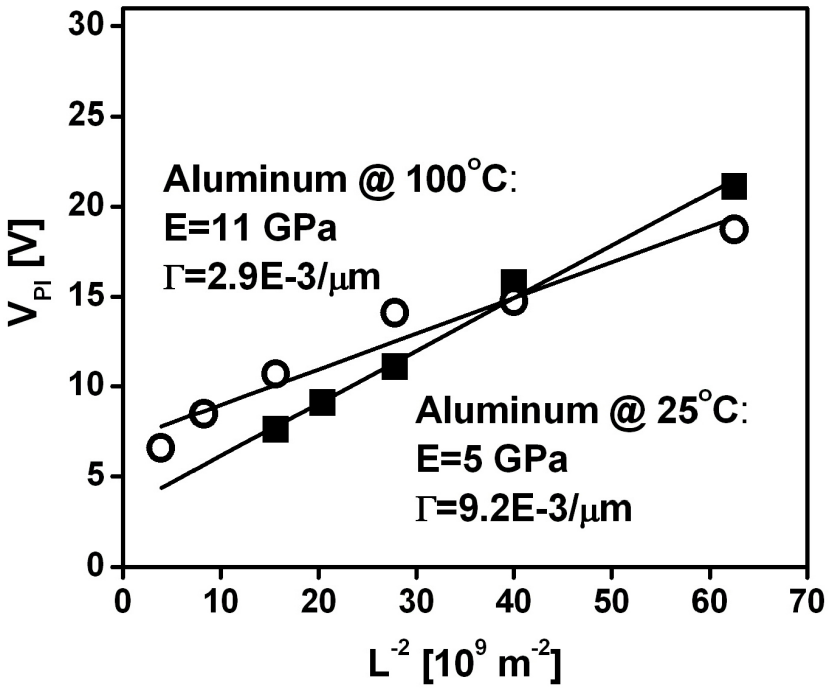

Figure 6.10. Young's modulus (E) and strain gradient (Γ) extraction from pull-in voltage measurements of Al cantilever beams of various lengths, deposited at 25°C (closed symbols) and 100°C (open symbols).

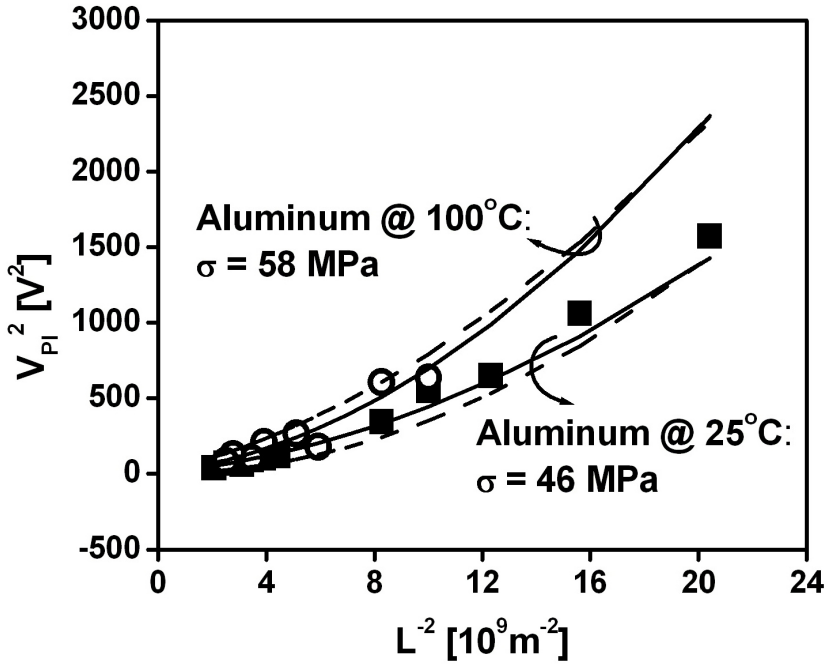

Figure 6.11. Residual stress (σ) extraction from pull-in voltage measurements of Al clamped-clamped beams deposited at 25°C (closed symbols) and 100°C (open symbols). The dashed curves represent expected values from wafer curvature measurements.

6.5 Aluminum-Induced Crystallization of Poly-Si for MEMS Structural Layer

Poly-Si films can be formed at temperatures well below 600°C by metal-induced crystallization [21]. Hiraki [22] proposed a "screening model" to explain why the crystallization temperature of Si decreases when it is in contact with certain metals: screening (by mobile electrons in the metal) of the Coulomb interaction responsible for covalent bonding destabilizes Si covalent bonds and hence lowers the energy required to break the bonds, which aids the transformation of the Si from amorphous phase to polycrystalline phase. In the aluminum-induced crystallization (AIC) process used in this work, an Al layer and a-Si layer are deposited sequentially. When this layer stack is heated (to 350°C), the a-Si intermixes with the Al and agglomerates, resulting in the nucleation and growth of Si grains within the Al layer. As the crystallization proceeds, the Al is displaced, until a complete layer exchange has occurred. The following parameters have been found to influence the quality of the AIC poly-Si layer: the a-Si to Al layer thickness ratio, the AIC anneal temperature, the Al layer microstructure, and the interface between the Al and a-Si layers [23, 24]. By using Al-2%Si rather than Al to promote grain nucleation, the crystallization temperature can be lowered to 325°C [25].

6.5.1 Formation of Polycrystalline Silicon Films

A Novellus M2i DC magnetron sputter deposition system was used to deposit and anneal thin-film stacks of Al-2%Si and a-Si layers, without breaking vacuum, to form poly-Si films as follows. Oxidized silicon wafers (with 300-nm thick SiO_2) were used as the starting substrate. First, a 500-nm thick Al-2%Si layer is deposited at a temperature and pressure of 25°C and 4 mT, respectively. The Al-2%Si film is then exposed to oxygen for 2 minutes at 25°C and 2 mT to form a thin interfacial oxide for the AIC process. A 750-nm thick a-Si film is then deposited at 25°C, 3.6 mT. Note that the a-Si film must be at least 1.4 times thicker than the Al-2%Si film in order to ensure a continuous poly-Si film at the end

of the AIC process [26]. A cross-sectional SEM of the as-deposited film stack is shown in Fig. 6.12(a).

The Al-2%Si/a-Si thin film stack is then annealed in vacuum ($\sim 10^{-7}$ T) at 350°C for 3 hours. During this anneal, the Si displace the Al, resulting in a 500-nm thick poly-Si layer on the bottom and an Al layer with embedded Si clusters on the top, as shown in Fig. 1(b). The thin interfacial oxide layer ensures a uniform poly-Si layer thickness [26]. It is apparent from Fig. 6.12(b) that the layer exchange process is not yet completed, however. Thus, selected samples received an additional pulsed (30 ns) excimer laser anneal (ELA). The ELA (at 308 nm wavelength) is performed with 3 shots at a fluence of 100 $\frac{\text{mJ}}{\text{cm}^2}$ to drive the layer exchange process to completion, as shown in Fig. 6.12(c). Finally, the top layer of Al was selectively removed with a wet Al etchant.

AIC poly-Si films are conductive due to the incorporation of Al, which is an acceptor-type impurity, at the solid solubility limit [26, 27]. Nast *et al.* [27] performed Hall-effect measurements at room temperature to determine the mobile carrier concentration and resistivity: for poly-Si films formed by AIC at 500°C, the hole concentration (p) and resistivity (ρ) were $\sim 2.6 \times 10^{18}\text{cm}^{-3}$ and 0.041 Ωcm, respectively. The resistivities of the AIC poly-Si films studied in this work were measured from four-point probe measurements, to be 0.176 Ωcm and 0.172 Ωcm for films formed with and without an ELA treatment, respectively. These higher resistivity values are likely due to lower hole concentrations because of the lower solid solubility of Al in Si at 350°C.

6.5.2 X-ray Diffraction Analysis of AIC Poly-Si Films

X-ray diffraction (XRD) analyses were performed on annealed samples before and after the removal of the top Al layer, using a Siemens D-5000 X-ray diffractometer with Cu Kα radiation ($\lambda = 1.5418$Å). The anode voltage and emission current for the x-ray source were 40 kV and 30 mA, respectively. Fig. 6.13 shows the 2θ scans for samples prior to removal of the top Al layer. A strong Si(400) peak is observed due to the substrate, and a large Al(111) peak is observed due to the top Al layer. The Si(111) peak is due to the

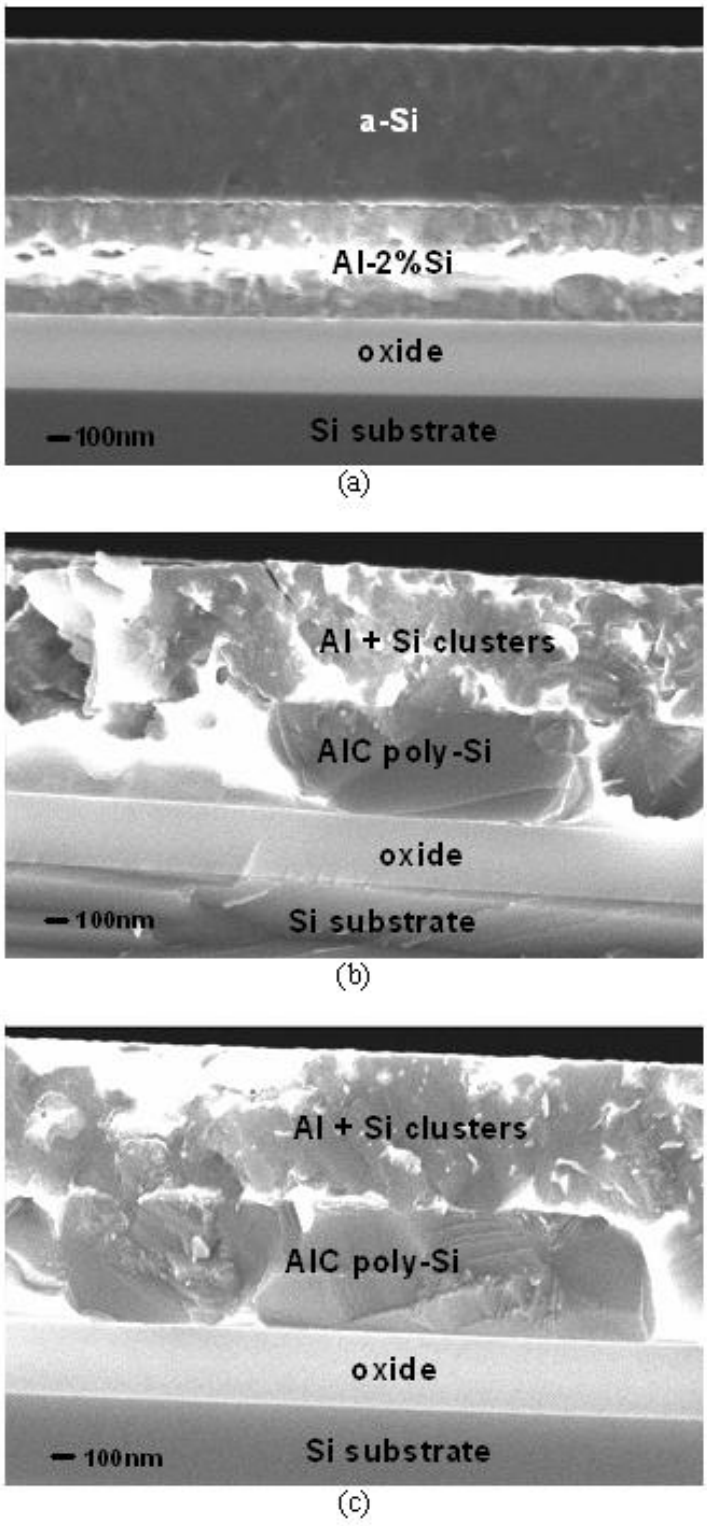

Figure 6.12. Cross-sectional scanning electron micrographs of (a) as-deposited Al-2%Si/a-Si thin-film stack, (b) film stack after a 350°C, 3 hr anneal, and (c) film stack after a 350°C, 3 hr anneal + an ELA treatment.

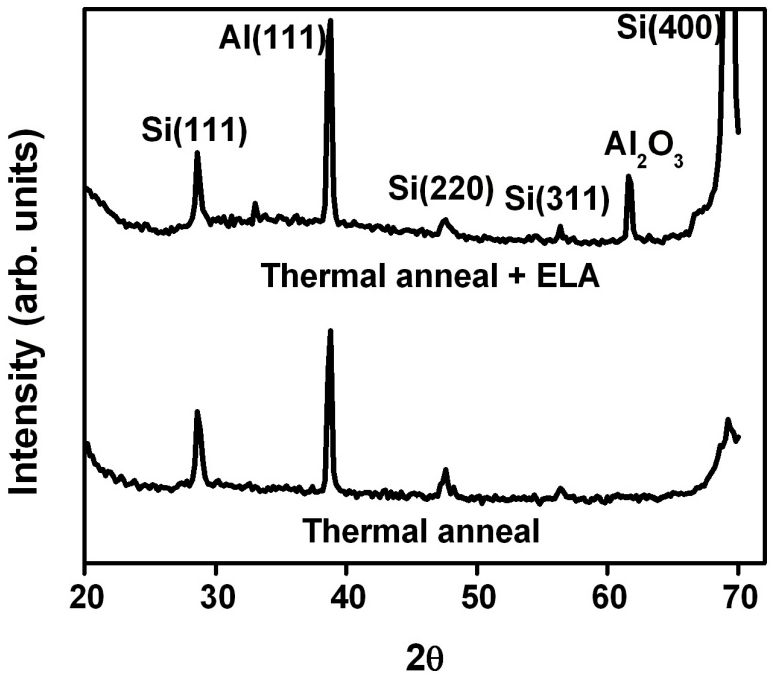

Figure 6.13. XRD 2θ scans of annealed thin film stacks prior to removal of the top Al layer. The lower curve is for a sample which did not receive an ELA treatment; the upper curve is for a sample which received an additional ELA treatment. The Si(111) peak and the weaker Si(220) and Si(311) peaks indicate the successful formation of a poly-Si layer.

bottom poly-Si layer, as are the weaker Si(220) and Si(311) peaks. An additional peak at 61.6° is seen for the sample which received an ELA treatment, which can be attributed to Al_2O_3(018) or Al_2O_3(122). This indicates that polycrystalline alumina is formed during the ELA treatment, which is performed in (oxygen-containing) ambient air.

Fig. 6.14 shows the 2θ scans for samples after removal of the top Al layer. The crystalline Al and Al_2O_3 peaks are no longer present, whereas the poly-Si peaks remain, as expected. The texture of the poly-Si films can be determined from the fractional volumes of the (111), (220) and (311) peaks. Although the (110) texture cannot be measured directly due to the lack of crystal symmetry, it can be deduced from the (220) peak. The (100) texture of the poly-Si films cannot be determined due to the large Si(400) peak from the substrate. The (111):(220):(311) area ratio for AIC poly-Si films formed without ELA treatment is 1:0.38:0.20. For films formed with an ELA treatment, the area ratio is almost unchanged at 1:0.39:0.21. With the normalization factors of 1, 0.38 and 0.19 for the (111), (220) and (311)

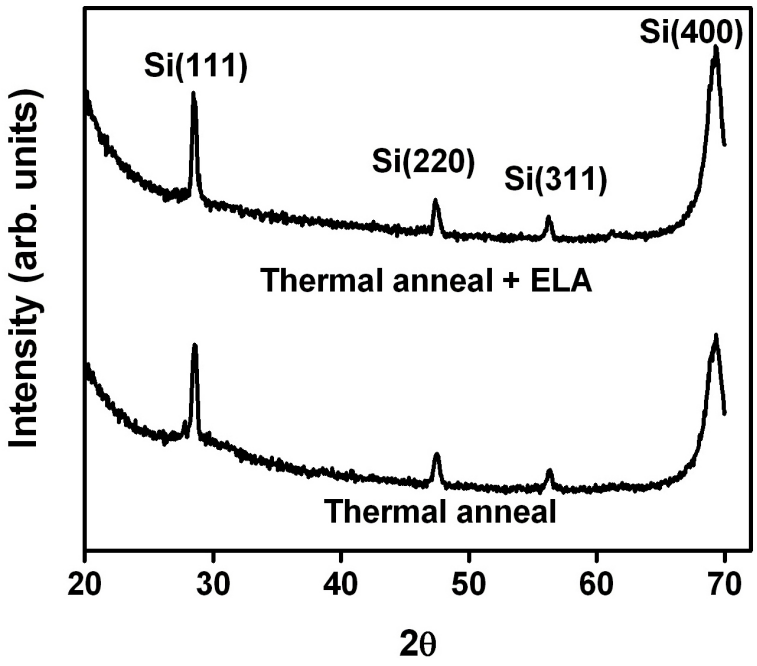

Figure 6.14. XRD 2θ scans of annealed thin film stacks after removal of the top Al layer. The lower curve is for a sample which did not receive an ELA treatment; the upper curve is for a sample which received an additional ELA treatment.

peaks, respectively [28], the fractional volumes of the three textures are approximately equal, indicating no dominant grain orientation. By comparison, Haji et al. [29] and Christiansen et al. [30] showed that poly-Si films formed by solid phase crystallization (SPC) and ELA have strong (111) texture when the films have large crystallites (*i.e.* when the average grain size is much greater than the film thickness, as is the case for poly-Si formed by AIC [24]). Both studies also showed that films with smaller crystallites have no preferred grain orientation.

6.5.3 Mechanical Properties of AIC Poly-Si Films

Two-terminal relays were fabricated on heavily n-type doped Si(100) wafer substrates with a 150-nm thick SiO_2 sacrificial layer and a 500-nm thick AIC poly-Si structural layer. The AIC poly-Si films were patterned to form cantilever beams and clamped-clamped beams of various lengths, using conventional photolithography and dry etching processes.

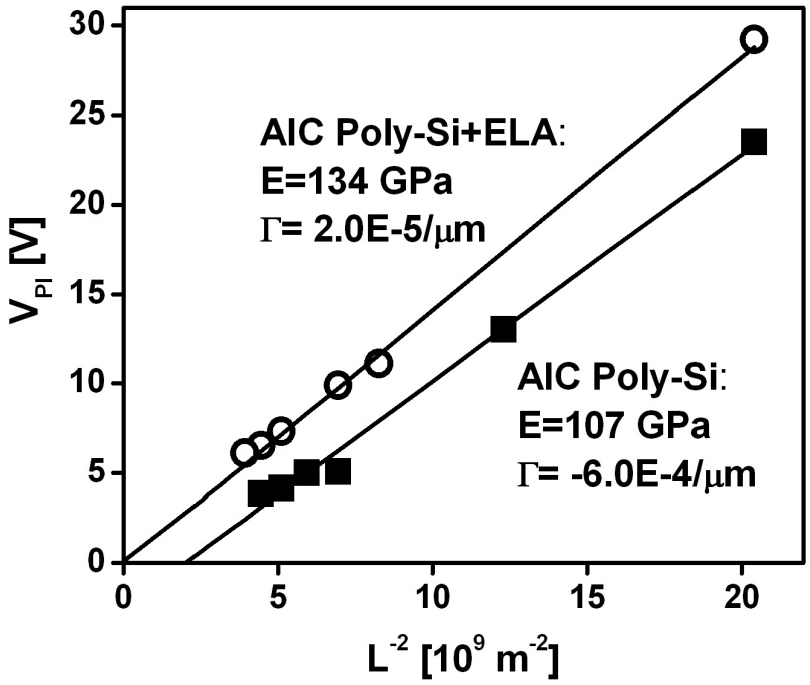

Figure 6.15. Young's modulus (E) and strain gradient (Γ) extraction from pull-in voltage measurements of AIC poly-Si cantilever beams of various lengths, with and without ELA treatment, shown by open and closed symbols, respectively.

The beams were released using a timed (15-minute) HF vapor etch. Pull-in voltage (V_{PI}) measurements for 1-μm wide beams of various lengths were used to extract the mechanical properties of the AIC poly-Si films. The workfunction difference ($\Delta\Phi$) of 1 V for a p-doped poly-Si structural beam and n+ doped Si bottom electrode is incorporated in the pull-in voltage measurements.

From Fig. 6.15, the slope of the V_{PI} versus $\frac{1}{L^2}$ plot indicates that the Young's modulus of AIC poly-Si formed without an ELA treatment (107 GPa) is between the bulk Al and Si values, consistent with expectations based on Fig. 6.12b. The value of Young's modulus is determined to be 134 GPa for the AIC poly-Si with ELA treatment, which falls within the range for monocrystalline silicon [31]. This confirms that the additional ELA treatment completes the layer exchange process, as expected from Fig. 6.12c.

The extracted Γ values are shown in Fig. 6.15. The AIC poly-Si film formed without an ELA treatment exhibits moderate, negative strain gradient ($\Gamma = -6.0 \times 10^{-4} \mu m^{-1}$) and

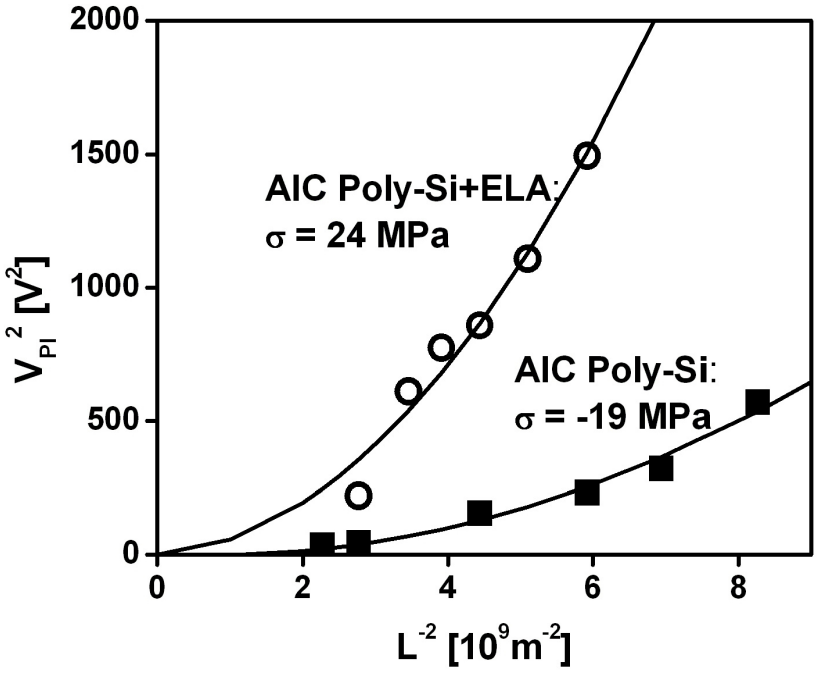

Figure 6.16. Residual stress (σ) extraction from pull-in voltage measurements of AIC poly-Si clamped-clamped beams with and without ELA treatment, shown by open and closed symbols, respectively.

low Young's modulus (which is generally undesirable) because of incomplete layer exchange during the crystallization process. The AIC poly-Si film formed with an ELA treatment exhibits a slight positive strain gradient ($\Gamma = 2.0 \times 10^{-5} \mu m^{-1}$), since the partial melting and recrystallization which occurs during the ELA process results in tensile strain in the surface region [32]. The AIC poly-Si film with ELA treatment exhibits low strain gradient comparable to high-temperature deposited poly-Si, and an order of magnitude lower than that of poly-$Si_{0.4}Ge_{0.6}$.

Residual stress is extracted from a plot of V_{PI}^2 versus $\frac{1}{L^2}$, shown in Fig. 6.16. The AIC poly-Si film formed without an ELA treatment exhibits low compressive stress (-19 MPa). An additional ELA treatment causes the film to become tensile on average (24 MPa), consistent with ELA treatment on poly-SiGe films [32]. Thus, AIC poly-Si with the ELA treatment is a promising material and exhibits similar mechanical properties with high-temperature as-deposited poly-Si while requiring much lower fabrication temperature.

6.6 Summary

The mechanical properties of candidate low-thermal-budget MEMS structural materials have been investigated for integration with CMOS electronics. Metal films were considered due to excellent conductivity and ability to deposit the films at low temperatures. Metals deposited by PVD have large residual stress due to large intrinsic stress or thermal stress, up to few hundred MPa up to 1GPa. Of the four metals investigated (Al, Ni, Ti and TiN), only Aluminum films deposited at low temperatures (<100°C) exhibit low tensile residual stress. However, the strain gradient of Al is larger than that of low-temperature as-deposited poly-$Si_{0.4}Ge_{0.6}$. These metals are promising for small MEMS structures such as nanoscale relays and memories, but cannot be used for large MEMS structures such as inertial sensors.

Poly-Si films can be formed at temperatures lower than required for poly-$Si_{0.4}Ge_{0.6}$ by AIC. AIC poly-Si films formed at 350°C exhibit moderate strain gradient, lower than that of low-temperature poly-$Si_{0.4}Ge_{0.6}$ but still larger than that of high-temperature poly-Si films. AIC poly-Si exhibits much lower compressive stress than poly-$Si_{0.4}Ge_{0.6}$ films. To ensure complete layer exchange, an additional low energy fluence ELA treatment was performed, resulting in a Young's modulus of AIC poly-Si that is well within the range of bulk Si values. With the additional ELA treatment, the film exhibits low strain gradient comparable with high-temperature poly-Si films and low tensile stress. Since AIC poly-Si formed with the additional ELA treatment has superior mechanical properties and can be formed at lower temperatures as compared to poly-$Si_{0.4}Ge_{0.6}$, it is a promising structural material for large MEMS devices built over CMOS electronics, such as inertial sensors.

6.7 References

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Chapter 7

Conclusions

7.1 Summary of Contributions

Several low-thermal-budget processes and structures were proposed in this work for applications such as flat panel displays and 3-D integrated microsystems.

The flat panel display industry has been continuously growing as poly-Si TFT technology is used increasingly for mobile applications such as cell phones, digital cameras and laptop displays. One goal that many TFT manufacturers are aiming for is system-on-panel (SOP), where all electronic circuitry is directly fabricated on the display substrate. A portion of this work addressed poly-Si TFT processes and device structures that can improve device uniformity and reliability for SOP applications.

Low-thermal-budget materials for integrated mechanical microsystems have been investigated for MEMS applications ranging from inertial sensors to RF filters to nanoscale relays. The remainder of this work addressed finding a low-temperature structural material that is compatible with post-CMOS processing with excellent mechanical properties.

7.1.1 Contributions to Poly-Si Thin Film Transistor Technology

The first process technique addressed the need to improve the Si/SiO_2 interface with an ultra-low-temperature process thermal budget of 150°C. Ultraviolet (UV) oxidation was used to form a gate oxide interfacial layer. The UV oxide shows excellent interface properties, if grown at a pressure of 0.5 mT and temperature of 150°C. A low interface trap density (D_{IT}) and fixed oxide charge (Q_F) is measured by surface charge analysis. A TFT gate oxide comprising of a UV oxide interfacial layer and PECVD gate oxide deposited at maximum process temperature of 150°C exhibits better oxide qualities compared to a gate oxide without the UV oxide interfacial layer. Lower D_{IT}, Q_F and high electric field breakdown was achieved with the UV interfacial oxide. Thus, this oxidation process is promising for flexible displays fabricated on plastic substrates.

A second process technique, for defect passivation, was introduced for improved TFT performance and reliability. Selenium implanted into the TFT channel at a moderate dose was shown to effectively passivate defects in the poly-Si channel. The device shows improvements in carrier mobility and off-state leakage current compared to an unpassivated poly-Si TFT device. After electrical stress at high gate and drain biases, devices with Se passivation exhibit better reliability than unpassivated and hydrogen-passivated devices, due to the strong Si-Se bond. Selenium and hydrogen passivation are complementary techniques that can successfully passivate tail and midgap trap states.

A new TFT device structure was proposed that would improve device uniformity by reducing sensitivity to grain boundaries in the poly-Si channel. Two-dimensional device simulations showed that an accumulation-mode TFT device requires thin gate oxide and Si channel thicknesses to achieve high I_{ON}/I_{OFF} ratios. The threshold voltage and on-state current of an accumulation-mode TFT showed less sensitivity to a single grain boundary location in the channel compared to a conventional enhancement-mode TFT. The fabrication process flow for a vertical accumulation-mode TFT was proposed.

A poly-Si tunneling field effect transistor (TFET) was fabricated at low process thermal

budget of 600°C. The poly-Si TFET has lower off-state current compared to a conventional n-channel TFT for long channel devices, but does not improve the TFT on-state current. However, the measured on-state current was greater in shorter channel devices due to the tunneling current and impact ionization at short channels. However, high off-state leakage currents were also measured in these TFTs. The subthreshold slopes were worse in the TFET devices due to the sensitivity of S to gate oxide thickness in the TFET device. The TFET gate oxide and gate length dimensions should be scaled to fully achieve benefits of the novel structure. Further optimization of the poly-Si TFET is necessary to achieve high on/off current ratios and steep subthreshold slopes. An optimized device structure is proposed in the next section.

7.1.2 Low-Thermal-Budget Materials for 3-D MEMS Integration

Low-thermal-budget materials were investigated for fabrication of MEMS on CMOS for 3-D integration applications. Excellent mechanical properties, such as average low tensile stress and low strain gradient, are required. Metals and poly-Si formed at low temperatures were investigated as potential mechanical materials. The mechanical properties of these films were measured by wafer curvature and analytical model. The average residual stress of metals deposited by PVD were dependent on sputter deposition process parameters, which yielded highly tensile films (such as nickel) or highly compressive films (such as titanium and titanium nitride). Only aluminum exhibited low average residual stress; however, large strain gradients were measured. Poly-Si can be formed by aluminum-induced crystallization (AIC) at temperatures below 350°C. These films showed promising mechanical properties, which further improved with an additional excimer laser anneal. The resulting AIC poly-Si films with the excimer laser treatment showed low tensile stress and low strain gradients which are promising for large MEMS devices such as inertial sensors and small MEMS devices such as nanoscale relays.

7.2 Suggestions for Future Work

7.2.1 Accumulation Mode Thin Film Transistors

The accumulation-mode MOSFET was simulated using a two-dimensional device simulator. The simulated results show that the accumulation-mode device must have thin gate oxide films below 10 nm and channel thickness below 15 nm to achieve high I_{ON}/I_{OFF} current ratios. However, several challenges arise in the fabrication of accumulation-mode TFTs, including the deposition of thin gate oxide and silicon film thickness and crystallization of thin silicon films. The vertical accumulation-mode TFT was proposed, where spacer lithography would be used to define the active region. In this structure, the deposition and crystallization of thin Si channel is addressed.

The other challenge that arises is finding a thin gate oxide deposition process formed at low temperatures. By forming a good quality 10-nm-thick gate oxide, lower supply voltages can be utilized which decreases the power consumption and alleviates avalanche-induced short channel effects [1]. A good quality interface can be achieved by a UV oxidation process, proposed in chapter 2, which can be incorporated in the accumulation-mode TFT fabrication.

The accumulation-mode TFT can be fabricated by a standard TFT processes and the UV oxide process. The new structure should provide better device uniformity due to lessened sensitivity to grain boundaries in the poly-Si channel.

7.2.2 Optimized Silicon Tunneling Field Effect Transistor Structure

Exploratory work in polycrystalline silicon tunneling field effect transistors (poly-Si TFETs) was presented in this work. Preliminary assessment of poly-Si TFET design shows the enhancement in I_{ON} is achieved but at the cost of high I_{OFF} and poor S. Because the undoped poly-Si channel is highly resistive due to low channel doping and high density of grain boundaries, the on-state channel resistance limits the current in this device.

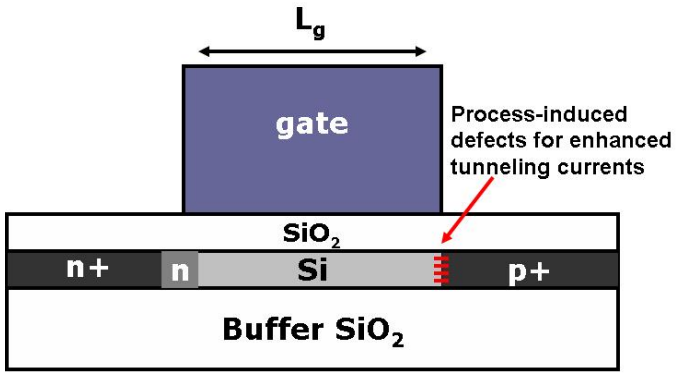

Figure 7.1. Optimal TFET design with process-induced defects for enhanced tunneling currents.

From this work, an optimal TFET design is proposed in Fig. 7.1 for low-power applications. The proposed device utilizees a conventional high-temperature CMOS fabrication process, and so it is beyond the scope of this work. The Si TFET can be fabricated on silicon-on-insulator (SOI) substrate with an undoped channel and is absent of grain boundaries. The TFET needs thinner gate oxides below 10 nm in order to achieve steep subthreshold slopes comparable to the MOSFET with equivalent gate oxide thickness. To suppress ambipolar operation at the n+ drain tunneling junction, an n-type lightly-doped drain (LDD) region is introduced. By adding a graded junction, the electric field at the LDD is less abrupt, which suppresses band-to-band tunneling current at this junction. Process-induced traps can be introduced at the p+ source tunneling junction, which enhance the band-to-band tunneling on-state current. One method of introducing traps selectively is by masking most of the TFET and implanting through unmasked portions. Incorporating these proposed changes will benefit from advantages of monocrystalline Si TFETs (low I_{OFF} and steep S) with enhancements in I_{ON} from trap-assisted tunneling currents through traps selectively introduced near the tunneling junction.

7.3 References

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