Novel Material Integration for Reliable and Energy-Efficient NEM Relay Technology

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Technical Report No. UCB/EECS-2014-227
http://www.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-227.html

December 19, 2014

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By

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A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Tsu-Jae King Liu, Chair
Professor Elad Alon
Professor Ronald Gronsky

Fall 2014

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Abstract

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Energy-efficient switching devices have become ever more important with the emergence of ubiquitous computing. NEM relays are promising to complement CMOS transistors as circuit building blocks for future ultra-low-power information processing, and as such have recently attracted significant attention from the semiconductor industry and researchers. Relay technology potentially can overcome the energy efficiency limit for conventional CMOS technology due to several key characteristics, including zero OFF-state leakage, abrupt switching behavior, and potentially very low active energy consumption. However, two key issues must be addressed for relay technology to reach its full potential: surface oxide formation at the contacting surfaces leading to increased ON-state resistance after switching, and high switching voltages due to strain gradient present within the relay structure.

This dissertation advances NEM relay technology by investigating solutions to both of these pressing issues. Ruthenium, whose native oxide is conductive, is proposed as the contacting material to improve relay ON-state resistance stability. Ruthenium-contact relays are fabricated after overcoming several process integration challenges, and show superior ON-state resistance stability in electrical measurements and extended device lifetime. The relay structural film is optimized via stress matching among all layers within the structure, to provide lower strain gradient (below 10^{-3} μm^{-1}) and hence lower switching voltage. These advancements in relay technology, along with the integration of a metallic interconnect layer, enable complex relay-based circuit demonstration. In addition to the experimental efforts, this dissertation theoretically analyzes the energy efficiency limit of a NEM switch, which is generally believed to be limited by the surface adhesion energy. New compact (<1 μm^2 footprint), low-voltage (<0.1 V) switch designs are proposed to overcome this limit. The results pave a pathway to scaled energy-efficient electronic device technology.

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Acknowledgements

This dissertation is a microcosm of my graduate school life, and I have benefited a lot from the thoughtful journey. In a sense, this is the most difficult part to write in this dissertation since it brings back many bittersweet memories. There are so many individuals whom I have crossed paths with, and so many memorable stories to relive. Now at the end of my graduate studies, I would like to give thanks to all of those who made an impact on this dissertation and who helped me in achieving this milestone.

First I would like to acknowledge my advisor, Professor Tsu-Jae King Liu for her mentorship and guidance throughout my graduate student career. Her extensive knowledge, true professionalism and insightful vision have not only guided my research, but also exemplified how a scholar and visionary should be. Her dedication and technical prowess has given me great inspiration both professionally and personally. I had no knowledge and no interest to mechanical switches when I stepped onto UC Berkeley campus, but her passion has transformed me into an enthusiast and ultimately motivated me to complete my graduate study in this field.

I would like to acknowledge Professor Elad Alon for countless discussions about relay technology and circuits throughout the collaboration in demonstrating relay-based circuits, as well as serving as the chair of my qualifying exam committee. His insightful suggestions have immense impact on this dissertation. I would like to express my gratitude to Professor Vladmir Stojanović and Professor Dejan Marković (UCLA) for many fruitful discussions in this collaboration, and to my colleagues Dr. Matthew Spencer, Dr. Chengcheng Wang (UCLA), Dr. Hossein Farborzi (MIT), Sumit Dutta (MIT), and Fred Burghardt for sharing the excitement when making last minute dashes to our deadlines together.

I would like to thank many faculty members who led me through the vast knowledge in the world of science and engineering: Professor Ronald Gronsky for serving on my qualifying exam and dissertation committees, whose kind suggestions and unlimited patience finally make this dissertation a reality; Professor Ming Wu for serving on my qualifying exam committee, and helping me look at my research from a different angle to make it more complete; Professor Eli Yablonovitch for supporting my energy-efficient nanomechanical switch designs, and for teaching me to be persistent to basic physics when exploring new technology; Professor Junqiao Wu for sharing his ideas to experimentally demonstrate aggressively scaled switch designs.

I would like to express my appreciation to Professor Eric Pop, who gave me research opportunity when I was an undergrad in University of Illinois at Urbana-Champaign and dedicated so much of his time to guiding a youngster. It is his encouragement and support that made me a researcher in solid state electronics. I would also like to thank Professor K.C. Hsieh and Professor Joseph Lyding for their great classes that sparked my interest in this field.

I would like to thank Dr. Louis Hutin, Dr. Vincent Pott, and Dr. Rhesa Nathanael for being empathetic mentors when I started my graduate study and for their tremendous support when difficulty arose in my research. I am also fortunate to work with so many great minds in King Group, including Dr. Min Hee Cho, Dr. Nattapol Damrongplasit, Dr. Jun Fujiki, Dr. Byron Ho, Dr. Zachery Jacobson, Dr. Jaeseok Jeon, Dr. Hei “Anderson” Kam, Dr. Kimikiko Kato, Dr. Sung Hwan Kim, Dr. Wook Hyun Kwon, Dr. Donovan Lee, Dr. Peter Matheu, Dr. Eung Seok

Park, Dr. Changhwan Shin, Dr. Xin Sun, Dr. Reinaldo Vega, Dr. Nuo Xu, Dr. Jack Yaung, Yenhao “Philip” Chen, Chuang Qian, Peng Zheng, Xi “Robin” Zhang, Jeff Sun, Yoolhee “Hailey” Kim, Benjamin Osoba, and Urmita Sikder. Their companionship in the cleanroom, in the characterization lab, and in the office made the tough work satisfying, and the lively interactions with them sparked new ideas that contributed to my research.

Experimental demonstrations in this dissertation would not be possible without the staff of UC Berkeley Marvell Nanofabrication Lab, where most of the magic happens. Maintaining a university research cleanroom is a daunting task. Nevertheless you all did a marvelous job in supporting one of the most advanced one. In particular, I would like to thank Jimmy Chang, Joe Donnelly, Jay Morford, Sia Parsa, and Evan Stateler for helping my experiments running more smoothly, and for kindly sharing the process wisdom they acquired from maintaining the fabrication tools with me.

I would like pay additional thanks to industry collaborators—Dr. Wade Xiong, Dr. Chanro Park, Rinus Lee, and Wei Yip Loh from SEMATECH. The work in this dissertation is partially supported by National Science Foundation (NSF) Graduate Research Fellowship Program, DARPA/MTO Nano-Electro-Mechanical Systems program, NSF Center for Energy Efficient Electronics Science, and Center for Materials, Structures, and Devices.

I owe deepest debt of gratitude to my family. It is difficult to sail alone to a new country at a young age, but it is reassuring to know that their unconditional love, patience, and encouragement are always with me. I would not be here today without the sacrifices they made for me and the faith they have in me. I would like to thank I-Hsuan for always being besides me. Her laughter in bright days and her compassion at my dark times helped me to navigate through all the adventures of life. Finally, I would like to shout out to all my friends, whether we met in Taiwan, in Berkeley, in Urbana-Champaign, or anywhere around the world. I cherish our friendship that made my days enjoyable and delightful.

Chapter 1

Introduction

1.1 CMOS Energy Efficiency Limit and the Era of Low-Power Electronics

The invention of complementary metal-oxide-semiconductor (CMOS) transistor technology, which is used in today's very large scale integrated (VLSI) circuits, has revolutionized electronics and information storage technology and has shaped the world that we live in today. For the past half century, the continuing miniaturization of transistors, guided by Moore's Law, has enabled ever more functional and affordable electronic devices [1]. By scaling down transistor dimensions, the performance and energy efficiency of VLSI circuits have been improved due to reduced resistance and capacitance. With each new generation of CMOS technology, integrated circuit "chip" functionality has doubled roughly every two years, or the production cost has halved for the same functionality. This exponential functionality/cost improvement has led to the age of "smart" electronics, where people are surrounded by computing and sensory solid-state devices and circuits.

While simply scaling all transistor dimensions and voltages proportionally had traditionally led to tremendous success in improving transistor performance, scaling CMOS transistors in the deep sub-micron regime has become increasingly more difficult [2, 3]. Many dimensional scaling challenges have been addressed on a generation-by-generation basis by introducing new materials, advanced processing techniques, and novel device structures. However, the failure to scale transistor threshold voltage (V_{TH}) and circuit supply voltage (V_{DD}) in deep sub-micron CMOS technology cannot be easily addressed by process and design efforts since it is fundamentally inherent to the operating principle of CMOS transistors. Figure 1.1 shows the scaling of V_{TH} and V_{DD} for several technology generations, in which V_{TH} has been roughly constant across several technology generations and both V_{TH} and V_{DD} have failed to scale proportionally with device dimensions as in the traditional Dennard scaling scheme [4, 5].

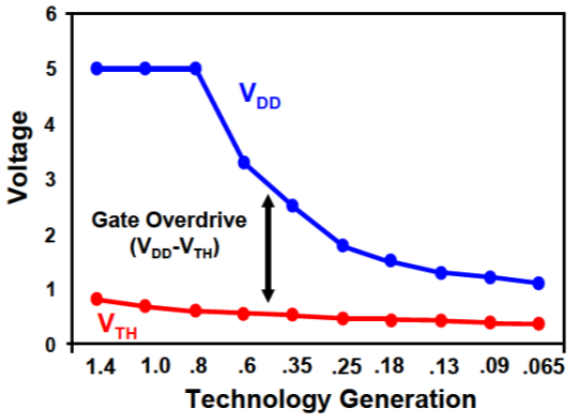


Figure 1.1. Historical V_{DD} and V_{TH} scaling trends, failing to scale with the transistor dimensions. The gate overdrive voltage has also been decreasing in recent generations [6].

CMOS transistors are electronic switches in which the barrier for electron conduction is controlled by the gate voltage (V_G). When $V_G \geq V_{TH}$ to turn ON the transistor, the potential barrier between source and drain is negligible to allow mobile carriers to diffuse into and drift across the channel region. When V_G is low, the potential barrier blocks most of the carrier flow except for a certain number of electrons which have sufficient kinetic energy to diffuse over the barrier via thermionic emission. Since the energy distribution of mobile carriers follows the Boltzmann distribution, the amount of carriers with sufficient energy to diffuse over the barrier increases exponentially with reduction in the barrier height. In the subthreshold region of operation (i.e. $V_{TH} \geq V_G \geq 0$), the slope of the semi-log plot of drain current vs. gate voltage $\log(I_D)$-V_G is constant at fixed temperature, and is characterized by the subthreshold swing (SS). Due to the thermionic emission nature of subthreshold current, SS of CMOS transistors is fundamentally limited by the thermal voltage, as $SS \geq \ln(10)\times(kT/q)$ = 60 mV/decade at room temperature. Since kT/q is a non-scaling physical constant, reductions in V_{DD} and V_{TH} of transistors leads to the dilemma illustrated in Figure 1.2. For a technology with threshold voltage V_{TH1}, reducing supply voltage from V_{DD1} to V_{DD2} leads to reduced transistor ON-state drive current and thus degraded circuit performance. To retain the same circuit performance while reducing supply voltage, the threshold voltage must be reduced (from V_{TH1} to V_{TH2}) in order to maintain the same gate overdrive voltage. However, reducing threshold voltage leads to exponentially increasing OFF-state leakage current I_{OFF} (i.e. I_D at V_G = 0). This is the primary reason that voltage scaling has lagged behind dimensional scaling in recent generations of CMOS technology (since the 90 nm node), as V_{DD} and V_{TH} cannot be scaled effectively without losing performance or increasing power consumption.

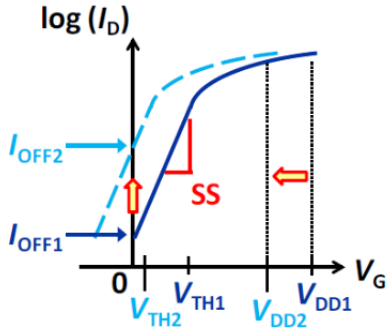


Figure 1.2. log(I_D)-*vs.*-V_G plot of a MOS transistor, showing the effect of scaling V_{TH} and V_{DD} with non-zero subthreshold swing. The leakage current increases exponentially with V_{TH} reduction [7].

To address this dilemma, parallelism has been widely adopted to operate circuits at lower I_{OFF} while recouping the performance loss at the system level by running multiple processors in parallel. However, parallelism will eventually be ineffective due to a fundamental energy efficiency limit for CMOS circuits [8]. Figure 1.3 shows the tradeoff between dynamic and leakage energy consumption on an energy per operation basis for a CMOS digital logic circuit. The dynamic energy, which is proportional to V_{DD}^2, can be scaled by reducing V_{DD}. However, in doing so the circuit suffers either increased delay (via reduced I_D) or leakage. The energy dissipated due to transistor OFF-state leakage is given by:

$$E_{leak} = L_D f I_{OFF} V_{DD} t_{delay}, \tag{1.1}$$

where L_D is the logic depth, f is the fanout, and t_{delay} is the time delay per operation. As evidenced in equation 1.1, E_{leak} increases with reduced V_{DD} via super-linear I_{OFF} or t_{delay} increase. This implies an optimal energy point for total energy consumed per operation and this optimal E_{tot} represents a fundamental energy efficiency limit given the operating principle of CMOS transistors.

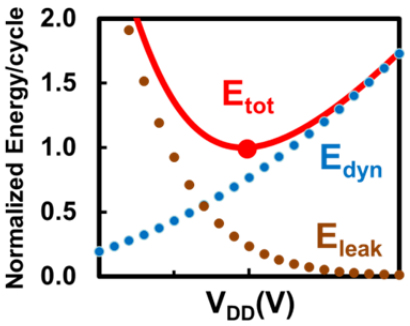


Figure 1.3. CMOS energy per operation tradeoff between dynamic and leakage energy.

The consequence of failing to scale voltages commensurately with transistor dimensions is shown in Figure 1.4. As CMOS transistors continue to shrink in size, the chip-level power density increases exponentially. Passive (leakage) power consumption used to be an afterthought when considering power implications of CMOS circuit designs, but is now balanced against active (switching) power consumption in the course of CMOS circuit design optimization. As a result, the semiconductor industry has been searching for advanced device concepts that are not based on switching via modulation of thermionic emission, such as devices that operate by modulating tunneling, mechanical movements, or spin-torque [9]. In general this approach in finding "More-than-Moore" devices aims to circumvent the CMOS energy efficiency limit by providing for steeper subthreshold swing (SS < 60 mV/decade), so that I_{OFF} and passive power consumption can be lower than for CMOS transistors. The integration of lower-power devices is critical for realizing ubiquitous information processing, in which people are surrounded by low-power distributed wireless sensing and computing devices that allow them to interact in real time with their environment [10].

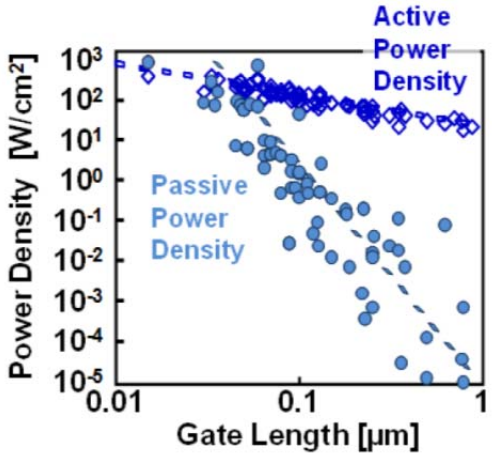


Figure 1.4. CMOS circuit power density increase with transistor scaling [11].

1.2 Energy-Efficient Nano-electro-mechanical Relay Technology

Among all steep-subthreshold switching devices, the nano-electro-mechanical (NEM) relay is the only one that offers the ideal characteristics of zero OFF-state leakage current and abrupt switching between OFF- and ON-states so that $SS \sim 0$, to eliminate the tradeoff between active and passive power consumption [12]. In this section, the operating concept, device design, and process flow for prototype logic relay devices is presented. The challenges and concerns for NEM relay technology are further analyzed in sections 1.3 and 1.4.

1.2.1 Device Operating Concept

Figure 1.5 illustrates the operation of a basic 3-terminal (3-T) relay with movable source and fixed gate and drain electrodes. In the OFF-state, the source and drain terminals are separated by an air gap so that no current can flow between them. When a voltage is applied to the gate terminal, the movable structure is actuated downward by electrostatic force. When the applied voltage is sufficiently large, the source comes into contact with the drain, forming a low-resistance path for current conduction. To turn OFF the switch, the gate voltage (V_G) is removed and the spring restoring force of the movable source electrode actuates it upwards, breaking the contact between source and drain. Electrostatic actuation is attractive for digital logic operations because the capacitive actuator is easy to manufacture using conventional processing techniques, requires low active power, and is scalable to small dimensions [7].

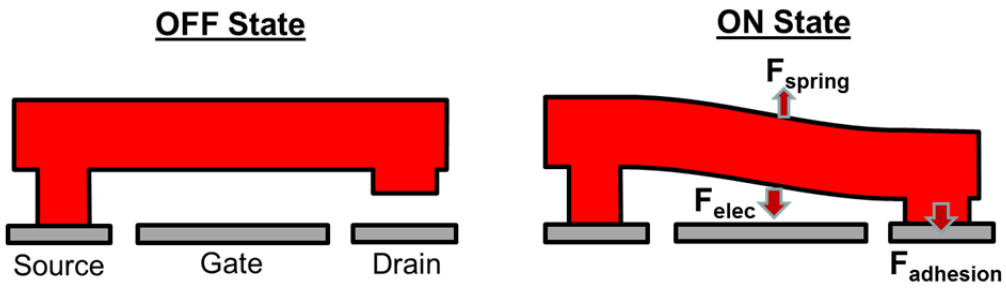


Figure 1.5. Conceptual illustration of a 3-T relay in OFF- and ON-states.

Figure 1.6 shows the measured I-V transfer characteristics of a micrometer-scale relay. In the OFF-state, zero leakage current is observed due to the air gap preventing conduction; only ambient noise current is measured. As V_G increases, the movable structure is actuated intocontact with the drain electrode when V_G is greater than the pull-in voltage (V_{PI}). Since the device is turned ON by mechanical actuation, the switching behavior is perfectly abrupt. Note that surface adhesion force exists once the source/drain terminals are in contact. In the backward sweep, V_G is gradually lowered to reduce the electrostatic force, and eventually the spring restoring force of the movable structure becomes greater than the surface adhesion plus electrostatic forces when V_G is less than release voltage (V_{RL}). At this point the structure is actuated out of contact with the drain terminal. The hysteretic switching behavior ($V_{PI} > V_{RL}$) can be attributed to the so-called pull-in phenomenon and surface adhesive force [13, 14].

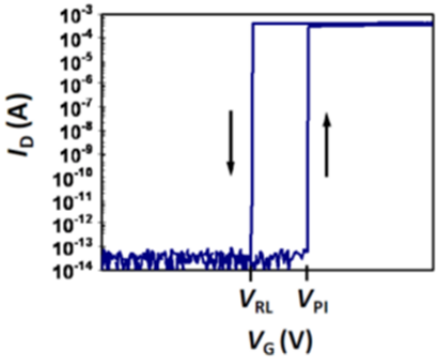


Figure 1.6. Typical measured I-V transfer characteristics of a relay; both forward and reverse gate-voltage sweeps are shown [7].

1.2.2 Relay Design and Fabrication

Figure 1.7 illustrates the schematic and cross-sectional views of a robust 4-terminal (4-T) logic relay design, fabricated using the process flow described in [15]. The 4-T structure comprises an body electrode, which consists of a vertically movable plate suspended over the gate and source/drain electrodes at each corner by a folded-flexure beam anchored to the substrate. The suspension beam design mitigates undesirable effects of residual stress upon release of the structure. The structural film consisting of polycrystalline silicon-germanium (poly-$Si_{0.4}Ge_{0.6}$) is deposited via low-temperature chemical vapor deposition (LPCVD) at 410ºC and is doped *in situ*. A pattterned metallic channel layer is attached to the underside of the body structure via an intermediary body insulator layer, which is a 40-50 nm-thick Al_2O_3 layer deposited via atomic layer deposition (ALD). The channel serves as the bridge between the source and drain electrodes when the relay is in the ON-state. The main advantage of this design is that the actuation terminals (gate and body), the current conduction path (drain, source and channel), and the flexures are all decoupled. The state of the relay is controlled by the gate-to-body voltage (V_{GB}) while ON-state current (I_{ON}) is controlled by the voltage between drain and source (V_{DS}). The square plate at the center of structure defines the actuation area (A_{ACT}) and the dimensions of folded flexures define the effective spring constant (k_{eff}) of the suspended structure; these parameters can be optimized separately. The air gap thickness in the contacting region (T_{CONT}) is made smaller than that in the actuation region (T_{ACT}) by depositing and patterning bi-layer LPCVD sacrificial silicon-dioxide (SiO_2) and later removing the bi-layer SiO_2 via hydrofluoric acid (HF) vapor release process to form air gaps [15]. This dimpled contact design is beneficial to precisely define the area of the contacting region, and it serves to reduce the hysteresis voltage and pull-in delay. Tungsten (W) is selected as the contacting material in the prototype design, and is deposited using DC magnetron sputtering to form the metallic electrode and channel layers.

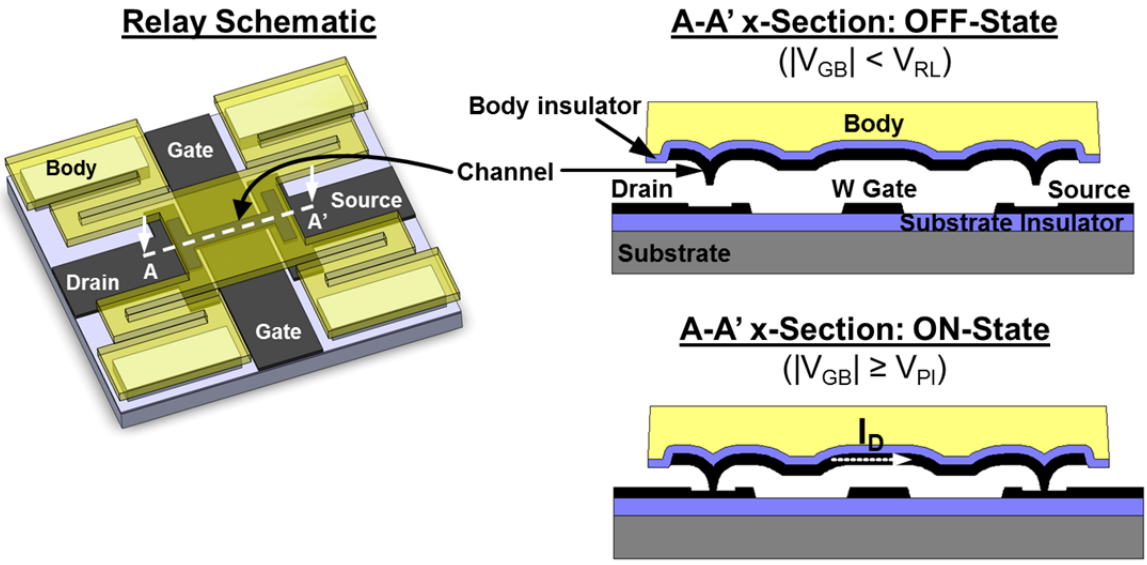


Figure 1.7. Schematic illustrations of a 4-T relay structure. The cross-sectional views of the relay are along the channel (A-A'), for both OFF- and ON-states [15].

Figure 1.8 shows the layout views of the prototype 4-T relay design and an improved 6-terminal (6-T) relay design. The 6-T relay design features two sets of source and drain terminals, effectively combining two switches into one single relay structure. The 6-T relay design eliminates parasitic capacitance effects and allows for more compact implementation of relay-based logic gates [16].

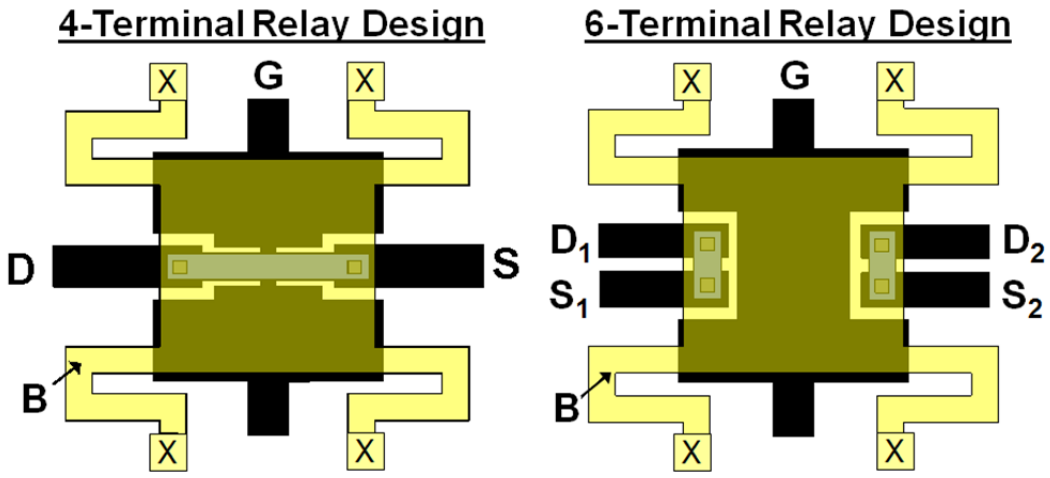


Figure 1.8. Schematic plan views of logic relay structures. (a) 4-T design with a single pair of source/drain electrodes. (b) 6-T design with two independent pairs of source/drain electrodes. Anchors are denoted by "X". (Figure modified from [17])

1.3 Reliability Challenges for Relay Technology

While prototype logic relays have been successfully fabricated, several challenges remain for NEM relay technology to reach its full potential. High cycling endurance is one of the most significant challenges, as stable operation is necessary for relay-based circuits to be practical. For logic applications, relay endurance should exceed 10^{14} ON/OFF switching cycles so that the circuit can operate reliably for 10 years at frequency of 100 MHz and activity factor of 0.01 [12]. Reliability issues for relays can be categorized into structural fracture and contact failure. Contact failure can be due to contact damage and deformation, permanent stiction due to micro-welding and humidity, or unstable ON-state resistance (R_{ON}) due to oxidation and contamination. Each of the failure modes is discussed in this section.

1.3.1 Structural Fracture

In general, there are three primary reasons for thin-film structures to fracture during device operation: strain exceeding the structural material's fracture strength; fatigue of the structural material; and breakdown due to a high bias voltage or high current across the structure. Permanent structural deformation can also occur if the yield strength of the structural material (generally lower than the fracture strength) is exceeded. In the case of logic relays, deformation and fracture due to strain can be avoided by designing for a maximum deflection distance that is much smaller than the suspension beam length [18] so that the maximum strain applied to the structure is less than 0.1%, well below the yield strength of poly-SiGe and most other materials. For the same reason, structural fatigue is unlikely due to low mechanical strain within the structure. In actual measurements, mechanical structural fracture has never been an issue for the prototype logic relay technology.

Structural breakdown during electrical measurements has been observed in prototype logic relays. A poorly designed movable body structure can collapse unintentionally to the underlying gate electrode due to a negative strain gradient or excessive V_{GB}, eliminating the air gap T_{ACT} separating the gate/body terminals. This results in a high voltage (as high as >20 V) between the two terminals with only a thin Al_2O_3 body dielectric separating them, causing the dielectric to breakdown. Proper design to eliminate strain gradient in relay structures is required, and such efforts are discussed in chapter 4. High current density can result in material ablation, as shown in Figure 1.9. Since poly-SiGe is relatively resistive compared to metal, a voltage difference exists between the center plate and one of the anchor pads (where body voltage is first applied) only for a brief moment after applying voltages. This AC breakdown issue can be resolved by designing four anchor pads to be interconnected by metal lines, ensuring that equipotential is achieved throughout body structure.

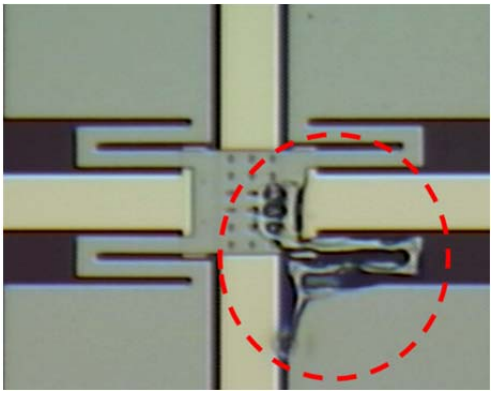


Figure 1.9. Ablation of a resistive flexural suspension beam due to application of voltage at the beginning of electrical measurements (before the body structure reaches equipotential).

It should also be noted that due to the small movable mass and relatively stiff spring (k_{eff} > 10 N/m), the relays discussed in this work are not sensitive to external shock and thermal vibration [12]. Acceleration that is thousands times larger than gravity is needed to cause unintended relay switching.

1.3.2 Contact Wear and Tear

Relays for radio-frequency (RF) switching applications have long been plagued by insufficient endurance that comes along with the soft contacting material, which is needed since RF switches require low R_{ON} (less than 1 Ω) to minimize signal loss. For logic applications, R_{ON} requirement can be greatly relaxed to ~10 kΩ so that hard refractive materials can be used as the contacting material [19, 20]. The contacting material must withstand >10^{14} ON/OFF cycles without significant wear or deformation at the contacting surfaces. The resistance to wear and tear of the contacting surfaces can be further enhanced by the application of an ultra-thin coating, such as titanium oxide (TiO_2), at the expense of slightly increased R_{ON} [21]. Figure 1.10 shows atomic force microscopy (AFM) measurements of the contacting region before and after switching. No discernible differences were observed in contacting electrode topology, confirming the superior wear resistance of a W contacting electrode. The wear resistance of the contacting metal is a major issue when selecting candidates to replace W as the contacting material for NEM relays, as discussed in detail in chapter 2.

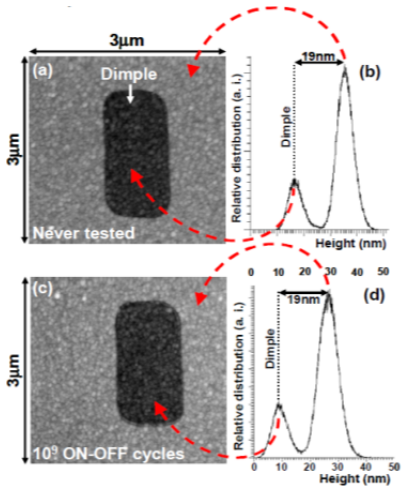


Figure 1.10. AFM scan of the W contacting electrode with TiO_2 coating before and after 10^9 ON/OFF cycles with V_{DS} = 1 V. No wear or deformation is observed in the landing zone of the electrode [15].

1.3.3 Stiction due to Capillary Force

Permanent stiction at the contacts can occur due to high surface forces, which mainly consists of van der Waals force, capillary force, and material bonding [22, 23]. Stiction due to capillary force is a common issue for MEMS structures. The capillary force develops when sacrificial layers are removed during the release process to form air gaps, exposing the metal contacting surfaces which are generally hydrophilic. The conventional release process involves liquid hydrofluoric acid (HF) as the etchant, and a strong attractive force exists between contacting surfaces when the structure is pulled out of liquid HF. An alternative release process using vapor-phase HF can be employed to release logic relays at the final step of fabrication to mitigate the stiction issue.

Even with the dry release process, stiction is still an issue for NEM relay technology due to the contacting surfaces attracting humidity from the environment. Water is a by-product of the HF vapor release process, and without proper pumping the water molecules may lead to stiction similarly as for a wet release process. When exposed to ambient air, a phenomenon called capillary condensation can also occur at the contacting surfaces to increase capillary force [24]. Controlling humidity is important both during and after the dry release process, and can be potentially addressed via hermetically sealed packaging [25]. Surface coating using organic self-assembled-monolayer (SAM) molecules also can be used to achieve hydrophobicity and thereby eliminate capillary force [26].

1.3.4 Micro-welding

In digital integrated circuits, the switching devices are used to charge and discharge nodal capacitances present in the circuit. During the transient response of switching events, current flows between the source and drain terminals of the corresponding switching device. In a logic relay, R_{ON} is dominated by the contact resistance between channel and source/drain electrodes since the contacting surfaces are not perfectly smooth and physical contact only occurs locally at a few asperities. While current flows between source and drain terminals, Joule heating occurs and the temperature is the highest at the contacts due to high resistance [27]. As the contact temperature nears the melting point of the contacting material, atoms around the contacting asperities become thermally activated to fill the physical voids and to increase the real contact area (as opposed to the apparent/drawn contact area which remains the same), as illustrated in Figure 1.11. The increased real contact area results in increased surface adhesion (mainly bonding and van der Waals forces) and ultimately micro-welding when the surface adhesive force exceeds the spring restoring force to prevent the relay from turning OFF.

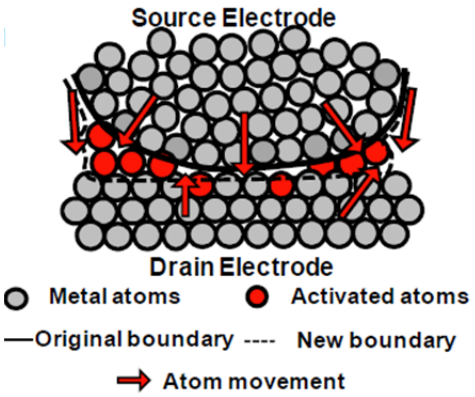


Figure 1.11. Diffusion of thermally activated atoms at the contacting surfaces when the local temperature approaches melting point, eventually filling the void in between the contacting surfaces [27].

A model has been derived to predict the endurance of relays due to micro-welding failure, showing that contacts with high resistance and high activation energy are desirable [27]. Reducing the supply voltage is also desirable, and scaled relays operating at 1 V or lower voltage are predicted to have endurance exceeding 10^{15} ON/OFF cycles without micro-welding failure [27]. Switching of very high voltages should be avoided,as micro-welding remains a key issue for high-voltage NEM switches [12, 28].

1.3.5 ON-state Resistance Degradation

In addition to high endurance, relays must operate at a sufficiently stable R_{ON} to be practical for integrated circuit applications. The primary reason for unstable R_{ON} is non-conductive layer formation on the contacting surfaces, hindering current conduction between source and drain terminals. The thin non-conductive layer comes mainly from native oxide formation when the contacting material is exposed to air, and from polymer buildup due to contaminants from the environment [20, 29]. While polymer buildup can be controlled by hermetically sealed packaging and by applying additional cleaning procedures during the relay fabrication process, the oxide formation issue is inherent to the material property of the contacting material. For prototype relays with W as the contacting material, the native oxide formation, exacerbated by the high local temperature from Joule heating, eventually caused R_{ON} to rise to an unacceptable level [20]. Figure 1.12 shows the Auger electron spectroscopy (AES) results for W contacts before and after cycling, with the W peak attenuated post-switching indicative of the formation of non-conductive native oxide. To address this issue, alternative contacting materials to W are explored in chapter 2 and relays with stable R_{ON} are demonstrated in chapter 3.

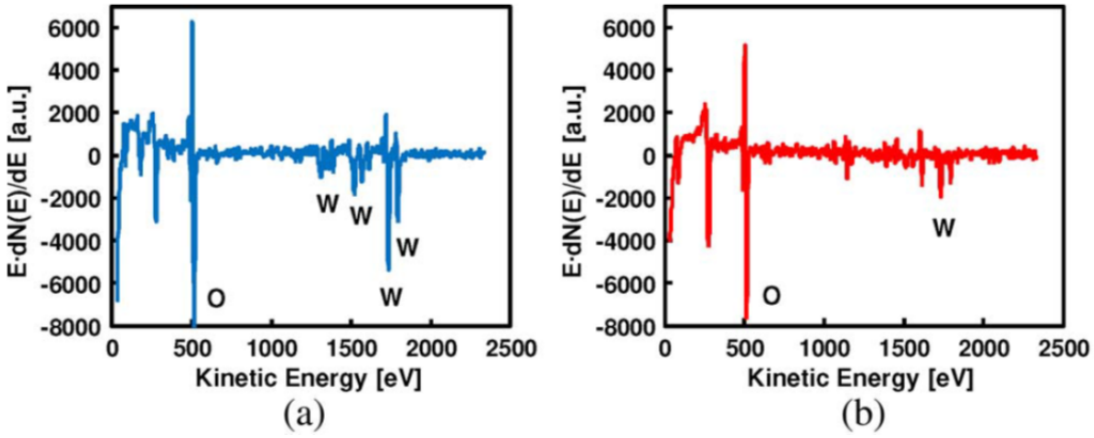


Figure 1.12. AES spectra of the W contacting surface (a) freshly after release process, and (b) after operating 5×10^7 ON/OFF cycles [20].

1.4 Voltage Scaling for Relay Technology

Reduction in relay operating voltage offers several benefits: avoidance of dielectric-breakdown-induced damage during electrical testing; extended relay lifetime due to reduced micro-welding; retarded native oxide formation at the contacts, and reduced energy consumption. The reliability benefits of reduced relay operating voltage were discussed in detail in section 1.3. Since a relay technology essentially consumes zero leakage power, the total power consumption is due to dynamic power and is proportional to V_{DD}^2, which clearly is reduced by lowering the supply voltage.

The key operating voltages to minimize for logic relays are V_{PI} and the hysteresis voltage $V_{PI} - V_{RL}$. V_{PI} reduction can be attained by optimizing the relay design and fabrication process, with techniques and challenges discussed in the literature and chapter 4 [7, 12, 13, 30]. Minimizing hysteresis voltage is beneficial because V_{PI} and V_{RL} of 4-T and 6-T relays can be reduced via body biasing, as shown in Figure 1.13. When a negative voltage is applied at the body terminal, V_{PI} and V_{RL} of are reduced effectively [15, 31]. For proper operation, V_{RL} must be greater than 0 V; thus, the hysteresis voltage sets a lower limit for V_{PI} and hence the supply voltage. Complementary relay-based circuits can also be achieved by applying appropriate body bias voltages to achieve complementary switching of pull-up and pull-down relays [16].

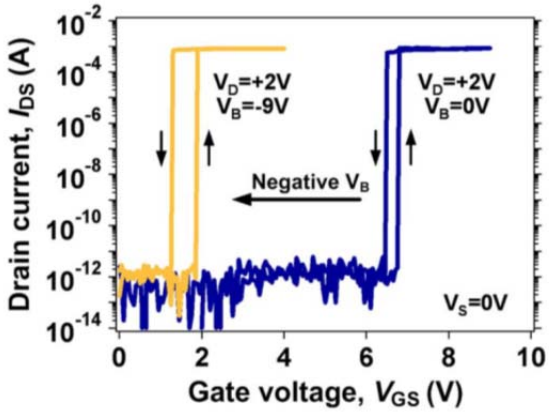


Figure 1.13. Measured I_{DS}-V_G characteristics of a 4-T relay with reduced V_{PI} and V_{RL} via body biasing [12].

1.5 Dissertation Objectives

This dissertation advances logic relay technology to achieve more stable and energy-efficient switching devices for digital logic applications. The reliability and voltage scaling challenges for NEM relays are addressed by material optimization, process integration, and design improvements. The fundamental energy limit for mechanical switches is also investigated and new energy-efficient switch designs are proposed. The remainder of this dissertation is organized as follows.

Chapter 2 examines potential candidates for replacing W as the relay contacting material to improve R_{ON} stability. Requirements for alternative contacting materials, as well as the advantages and disadvantages of each candidate, are discussed based on the typical failure modes. Challenges for integrating new contacting material are identified and overcome via several short flow experiments.

Chapter 3 demonstrates scaled logic relays with ruthenium (Ru) as the contacting material, which offer superior R_{ON} stability when compared to prototype W-contact relays. Fully integrated process flow and relay designs for Ru-contact relays are presented. Successfully fabricated Ru-contact relays are characterized and process improvements are discussed to further improve the stability of Ru-contact relays.

Chapter 4 describes the optimization of the relay structural stack to achieve lower operating voltages suitable for relay-based VLSI circuit implementation. Dimensional scaling and voltage scaling of relays are discussed and interconnect technology for fabricating relay-based circuits is developed.

Chapter 5 models the switching energy of generalized nanomechanical switches and proposes new switch designs to overcome the generally-conceived energy efficiency limit of nanomechanical switches. Conventional and proposed switch designs with similar dimensions are benchmarked using the developed force and energy models. A pathway to experimental demonstration of the energy-efficient switch design is hinted with initial results.

Chapter 6 summarizes the key findings and contributions of this dissertation. Suggestions are offered regarding potential future research directions in NEM relay technology.

1.6 References

[1] G. E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics,* vol. 38, pp. 114-117, 1965.

[2] B. Davari, R. H. Dennard and G. G. Shahidi, "CMOS Scaling for High Performance and Low Power—The Next Ten Years," *Proc. IEEE,* vol. 83, no. 4, pp. 595-606, 1995.

[3] T. Skotnicki, J. A. Hutchby, T.-J. King, H.-S. P. Wong and F. Boeuf, "The End of CMOS Scaling: Toward the Introduction of New Materials and Structural Changes to Improve MOSFET Performance," *IEEE Circuits Dev. Mag.,* vol. 21, no. 1, pp. 16-26, 2005.

[4] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous and A. R. LeBlanc, "Design of Ion-implanted MOSFET's with Very Small Physical Dimensions," *J. Solid-State Circuits,* Vols. SC-9, no. 5, pp. 256-268, 1974.

[5] E. J. Nowak, "Maintaining the Benefits of CMOS Scaling when Scaling Bogs Down," *IBM J. Res. Develop.,* vol. 46, pp. 169-186, 2002.

[6] P. Packan, "Device and Circuit Interactions," in *IEEE IEDM '07 Short Course: Perf. Boosters Adv. CMOS*, Washington, DC, USA, 2007.

[7] R. Nathanael, "Nano-Electro-Mechanical (NEM) Relay Devices and Technology for Ultra-Low Energy Digital Integrated Circuits," in *Ph.D. Dissertation, University of California, Berkeley*, 2013.

[8] H. Esmaeilzadeh, E. Blem, R. St. Amant, K. Sankaralingam and D. Burger, "Dark Silicon and the End of Multicore Scaling," in *Proc. 38th Int. Symp. Computer Architecture*, San Jose, CA, USA, 2011.

[9] K. Kuhn , U. Avci, A. Cappellani, M. D. Giles, M. Haverty, S. Kim, R. Kotlyar, S. Manipatruni, D. Nikonov, C. Pawashe, M. Radosavljevic, R. Rios, S. Shankar, R. Vedula, R. Chaua and I. Young, "The Ultimate CMOS Device and Beyond," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2012.

[10] J. M. Rabaey, "The Swarm at the Edge of the Cloud—A New Perspective on Wireless," in *Symp. VLSI-C*, Honolulu, HI, USA, 2011.

[11] B. Meyerson, "Innovation: The Future of Silicon Technology," in *Semico Impact Conf.*, Taipei, Taiwan, 2004.

[12] V. Pott, H. Kam, R. Nathanael, J. Jeon, E. Alon and T.-J. King Liu, "Mechanical Computing Redux: Relays for Integrated Circuit Applications," *Proc. IEEE,* vol. 98, no. 12, pp. 2076-2094, 2010.

[13] J. Yaung, "NEM Relay Scaling for Ultra-low Power Digital Logic," Ph.D. Dissertation, University of California, Berkeley, 2014.

[14] G. M. Rebeiz, RF MEMS: Theory, Design, and Technology, New York: John Wiley & Sons, 2003.

[15] R. Nathanael, V. Pott, H. Kam, J. Jeon and T.-J. King Liu, "4-Terminal Relay Technology for Complementary Logic," in *IEDM Tech. Dig.*, Washington, DC, USA, 2009.

[16] R. Nathanael, J. Jeon, I.-R. Chen, Y. Chen, F. Chen, H. Kam and T.-J. King Liu, "Multi-input, Multi-output Relay Design for Compact and Versatile Implementation of Digital Logic," in *Int. Symp. on VLSI Technol., Sys. Applications (VLSI-TSA)*, Hsinchu, Taiwan, 2013.

[17] I.-R. Chen, L. Hutin, C. Park, R. Lee, R. Nathanael, J. Yaung, J. Jeon and T.-J. King Liu, "Scaled Micro-Relay Structure with Low Strain Gradient for Reduced Operating Voltage," *Electrochem. Soc. Trans.,* vol. 45, p. 101, 2012.

[18] H. Kam, V. Pott, R. Nathanael, J. Jeon, E. Alon and T.-J. King Liu, "Design and Reliability of a Micro-Relay Technology for Zero-Standby-Power Digital Logic Applications," in *IEDM Tech. Dig.*, Washington, DC, USA, 2009.

[19] F. Chen, H. Kam, D. Markovic, T.-J. King Liu, V. Stojanovic and E. Alon, "Integrated Circuit Design with NEM Relays," in *Proc. IEEE/ACM Int. Conf. Computer Aided Design*, San Jose, CA, USA, 2008.

[20] Y. Chen, R. Nathanael, J. Jeon, J. Yaung, L. Hutin and T.-J. King Liu, "Characterization of Contact Resistance Stability in MEM Relays With Tungsten Electrodes," *IEEE/ASME J. MEMS,* vol. 21, no. 3, pp. 511-513, 2012.

[21] W. R. Ashurst, Y. J. Jang, L. Magagnin, C. Carraro, M. M. Sung and R. Maboudian, "Nanometer-thin Titania Films with SAM-level Stiction and Superior Wear Resistance for Reliable MEMS Performance," in *Proc. IEEE 17th Int. Conf. MEMS*, Maastricht, The Netherlands, 2004.

[22] J. Yaung, L. Hutin, J. Jeon and T.-J. King Liu, "Adhesive Force Characterization for MEM Logic Relays with Sub-micron Contacting Regions," *IEEE/ASME J. MEMS,* vol. 23, no. 1, pp. 198-203, 2014.

[23] B. Jensen, K. Huang, L. L.-W. Chow and K. Kurabayashi, "Adhesion Effects on Contact Opening Dynamics in Micromachined Switches," *J. Appl. Phys.,* vol. 97, p. 103535, 2005.

[24] R. T. Howe and R. Maboudian, "Critical Review: Adhesion in Surface Micromechanical Structures," *J. Vac. Sci. Technol. B,* vol. 15, no. 1, pp. 1-20, 1997.

[25] E. S. Park, J. Jeon, V. Subramanian and T.-J. King Liu, "Inkjet-printed Microshell Encapsulation: A New Zero-level Packaging Technology," in *Proc. IEEE 25th Int. Conf. MEMS*, Paris, France, 2012.

[26] R. Maboudian, W. R. Ashurst and C. Carrao, "Self-assembled Monolayers as Anti-stiction Coatings for MEMS: Characteristics and Recent Developments," *Sen. Actuator A,* vol. 82, no. 1, pp. 219-223, 2000.

[27] H. Kam, E. Alon and T.-J. King Liu, "A Predictive Contact Reliability Model for MEM Logic Switches," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2010.

[28] W. W. Jang, J. O. Lee, J.-B. Yoon, M. S. Kim, J.-M. Lee, S.-M. Kim, K.-H. Cho, D.-W. Kim, D. Park and W.-S. Lee, "Fabrication and Characterization of a Nanoelectromechanical Switch with 15-nm-thick Suspension Air Gap," *Appl. Phys. Lett.,* vol. 92, no. 10, p. 103110, 2008.

[29] L. Chen, H. Lee, Z. J. Guo, N. E. McGruer, K. W. Gilbert, S. Mall, K. D. Leedy and G. G. Adams, "Contact Resistance Study of Noble Metals and Alloy Films using a Scanning Probe Microscope Test Station," *J. Appl. Phys.,* vol. 102, no. 7, p. 074910, 2007.

[30] H. Kam, T.-J. King Liu, V. Stojanovic, D. Markovic and E. Alon, "Design, Optimization, and Scaling of MEM Relays for Ultra-Low-Power Digital Logic," *IEEE Trans. Elec. Dev.,* vol. 58, no. 1, pp. 236-250, 2011.

[31] J. Jeon, R. Nathanael, V. Pott and T.-J. King Liu, "Four-Terminal Relay Design for Improved Body Effect," *IEEE Elec. Dev. Lett.,* vol. 31, no. 5, pp. 515-517, 2010.

Chapter 2

Process Integration Development for a Stable Relay Contacting Material

2.1 Introduction

Micro-relay technology is attractive for overcoming the energy limit for CMOS circuits because it offers zero OFF-state leakage current (I_{OFF}) and perfectly abrupt switching behavior. Previous efforts focused on developing a reliable relay fabrication process [1, 2], prototype circuit demonstrations [3, 4], relay technology scaling [5], and predictive compact modeling [6, 7]. These prototype relays used tungsten (W) as the contacting electrode material because W is a hard refractory metal which has superior resistance to mechanical wear and tear [8]. However, W exposed to air forms non-conductive native oxide which causes ON-state resistance (R_{ON}) to gradually increase so that R_{ON} eventually rises to an unacceptable level. Finding an alternative contacting material that offers stable R_{ON} is important to realize the full potential of relay technology.

In this chapter, potential candidates for stable contacting electrode materials will be investigated. Criteria for selecting suitable contacting material for relay technology are proposed and relevant material properties for each candidate are examined. Based on a previously demonstrated process flow and relay design, challenges for integrating each candidate material into the existing process flow will be identified. Ruthenium (Ru) is an attractive candidate, and solutions for overcoming its unique integration challenges are proposed.

2.2 Advanced Contacting Material Selection

Of the five main failure modes for relays that are discussed in chapter 1, four of them are related to the design and reliability of contacting surfaces. Therefore contacting material engineering is one of the most important aspects for developing a reliable relay technology. In this section, key properties that are desirable for relay contacting material are discussed and potential candidates are identified and examined.

2.2.1 Requirements for Relay Contacting Material

For a reliable micro-relay technology, hard material is desirable due to its superior resistance to mechanical wear and tear. Unlike radio-frequency (RF) MEMS switches, for which R_{ON} must be minimized in order to achieve minimum signal loss, R_{ON} ~ 10 kΩ is considered acceptable for relays designed for digital applications [9]. This is because the switching delay of a relay is dominated by the mechanical movement of the relay rather than the electrical RC delay for charging and discharging load capacitance [10]. The relaxed R_{ON} requirement allows the usage of hard refractive metal and surface coating to improve endurance [2, 11, 12].

A material with high melting point is also desirable to alleviate micro-welding issue for relay technology. Figure 2.1 shows the finite-element simulation results showing high local temperature at a contacting asperity as current flows through it. To avoid micro-welding, the local temperature at asperities must be much lower than the melting temperature of the contacting material. A contacting material with melting point greater than 1500ºC is desirable for achieving relays with high endurance. As indicated in Figure 2.1, higher contact resistance (R_c) is helpful for reducing local Joule heating. This also suggests that low contact resistance is both unnecessary and undesirable for logic relays due to high peak temperature at the contacts. Contact engineering and/or surface coating to increase contact resistance may be required if R_c turns out to be too low for logic relays.

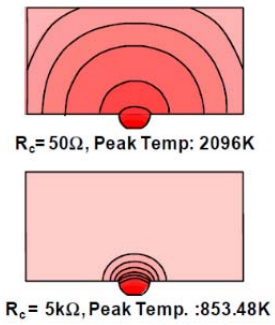


Figure 2.1. ANSYS simulation of temperature contours at asperities due to Joule heating [6].

In order for relays to be suitable for digital logic applications, R_{ON} must be stable within a certain range over the relays' lifetime. Insulating native-oxide formation and hydrocarbon contamination are two primary causes leading to R_{ON} instability because they both form a thin non-conductive layer at the contacting surfaces. Therefore, a contacting material that either does not oxidize in ambient air or forms a conductive native oxide is desirable for relay technology.

Another failure mode related to relay contact engineering is stiction, wherein attractive capillary forces dominate the spring restoring force of a mechanical switch, causing permanent contact closure. To avoid stiction failure, vapor-phase hydrofluoric acid (HF) is used to release the relays fabricated in this work. In turn, the contacting material must withstand the HF vapor release process. For each contacting material candidate, short loop tests are conducted to verify compatibility with HF vapor.

A relay contacting material also should be non-brittle, electrically conductive, and formed using a low-temperature (<410ºC) fabrication process that is compatible with CMOS back-end-of-line (BEOL) metals. A CMOS-compatible process allows relays to be built on top of CMOS BEOL interconnects to form CMOS-relay hybrid circuits. Practically, cost and compatibility with thin-film processing for relay applications also limit material selection.

Figure 2.2 shows the contact resistance and hardness measurements of several noble metals and their alloys that are commonly used as a contacting material in MEMS switches. While the metals and alloys listed here are mainly of interest for RF applications, they serve as a good starting point for identifying possible contacting material candidates for logic applications. Ruthenium, platinum and rhodium will be examined in the subsequent sections with regard to process compatibility.

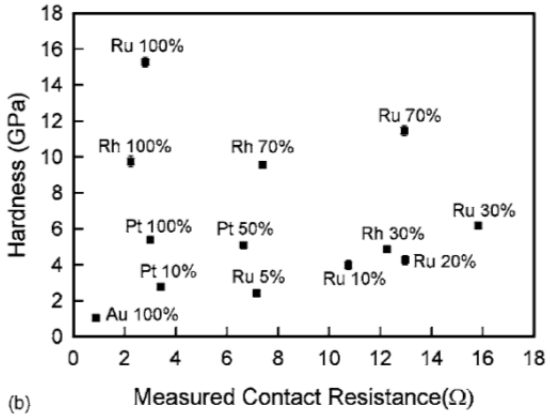


Figure 2.2. Measured contact resistance and hardness at 24 nm indentation depth for metal and metal alloy thin films with 300 nm thickness. Metal alloys are formed by co-sputtering gold (Au) and noble metals [13].

Table 2.1 summarizes relevant bulk material properties for metals under consideration, including platinum (Pt), ruthenium (Ru), rhodium (Rh), iridium (Ir), and osmium (Os). These metals were selected due to their high melting temperature and stability in air and oxidizing environments. These materials are also useful for other thin film applications, including CMOS metal gate technology [14], protective coatings [15, 16], and silicidation [17]. Thanks to these existing applications, thin film deposition and etching techniques for these metals are mostly well-researched and documented. As a reference, W is also listed in Table 2.1 for comparison. W is quite attractive as the contacting material for building prototype relays since it is the metal with highest known melting point, minimizing potential micro-welding and contact vaporization issues [6]. However, W oxidizes in air and forms a native oxide layer that consists of WO_3 and other WO_x compounds [18, 19]. The resistivity of thin film WO_3 is ~30 Ω-m, hindering current conduction at the contacts [20]. In subsequent sections, candidates for replacing W as the contacting material will be examined in depth according to the requirements set forth in this section.

TABLE 2.1

BULK MATERIAL PROPERTIES FOR SELECTED TRANSITION METALS

	W	Pt	Ru	Rh	Ir	Os
Resistivity [nΩ-m]	52.8	105	71	43.3	47.1	81.2
Melting Point [ºC]	3422	1768	2334	1964	2446	3033
Mohs Hardness	7.5	4.0	6.5	6.0	6.5	7.0
Brinell Hardness [GPa]	2.57	0.39	2.16	1.10	1.67	3.92
Native Oxide	WO_x	PtO_x	RuO_2	none	IrO_2	OsO_2

2.2.2 Platinum

Platinum is a widely used transition metal in silicide and in MEMS applications due to its high chemical resistance, relatively high temperature stability and high Young's modulus [21]. The high melting point of Pt, when compared to widely used gold (Au) or aluminum (Al) structures, allows Pt-based RF MEMS devices to be resistant to plastic deformation and to remain highly conductive at elevated temperatures [21]. Pt or Pt-Au alloy are also widely used as contacting materials in ohmic-contact or high power-handling capability switching devices for improved reliability [22, 23]. Pt forms both PtO_2 and, to a lesser extent, PtO in air at room temperature [24]. Both oxide compounds are stable in air and are semi-conductive, with their thin films showing resistivity values ~10^{-5} Ω-m and ~10^{-2} Ω-m for PtO and PtO_2, respectively [25]. Experiments also showed that Pt is resistant to HF vapor used for the relay dry release process.

While Pt possesses several desirable properties for MEMS applications, particularly for RF MEMS devices, there are many challenges for employing Pt as the contacting material in logic relays. Despite the relatively high hardness and high melting point making Pt suitable for RF MEMS applications, these properties are likely insufficient for achieving reliable logic relay operation. Table 2.1 shows that compared to other metals in the platinum group (i.e. Ru, Rh, Ir, Os), Pt is significantly softer and has lower melting temperature. Figure 2.3 shows the contact resistance degradation of Au-Pt contacts during hot-switching events in various environments and current levels. The result shows extremely poor contact resistance stability for Au-Pt contacts at high current levels [26]. While controlling current through contacts below 30 μA (R_{ON} ~ 100 kΩ) can lead to improved contact resistance stability, such high resistance is undesirable for logic applications. Alternatively, Pt contact resistance stability may also be improved by controlling an inert ambient around Pt-contact switches. However this approach will not be explored in the scope of this work. Figure 2.4 shows the scanning electron microscopy (SEM) image of the contacting region in a Pt-coated ohmic-contact micro-relay after switching. Physical damage is clearly visible on the contacting surface, indicating Pt is susceptible to physical wear and tear due to its relatively low hardness. Electrical results show R_{ON} degradation after 100 and 10^5 cycles in O_2 and N_2 environments, respectively.

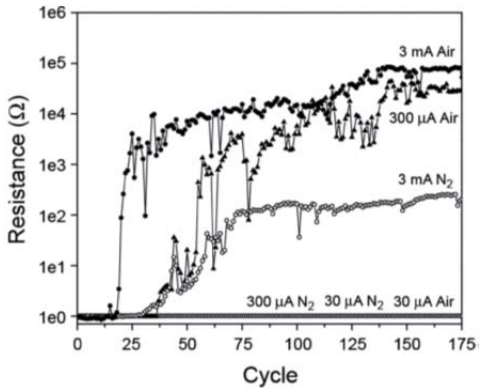


Figure 2.3. Contact resistance degradation characteristics for Au-Pt alloy contacts in a nanoindentation apparatus [26].

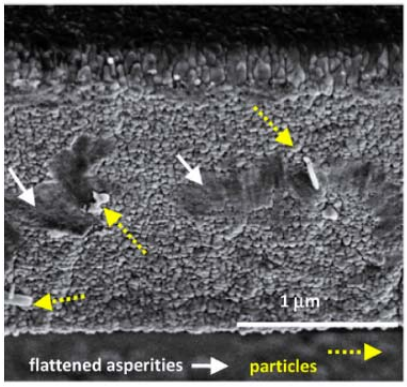


Figure 2.4. SEM micrograph of the contact bar in a Pt-contact switch with damage sites labeled. Similar surface damages were observed for devices tested in pure O_2 and N_2 environments [27].

2.2.3 Ruthenium

Ruthenium, RuO_2 and Ru-alloys have been investigated for several solid-state switch and memory applications, including for the metal gate stack in advanced CMOS and memory technology due to desirable work function, good resistivity and excellent thermal stability [28, 29]. Ru has also been widely used as the wear-resistant coating material on macroscopic electro-mechanical switches via either electroplating or sputtering [30]. For example, reed switches with Ru-coated contacting lead have been verified to exhibit excellent reliability characteristics, particularly for applications which require high current handling capability [31]. Despite its success in macroscopic switch contacts, Ru was only employed in a limited number of microscopic switches demonstrated in the literature.

With the combination of excellent conductivity, high melting temperature, and high hardness, Ru is an attractive contacting material candidate for addressing current handling, thermal stability and contact reliability issues in MEMS resistive switches [32, 33]. Ru is also extremely stable in air and resistant to most corrosive agents. In a comparison between Ru-Ru and traditional Au-Au contacts for high-power RF MEMS switches (Figure 2.5), Ru-contact switches show higher contact resistance but ~10x better lifetime characteristics for hot-switching, wherein current flows during contact detachment [32].

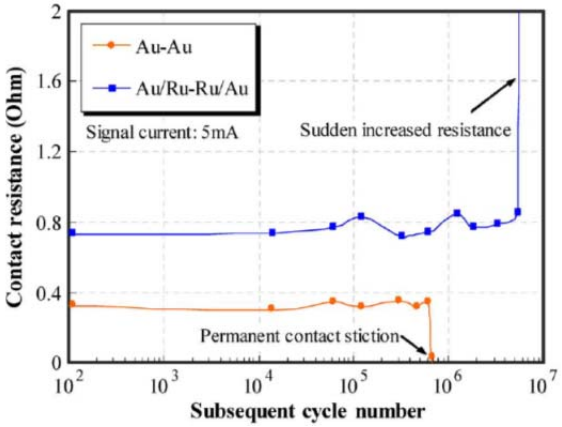


Figure 2.5. Comparison of contact resistant change over switching cycles of RF MEMS switches with Au-Au and Ru-Ru contacts [32].

In addition to superior hardness and thermal stability, a unique advantage for Ru as the contacting material is its conductive native oxide RuO_2. The resistivity of RuO_2 thin film has been characterized to be 4×10^{-7} Ω-m, about one order of magnitude higher than the metals considered in Table 2.1 [34]. This implies that while RuO_2 may be too resistive for conducting large current in the bulk channel, a thin layer of RuO_2 at contacting surfaces is unlikely to induce significant resistance penalty. It is reported that the contact resistance penalty is negligible for up to 25Å of RuO_2 thin layer on Ru bulk material [31]. In addition, RuO_2 is a very hard material (Mohs hardness 8) that has found practical applications as a wear resistant protective coating material.

Short flow experiments were designed to evaluate and address several process integration challenges for employing Ru as the relay contacting material. The results of integration experiments are detailed in Section 2.3.

2.2.4 Titanium Nitride

Other than elemental metals, wear-resistant ceramic materials are also interesting for NEMS switch applications. Titanium nitride (TiN) is one of the widely used protective coating materials used for high-temperature environments due to its high melting point (2930ºC), extreme hardness (Mohs hardness 9.0) and excellent chemical and thermodynamic stability. In addition, the electrical and thermal properties of TiN are similar those of metals, making it a very interesting candidate for many microelectronics applications. The most common application of TiN takes advantage of its low diffusivity to serve as a diffusion barrier material. TiN also has been explored for tunable-work-function metallic gate electrodes, self-aligned local interconnects, etch-stop and adhesion layers, etc. [35, 36]. The widespread adoption of TiN in various applications has led to a large body of existing knowledge for TiN thin film processing.

More recently, TiN has been investigated for the structural and contact materials of NEMS switches due to its unique combination of electrical, mechanical and thermal properties. From a reliability perspective, the high fracture strength and yield strength of TiN are beneficial for improving mechanical device endurance; the high hardness is helpful in reducing contact wear and tear; the high melting point and low surface adhesion energy (due to passivated surface) are important for resisting contact stiction [37, 38]. TiN also exhibits excellent chemical stability when exposed to pollutants, maintaining low contact resistance and no surface chloride or sulfide contamination [37]. Several NEMS switch applications utilizing TiN have been demonstrated, showing zero OFF-state current, high ON/OFF current ratio, and abrupt switching behavior [39, 40].

The deposition of TiN thin films can be achieved by many different methods, including reactive evaporation, sputtering, and chemical vapor deposition (CVD) [35]. The CVD process requires high temperature and therefore is not compatible with CMOS BEOL metals. The properties and purity of sputtered TiN film can vary significantly with the deposition condition, with resistivity in the range 25-160 μΩ-cm (10-100x higher than most metals discussed) [35]. Deposition can be performed by reactive sputtering using a Ti target in a N_2 rich environment, or directly using a pure TiN compound target for higher purity and improved density. Residual stress is a significant problem in NEMS devices since they lead to significant out-of-plane deflection of released structures. Fortunately the residual stress of TiN film can be relieved by an appropriate thermal annealing process, as shown in Figure 2.6 [38]. The low-stress TiN film investigated in this section was deposited by direct sputtering and the sheet resistance was found to be ~10 Ω/square for a 100 nm-thick film.

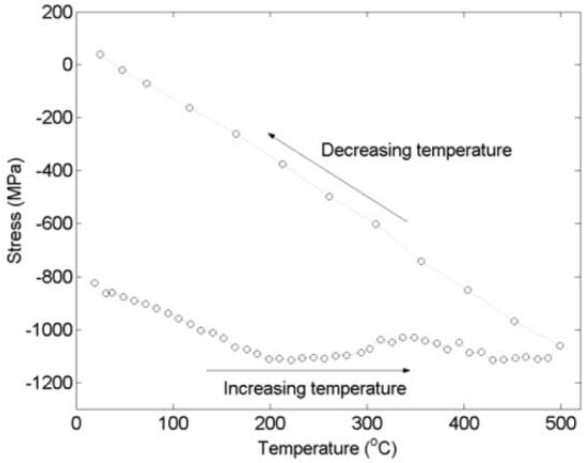


Figure 2.6. Stress evolution of TiN thin film during thermal annealing process up to 500ºC [38].

Several experiments were run to develop a fully integrated process flow for fabricating relays with TiN as the contacting material. The plasma etch process development is highlighted here using an Applied Materials Centura decoupled plasma source (DPS) etcher. While plasma etching of TiN thin films has been widely studied for microelectronics applications and many etch gas combinations (e.g. SF_6/Ar, CF_4/O_2, Cl_2/BCl_3, $Cl_2/CHF_3/N_2$/Ar) have been verified to be effective, the Cl_2-based chemistry was selected for development in the UC Berkeley Marvell Nanofabrication Laboratory due to better selectivity to the silicon dioxide (SiO_2) layer underlying the relay channel [41]. Figure 2.7 shows the etch rate for TiN and SiO_2, as well as TiN/SiO_2 etch selectivity with varying bias power. Etch selectivity can be significantly improved at low bias power with moderately decreased etch rate [41]. It is also reported that increasing Cl_2 flow leads to higher etch rate without significant impacting selectivity, but the benefit saturates at ~100 sccm of Cl_2 flow. Table 2.2 summarizes the etch development process in the Centura DPS etcher, showing the best result at 500 W source power, 50 W bias power, 10 mTorr chamber pressure, and 100 sccm Cl_2 flow (experiment #4). Note that to mimic the existing relay fabrication process, the SiO_2 used in the development process is the low temperature oxide (LTO) deposited by a Tystar low-pressure chemical vapor deposition (LPCVD) furnace at 400°C. The etch rate for LTO is expected to be much faster than for thermal SiO_2 in a plasma etcher. TiN/Al_2O_3 etch selectivity was also measured in experiment #4, as Al_2O_3 is used as the substrate insulator material. While Figure 2.7 suggests that a bias power lower than 50 W may be beneficial, the etch process aborted in the Centura DPS etcher due to high reflected power of the matching network (experiment #5).

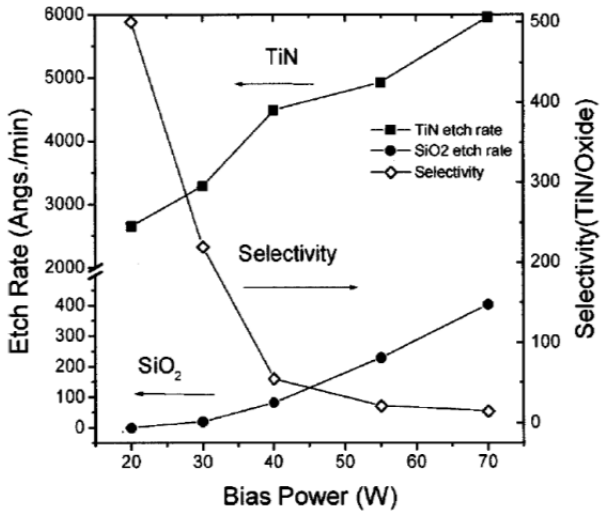


Figure 2.7. TiN and SiO_2 etch rate and TiN/SiO2 selectivity with respect to bias power in a high density helicon-wave plasma etcher. Source power is at 1900W, Cl_2 = 70 sccm, and chamber pressure is at 5 mTorr [41].

TABLE 2.2

ETCH DEVELOPMENT EXPERIMENTS FOR TITANIUM NITRIDE

	#1	#2	#3	#4	#5
Source Power [W]	500	500	500	500	500
Bias Power [W]	100	50	100	50	20
Pressure [mTorr]	20	20	10	10	10
Gas Flow [sccm]	Cl_2 = 100	Cl_2 = 100	Cl_2 = 100	Cl_2 = 100	Cl_2 = 100
TiN Etch Rate [nm/sec]	Etch failed (high refl. power)	Etch failed (high refl. power)	2.583	3.097	Etch failed (high refl. power)
LTO Etch Rate [nm/sec]			1.380	0.800	
TiN/LTO Selectivity			1.87	3.87	
Al_2O_3 Etch Rate [nm/sec]			N/A	0.362	
TiN/Al_2O_3 Selectivity			N/A	8.56	

Relays with TiN as the contacting material were fabricated using the etch recipe developed here. The fabricated relays were released using the Idonus HF vapor etch system. Figure 2.8 shows the measured I-V characteristics of a typical TiN-contact relay. Unfortunately, no source-drain current (I_{DS}) was found even at V_{DS} = 20 V. The gate current (I_G) increased to ~100 pA at V_G > 15 V, indicating that the relay structure is intact and can actually be actuated. The I_G leakage was through the Al_2O_3 body insulator when the body structure collapsed onto gate electrode at very high V_G. The results implied that the structure of relay was likely fabricated successfully but the contact area was either destroyed or transformed into an insulating film.

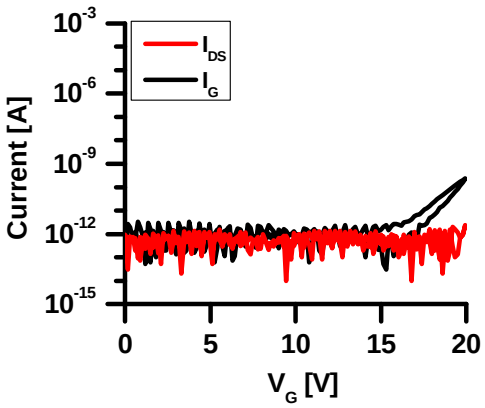


Figure 2.8. Typical measured I-V characteristics of TiN-contact relays, showing I_{DS} below noise limit at V_{DS} = 20 V.

Figure 2.9 shows the micrographs of TiN-contact relays before and after the release process. It is clear that the smooth, reflective TiN film of the electrode layer in Figure 2.8a had been attacked and transformed into a rough film in Figure 2.8b. The resistance between two measurement probes landing on the same probing pad was measured to be larger than 30 Ω, which was at least 1000x larger than for W or Ru probing pads under the same measurement condition. Since the electrode layer consisted of 70 nm of bottom W and 10 nm of top TiN layers, the TiN layer apparently was transformed into an insulating material instead of being etched away by HF vapor during the release process. Relays from the same lot were later released in the SPTS Primaxx µEtch System using anhydrous HF at reduced chamber pressure. The newer release system limits the water by-product and significantly improves etch selectivity. However the release process via the µEtch system yielded no improvements for TiN-contact relays in metrological and electrical measurements. Therefore, TiN was deemed incompatible with existing relay fabrication process. It is worth noting that TiN may still be an attractive candidate for hard contacts if the fabrication process does not involve HF.

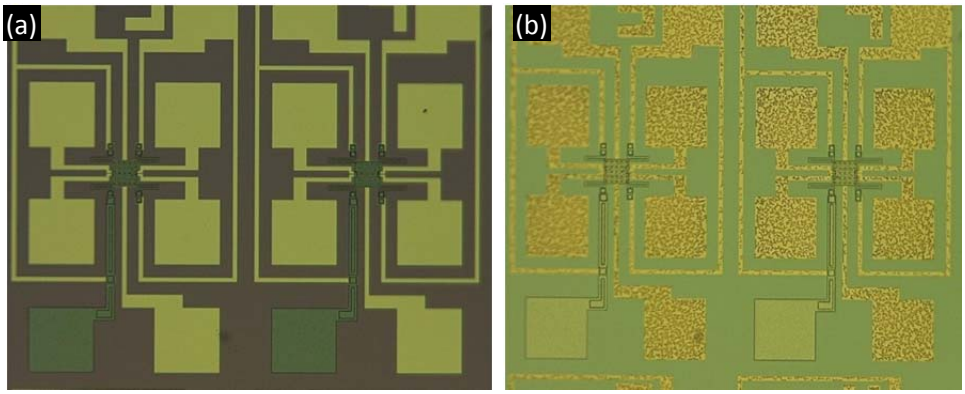


Figure 2.9. Micrographs of fabricated TiN-contact relays (a) before HF vapor release process and (b) after HF vapor release process. TiN electrode layer, including probe pads, interconnect traces, and contact landing regions are visibly attacked during the release process.

2.2.5 Other Candidates

Several other metals with high melting point and high hardness, and which either form no native oxide or form a conductive native oxide, were considered as potential contacting material for relay technology. The advantages and concerns of these platinum group metals, including Rh, Ir, and Os, will be discussed in depth in this section. However, each of these materials was deemed unsuitable after further investigation. It is also worth noting that these materials are extremely rare and at least 10x more expensive than Ru (and Ru is ~30x more expensive than W). For example, Ir is one of the ten least abundant stable elements in the earth's crust, which may be a concern for mass production.

Rh is a hard, inert material that is commonly used as the coating material for optically reflective surfaces, showing excellent resistance to most corrosive agents and aggressive chemicals. Rh also has been investigated as a potentially attractive contacting material in early studies for micro-relay actuators [42]. For micro-scale applications, Rh can be deposited or coated via electroplating, evaporation, or magnetron sputtering [43]. Due to its chemical inertness, Rh is difficult to oxidize even at high temperature (e.g. >1000ºC) or in strong chemical (e.g. electroplating solution) environments [31, 44]. Theoretically, relay operation will not cause R_{ON} to change for Rh-contact devices due to lack of native oxide, eliminating one of the most significant failure modes. However, it is also extremely difficult to etch Rh, which is essential for cost-effective manufacture of NEM relays. Unlike Ru, Rh does not form volatile products in plasma, therefore it is extremely difficult to dry-etch Rh layers for microelectronics applications. The only known chemical to wet etch Rh effectively is aqua regia, which will attack most of the other materials present in the relay structure [45]. It is important to point out that Rh may be an attractive candidate for relay contacting material if an effective plasma etching technique can be developed.

Ir and Os are attractive candidates for relay contacting material due to their conductive native oxides. IrO_2 exhibits the lowest resistivity (~3×10^{-7} Ω-m) of metal oxides among platinum group metals, while OsO_2 resistivity is roughly 6×10^{-5} Ω-m [46, 47]. Os and Ir are also the two stable elements with highest density, which is interesting for optical, metallurgical, sensing, and physical applications. Ir is also extremely resistant to acid corrosion and cannot even be attacked by boiling aqua regia (except under high pressure). Therefore Ir is an important material for wear and corrosion resistant coating applications [48]. In microelectronics, Ir and IrO_2 have been considered for dynamic random access memory (DRAM), ferroelectric random access memory (FeRAM), and more recently, as the contacting material for MEMS switches [49, 50]. On the other hand, Os thin film applications have been rather limited due to process difficulty and the extreme toxicity of one of its oxides, OsO_4 [51]. Both physical and chemical vapor deposition methods have been investigated for Ir and Os deposition, and atomic layer deposition (ALD) precursors have been developed [50, 51]. The main concern for Ir and Os is that they are brittle, thus many of their applications involve alloying instead of using pure metals. While it might be interesting to investigate possible Ir- or Os-alloy compositions for an attractive relay contacting material, alloy contacts will not be pursued here due to process complexity. Additionally, Ir contacts may be susceptible to carbon contamination. Figure 2.10 shows contact degradation of Ir-contact RF MEMS switches, which is detrimental for switching applications [52].

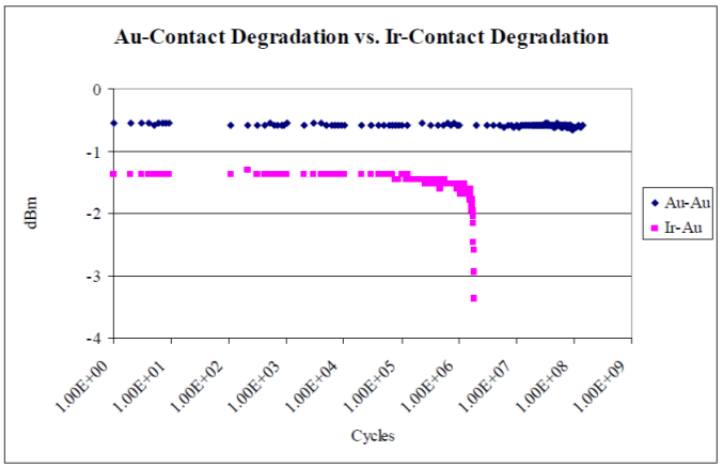


Figure 2.10. Comparison of contact resistant change over switching cycles of RF MEMS switches with Au-Au and Ir-Au contacts. The main failure mode is permanent adhesion for Au-Au contact switches whereas it is contact resistance degradation due to carbon contamination for Ir-Au contact switches [52].

2.3 Integration of Ruthenium as Contacting Material

Ru has been identified as the attractive candidate to replace W as the contacting material for NEM relays. Incorporating Ru into an existing relay process flow, however, proved to be very challenging in many aspects. Several short-flow experiments were designed to overcome these process integration challenges including deposition, adhesion, lithography, etching, etc. This section identifies key challenges and discusses these integration efforts for achieving a fully integrated process flow for fabricating Ru-contact relays.

2.3.1 Deposition

The Ru thin films in this work were deposited in the Randex sputtering system in the Marvell Nanofabrication Laboratory. The high-vacuum base pressure of the Randex system was typically 2-5 μTorr after more than 2 hours of pump-down using cryogenic pumping system. The DC sputtering forward power was set at 300 W while the reflective power was typically below 10 W. Deposition pressure was tuned by varying argon (Ar) gas flow.

Unfortunately, the initial deposition experiments yielded poor results. Table 2.3 summarizes the Ru deposition results for a selected number of samples, with deposition pressure set at 3 mTorr. Ru thin film samples were deposited on LTO to mimic deposition of the channel Ru layer. Figure 2.11 shows an example of a cracked Ru film on LTO, similar to the Ru film in samples #1-5. For a Ru layer thicker than ~20 nm, Ru cracked and delaminated from underlying LTO upon exposure to DI water. This result indicated that Ru layer thickness must be extremely limited to approximately 10 nm if no post-deposition treatments are performed. For a Ru layer thicker than ~60 nm, the film may crack and delaminate simply by exposing Ru to air ambient, presumably due to moisture present in air. Therefore Ru deposition will be limited to ~60 nm thickness on LTO even with post-deposition treatments discussed later in this section. Ideally, the Ru film should exceed 10 nm in thickness to guarantee good coverage (i.e. a continuous film) over the contact dimples.

TABLE 2.3

SELECTED RUTHENIUM DEPOSITION RESULTS ON LOW-TEMPERATURE OXIDE

Sample	Power	Dep. Pressure	Ru Layer Thickness	Results
#1	300 W	3 mTorr	~ 120 nm	Film cracked immediately after deposition
#2			~ 90 nm	Film cracked in shortly after air exposure
#3			~ 60 nm	Film cracked after 2 days in air
#4			~ 30 nm	Film cracked after exposure to water
#5			~ 20 nm	Film cracked after exposure to water
#6			~ 10 nm	OK

Figure 2.11. Picture of a cracked Ru film deposited on LTO after air exposure.

The possible reasons behind Ru film delamination have been investigated and studied. One plausible explanation is due to the high residual stress present in sputtered Ru films. It is reported that the residual stress of a sputtered Ru film varies significantly with deposition conditions such as DC power, bias power, deposition pressure, and substrate temperature [33]. Since the Randex system does not offer the capability to modify bias power or substrate temperature, the available knobs for process tuning are DC power and deposition pressure. Figure 2.12 shows the residual stress of Ru films with varying power and deposition pressure, with ~4 mTorr being the ideal deposition pressure for low-stress Ru film.

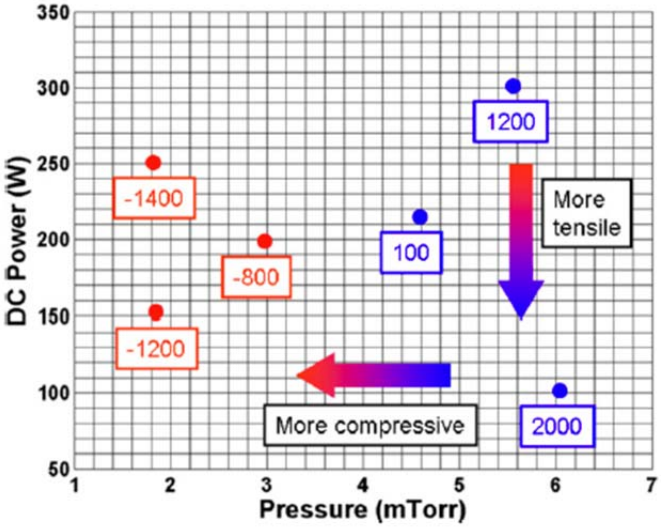


Figure 2.12. In-plane residual stress of sputtered Ru films deposited at different deposition pressures and power levels. Deposition was completed at 25ºC [33].

Table 2.4 summarizes selected Ru deposition results with various adhesion layers added between LTO and Ru, as well as post-deposition anneal treatment for relieving residual stress. It also shows the result for Ru deposition on an ALD Al_2O_3 underlying layer (sample #1), which is important for Ru electrode layer integration. It was observed that sputtered Ru film does not delaminate on Al_2O_3 even when the film was fairly thick (up to 300 nm). ALD Al_2O_3 was initially selected as the adhesion layer, but was later replaced by 3 Å of ALD TiO_2 to improve R_{ON} of Ru-contact relays. It was found that 20 nm of Ru usually can be safely deposited on LTO/TiO_2, although minor delamination occurred in one instance. To further alleviate the cracking and delamination issue, post-deposition anneal was performed (sample #5). It is reported that 400ºC may provide sufficient energy for Ru atoms to become mobile and relieve residual stress [33]. The annealing process was performed in a low-vacuum annealing chamber since a furnace anneal was not possible due to the pre-furnace wafer cleaning requirement (rinsing in deionized water).

TABLE 2.4

SELECTED RUTHENIUM DEPOSITION RESULTS WITH ADHESION LAYER AND THERMAL ANNEAL

Sample	Underlying Layer	Adhesion Layer	Ru Layer Thickness	Anneal	Result
#1	Al_2O_3	None	300 nm	None	OK
#2	LTO	1 nm Al_2O_3	60 nm	None	OK
#3	LTO	3 Å TiO_2	60 nm	None	Cracked with water
#4	LTO	3 Å TiO_2	20 nm	None	Mostly OK
#5	LTO	3 Å TiO_2	20 nm	400ºC 30 min.	OK

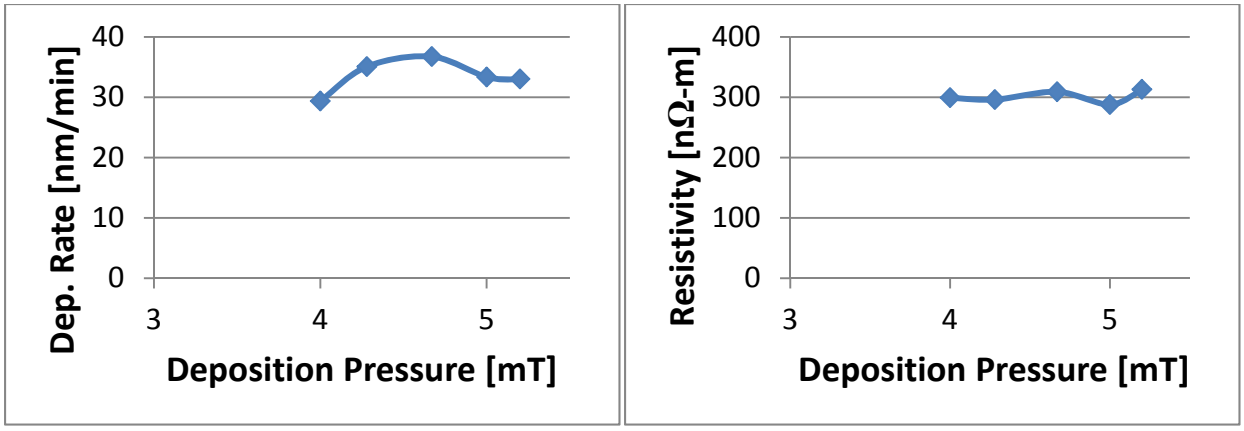


Figure 2.13. Deposition rate and resistivity of deposited Ru thin film, as a function of deposition pressure.

Figure 2.13 shows the deposition rate and film resistivity dependence of Ru films deposited using the Randex sputtering system. The Ru deposition rate is stable at ~30 nm per minute for deposition pressure below 4 mTorr, and slightly increases to ~35 nm per minute for pressure higher than 4 mTorr. The resistivity of Ru thin films deposited with pressure >4 mTorr is approximately 300 nΩ-m, which is ~4x higher than the bulk value.

To summarize, Ru sputtering deposition is best performed with 300 W DC forward power and 4 mTorr deposition pressure, which yields deposition rate at ~30 nm per minute. Ru layer thickness should be limited to 20 nm when deposited onto LTO, with 3 Å of TiO_2 inserted between Ru/LTO as adhesion layer. Post-deposition vacuum anneal (400ºC, 30 minutes) should also be performed immediately after deposition.

2.3.2 Etching

Ru and RuO_2 thin films are typically etched in O_2-containing plasma, forming the volatile by-product RuO_4 [53, 54]. Chlorine-based and fluorine-based plasma etch recipes are generally ineffective since the etch by-products $RuCl_3$ (decomposition temperature >500ºC before melting) and RuF_5 (boiling point 227ºC) are difficult remove near room temperature. The etching mechanism of Ru/RuO_2 in O_2-plasma has been widely studied for its potential application in advanced CMOS gate stacks, with multiple reports showing that a small percentage of Cl_2, CF_4, CF_3CFH_2 or N_2 addition in O_2 plasma strongly enhances the etch rate [53, 55]. The increase in Ru etch rate strongly correlates to an increase in measured O radical density, particularly for fluorine-based gas additions [53]. Among all gases above, Cl_2 is the most popular secondary etchant for etching Ru thin films. Figure 2.14 shows that O_2:Cl_2 = 4:1 ratio yields the highest etch rate, however the correlation between etch rate and O radical density is much weaker compared to fluorine-based gas addition. While the exact etching mechanism of O_2/Cl_2-containing plasma is unclear, it is believed that both O- and Cl-containing species participate in the etching kinetics as Ru oxychloride ions are detected during the etching process [54]. Oxygen ions and radicals remain to be the main etchant for generating volatile Ru compounds even with the addition of Cl_2, but Cl-containing ions play an important role in enhancing volatile by-product formation. It is also worth noting that RuO_4 by-product in the etching process is extremely toxic, and thus proper pumping system is essential.

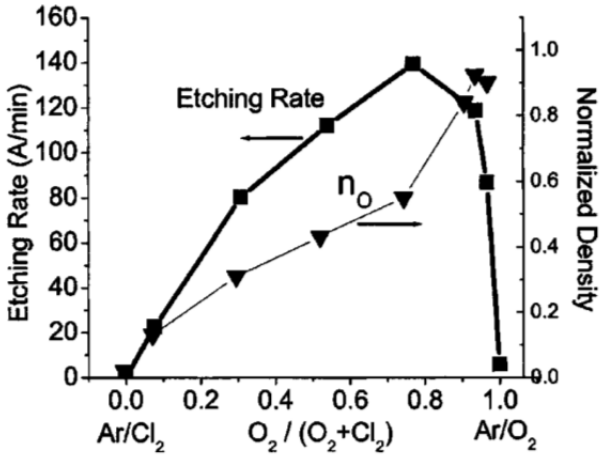


Figure 2.14. Ru etch rate and normalized oxygen radical density at various O_2/Cl_2 gas mixture. Other etch conditions are 150 W source power, 10 mTorr pressure, 15 sccm Ar, and 39 sccm total gas flow (O_2 + Cl_2). The oxygen radical density was measured by actinometry [54].

Aside from secondary gas additions, other parameters such as power, pressure, and gas flow rate can all affect Ru etch. High density plasma is crucial for Ru etching, thus high source power is desirable for creating high O radical density. Since Ru etching is highly ion-controlled, a high bias power (thus higher ion flux and higher ion energy) is known to increase the etch rate. For relay fabrication, however, selectivity to LTO and Al_2O_3 is considerably more important than simply a high etch rate. A slightly lower bias power can yield significantly better selectivity to oxide while only modestly sacrificing etch rate [56]. It is also found that a high total gas flow rate is important for Ru etching since it enhances by-product removal, and is beneficial for improving etch rate, sidewall angle, facet loss, and Ru-to-oxide selectivity [56, 57]. The effect of varying chamber pressure is more complicated, as lower pressure helps attaining better sidewall angle but leads to higher faceting [57].

Ru etching was performed using the Applied Materials Centura DPS etcher, which is capable of producing high-density plasma at low pressure. Selected etching results are summarized in Table 2.5. Etch rate was characterized and Ru-to-LTO and Ru-to-Al_2O_3 selectivity was measured. In all cases, excellent Ru-to-Al_2O_3 etch selectivity was found and the Al_2O_3 etch rate was negligible using Ru etching recipes. High source power at 1400 W and high total gas flow rate of 200 sccm were selected based on the capability of the DPS etcher. High etch rate and good selectivity to LTO were verified for 80% O_2 / 20% Cl_2 gas mixtures, with the etch rate ~3x higher than the etch rate with 100% O_2 flow. In summary, the optimal etch recipe for Ru uses 1400 W source power, 100 W bias power, 20 mTorr chamber pressure, 160 sccm O_2 and 40 sccm Cl_2 flows (sample #5). While a higher etch rate is possible by increasing the bias power, the selectivity to LTO is degraded.

TABLE 2.5

SELECTED RUTHENIUM ETCHING RESULTS

Sample	Source Power [W]	Bias Power [W]	Pressure [mTorr]	O_2 [sccm]	Cl_2 [sccm]	Etch Rate [nm/min]	Ru/LTO Selectivity
#1	1400	100	10	0	200	Negligible	N/A
#2				40	160	6	~0.3
#3				160	40	50	>10
#4				200	0	15	N/A
#5			20	160	40	55	>10
#6			30	160	40	Etch Failed	
#7		200	20	160	40	65	>5

Despite the success in developing Ru deposition and etching recipes, one issue arose during Ru etching development. Substantial surface leakage current was observed in the surface leakage test structure shown in Figure 2.15. Zero surface leakage is required for practical relay applications, but the leakage current was observed to be nearly 1 pA for a 1 μm gap between two Ru electrodes biased at 10 V. It was suspected that conductive etching by-product redeposited onto the surface. RuO_4 is known be unstable and can easily decompose back to Ru or RuO_2, as these decomposed residues can often be found in the etching chamber or pumping system foreline. The decomposition and redeposition is particularly bad for etching Ru in O_2/Ar plasma, while the effect is much subdued when Cl_2 is added to the gas mixture [54]. Post-etching cleaning recipes were developed to remove the decomposed residues and the results are summarized in Table 2.6. Although HF did not attack Ru, Al_2O_3 was attacked in sample #3 by diluted HF solution (49% HF diluted by 20x). Diluted hydrochloric acid (HCl) and hydrogen peroxide (H_2O_2) solution was found to be the most effective, with chemicals diluted by HCl:30%-H_2O_2:H_2O = 1:1:20.

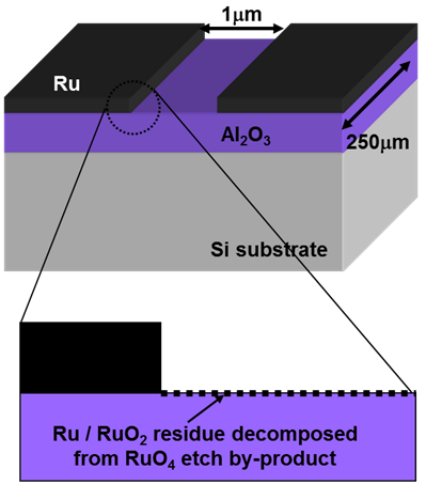


Figure 2.15. Test structure for measuring surface leakage between two Ru electrodes. The origin of surface leakage is also shown.

TABLE 2.6

RUTHENIUM SURFACE LEAKAGE DUE TO ETCH RESIDUE

Sample	Cleaning	Time	Al2O3	Ru	Leakage (10 V Bias)
#1	None		OK	OK	700 fA
#2	UV Exposure	10 min.	OK	OK	500 fA
#3	Diluted HF	<5 sec.	Attacked	OK	1.6 pA
#4	Diluted HCl/H_2O_2	3 min.	OK	OK	140 fA

2.3.3 Lithography

In the relay fabrication process, thin film layers are patterned using Rohm Haas UV 210-0.6 positive photoresist as the masking layer. Unfortunately, the photoresist is not compatible with Ru thin film due to two main issues. First, soft-baked photoresist does not adhere well to a Ru layer. Features with large aspect ratio frequently peeled off during photoresist development. This limited the aspect ratio for thin Ru lines, especially for features with linewidth narrower than 1 μm. Second, hard-baked photoresist on Ru layer is extremely difficult to remove without detrimental effects to the patterned Ru layer. Dry ashing of photoresists using O_2 plasma etches Ru due to the presence of oxygen radicals. Although the etch rate is much slower due to lower power, thin Ru lines <1 μm can still be eroded by O_2 plasma as shown in Figure 2.16. Wet etching is also ineffective in removing photoresist, as shown in Figure 2.17. Photoresist residues remained on Ru patterns even after 24 hours of exposure to commercially available PRS-3000 photoresist stripper solution.

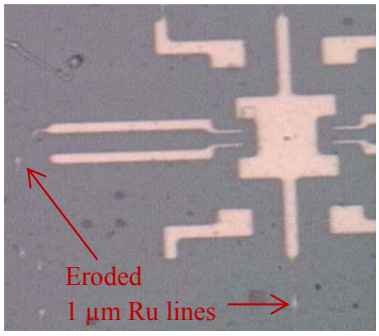


Figure 2.16. Micrograph of patterned Ru layer after photoresist dry ashing in O_2 plasma. Thin Ru lines were etched away by O_2 plasma.

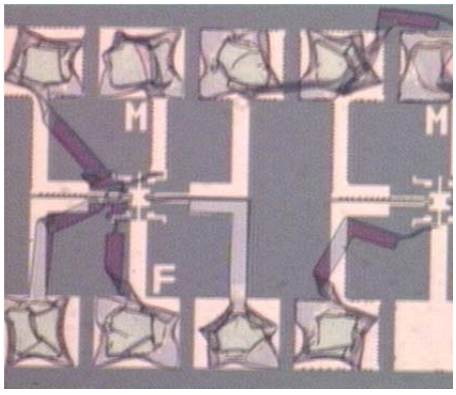


Figure 2.17. Micrograph of Ru layer after 24 hours of photoresist wet stripping. Photoresist residues were clearly present on Ru patterns.

To resolve photoresist compatibility issues, a hard mask is clearly necessary to properly pattern Ru layers. For the channel Ru film (deposited on LTO), the hard mask selection process and other process integration efforts pertaining to the channel layer will be discussed in section 2.3.4. For the electrode Ru film (deposited on Al_2O_3), LTO (deposited at 400ºC in a LPCVD furnace) is an ideal candidate for the hard mask. Mask patterns were transferred to the LTO layer using regular photoresist as the masking layer. Since O_2 plasma is detrimental to Ru, photoresist was removed using PRS-3000 photoresist stripper solution after dry etching LTO layer. It was found that the oxide etching process does not lead to photoresist crosslinking like the Ru etching process, thus photoresist can be easily removed. Ru was then etched using the recipe detailed in section 2.3.2 to transfer the patterns from the LTO hard mask layer to the Ru layer. Finally, the LTO hard mask was removed in the HF vapor system to completely transfer the patterns on the mask to the electrode Ru layer. Another advantage of using LTO as the hard mask is that the residual stress of Ru film can be relieved at 400ºC in the LPCVD furnace, allowing LTO to be deposited onto Ru without delamination. It was observed that depositing oxide at a lower temperature (e.g. plasma-enhanced CVD oxide at 300ºC) led to hard-mask delamination. It is also important for the photoresist-LTO-Ru pattern transfer process to be completed as soon as possible after Ru deposition to avoid potential delamination and cracking issues.

2.3.4 Channel Ruthenium Process Integration Challenges

The integration of Ru as the metallic channel material proved to be a significant challenge. Ru-to-SiO_2 adhesion issues, as discussed in section 2.3.1, required an ultra-thin adhesion promotion layer (i.e. 3 Å TiO_2 via ALD) between channel Ru and sacrificial LTO layers and limited the channel Ru thickness to ~20 nm. Such thin Ru film may have step coverage issues and may induce substantial R_{ON} penalty between source/drain terminals. Thus, a thicker metal layer must be added on top of Ru to improve R_{ON}. Furthermore, hard mask is required to etch Ru. LTO is not a viable hard mask candidate for channel Ru as LTO removal process cannot selectively etch the hard mask without attacking sacrificial layers.

A 70 nm W layer was proposed to serve as both the current conduction layer and the hard mask for etching Ru. The dry etching process for Ru was found to be very selective to W, and the W "hard mask" can simply remain on Ru after etching the channel Ru to facilitate current conduction in the channel. However, a W layer adheres poorly to Ru and delaminates from Ru. Figure 2.18 shows an example of delaminated W film on Ru after etching. Note that the W layers did not delaminate immediately after deposition; instead delamination generally occurred after exposure to liquid.

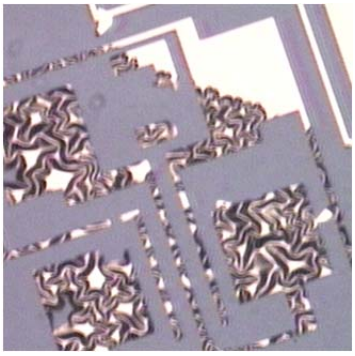


Figure 2.18. Micrograph showing W film delamination when deposited onto Ru in a short-flow experiment. The delaminated film can still be patterned although the traces became highly resistive.

Table 2.7 summarizes a series of short-loop experiments that were conducted to overcome this problem. In order for W to adhere well to Ru, carefully designed thermal annealing must be performed both after Ru deposition and after W deposition to relieve the residual stress in the channel metal films [58]. In the end, a bi-layer channel comprising a thin (15 nm) Ru bottom layer and a thicker (70 nm) W top layer—each vacuum annealed for 30 minutes at 400ºC—was found to be compatible with the subsequent relay fabrication process steps.

TABLE 2.7

SHORT-LOOP EXPERIMENTS TO MITIGATE RUTHENIUM CHANNEL INTEGRATION ISSUES

Process	3Å TiO_2	Ru Channel	1st Anneal	W Cap	2nd Anneal	Result
#1	Yes	60 nm	No	No	No	Ru film delaminated
#2	Yes	15 nm	No	70 nm	No	W film delaminated
#3	Yes	15 nm	Yes	70 nm	No	W film delaminated
#4	Yes	15 nm	Yes	70 nm	Yes	OK

2.4 Summary

Relay employing W as the contacting material are plagued by unstable R_{ON} over switching cycles. To achieve a highly reliable relay technology, alternative contacting materials were surveyed based on desirable material properties, namely excellent hardness, high melting temperature, and low resistivity. Additionally, it is highly desirable that the relay contacting material forms either no native oxide or a conductive native oxide when exposed to air, and is fully compatible with CMOS BEOL metals. Based on the requirements set forth for the contacting material, several platinum group metals and hard ceramic material (i.e. TiN) were further examined. Short-flow experiments were designed to identify issues for the new material to integrate into existing relay process flow. Based on the test results, Ru is identified as an attractive candidate for replacing W as the contacting material for relay technology.

To achieve a fully integrated process flow for Ru-contact relay technology, several process integration challenges must be addressed. Deposition and etching recipes were developed and characterized for Ru thin film. Residual stress control and adhesion to underlying layers are important for sputter-deposited Ru thin films, thus adhesion-promotion layers and thermal annealing were investigated to successfully relieve residual stress for Ru thin film with limited thickness. A post-etch clean recipe based on diluted HCl and H_2O_2 was developed to reduce surface leakage current. Ru was found to be incompatible with photoresist, and hard mask processes were developed for electrode and channel Ru layers.

2.5 References

[1] R. Nathanael, V. Pott, H. Kam, J. Jeon and T.-J. King Liu, "4-Terminal Relay Technology for Complementary Logic," in *IEDM Tech. Dig.*, Washington, DC, USA, 2009.

[2] H. Kam, V. Pott, R. Nathanael, J. Jeon, E. Alon and T.-J. King Liu, "Design and Reliability of a Micro-Relay Technology for Zero-Standby-Power Digital Logic Applications," in *IEDM Tech. Dig.*, Washington, DC, USA, 2009.

[3] F. Chen, M. Spencer, R. Nathanael, C. Wang, H. Fariborzi, A. Gupta, H. Kam, J. Jeon, T.-J. King Liu, D. Markovic, V. Stojanovic and E. Alon, "Demonstration of Integrated Micro-Electro-Mechanical (MEM) Switch Circuits for VLSI Applications," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, San Francisco, CA, USA, 2010.

[4] M. Spencer, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. King Liu, D. Markovic, E. Alon and V. Stojanovic, "Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications," *IEEE J. Solid-State Circuits,* vol. 46, no. 1, pp. 308-320, 2011.

[5] J. Yaung, L. Hutin, J. Jeon and T.-J. King Liu, "Adhesive Force Characterization for MEM Logic Relays With Sub-Micron Contacting Regions," *IEEE/ASME J. MEMS,* vol. 23, no. 1, pp. 198-203, 2014.

[6] H. Kam, E. Alon and T.-J. King Liu, "A Predictive Contact Reliability Model for MEM Logic Switches," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2010.

[7] H. Kam, T.-J. King Liu, V. Stojanovic, D. Markovic and E. Alon, "Design, Optimization, and Scaling of MEM Relays for Ultra-Low-Power Digital Logic," *IEEE Trans. Elec. Dev.,* vol. 58, no. 1, pp. 236-250, 2011.

[8] Y. Chen, R. Nathanael, J. Yaung, L. Hutin and T.-J. King Liu, "Reliability of MEM Relays for Zero Leakage Logic," in *Proc. SPIE 8614*, San Francisco, CA, USA, 2013.

[9] C. Goldsmith, J. Randall, S. Eshelman, T. H. Lin, D. Denniston, S. Chen and B. Norvell, "Characteristics of Micromachined Switches at Microwave Frequencies," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, San Francisco, CA, USA, 1996.

[10] F. Chen, H. Kam, D. Markovic, T.-J. King Liu, V. Stojanovic and E. Alon, "Integrated Circuit Design with NEM Relays," in *Proc. IEEE/ACM Int. Conf. Computer Aided Design*, San Jose, CA, USA, 2008.

[11] W. R. Ashurst, Y. J. Jang, L. Magagnin, C. Carraro, M. M. Sung and R. Maboudian, "Nanometer-thin Titania Films with SAM-level Stiction and Superior Wear Resistance for Reliable MEMS Performance," in *Proc. IEEE 17th Int. Conf. MEMS*, Maastricht, The Netherlands, 2004.

[12] V. Pott, H. Kam, J. Jeon and T.-J. King Liu, "Improvement in Mechanical Contact Reliability with ALD TiO2 Coating," in *Proc. AVS Conf.*, San Jose, CA, USA, 2009.

[13] L. Chen, H. Lee, Z. J. Guo, N. E. McGruer, K. W. Gilbert, S. Mall, K. D. Leedy and G. G. Adams, "Contact Resistance Study of Noble Metals and Alloy Films using a Scanning Probe Microscope Test Station," *J. Appl. Phys.,* vol. 102, no. 7, p. 074910, 2007.

[14] Y.-C. Yeo, "Metal Gate Technology for Nanoscale Transistors—Material Selection and Process Integration Issues," *Thin Solid Films,* Vols. 462-463, pp. 34-41, 2004.

[15] M. A. El Khakani, M. Chaker and B. Le Drogoff, "Iridium Thin Films Deposited by Radio-Frequency Magnetron Sputtering," *J. Vac. Sci. Technol. A,* vol. 16, no. 2, pp. 885-888, 1998.

[16] J.-P. Lu, P. W. Chu, R. Raj and H. Gysling, "Ultrahigh Vacuum Chemical Vapor Deposition of Rhodium Thin Films on Clean and TiO2-covered Si(111)," *Thin Solid Films,* vol. 208, pp. 172-176, 1992.

[17] C. S. Petersson, J. E. Baglin, J. J. Dempsey, F. M. d'Heurle and S. J. La Placa, "Silicides of Ruthenium and Osmium: Thin Film Reactions, Diffusion, Nucleation, and Stability," *J. Appl. Phys.,* vol. 53, no. 7, pp. 4866-4883, 1982.

[18] W. W. Webb, J. T. Norton and C. Wagner, "Oxidation of Tungsten," *J. Electrochem. Soc.,* vol. 103, no. 2, pp. 107-111, 1956.

[19] A. Warren, A. Nylund and I. Olefjord, "Oxidation of Tungsten and Tungsten Carbide in Dry and Humid Atmospheres," *Int. J. Refractory Metals & Hard Mater.,* vol. 14, pp. 345-353, 1996.

[20] K. Aguir, C. Lemire and D. B. Lollman, "Electrical Properties of Reactively Sputtered WO3 Thin Films as Ozone Gas Sensor," *Sens. and Actuators B,* vol. 84, no. 1, pp. 1-5, 2002.

[21] P. Ekkels, X. Rottenberg, R. Puers and H. A. C. Tilmans, "Evaluation of Platinum as a Structural Thin Film Material for RF-MEMS Devices," *J. Micromech. Microeng.,* vol. 19, p. 065010, 2009.

[22] S. Chong, B. Lee, S. Mitra, R. T. Howe and H.-S. P. Wong, "Integration of Nanoelectromechanical Relays With Silicon nMOS," *IEEE Trans. Elec. Dev.,* vol. 59, no. 1, pp. 255-258, 2012.

[23] H. Kwon, D.-J. Choi, J.-H. Park, H.-C. Lee, Y.-H. Park, Y.-D. Kim, H.-J. Nam, Y.-C. Joo and J.-U. Bu, "Contact Materials and Reliability for High Power RF-MEMS Switches," in *Proc. IEEE 20th Int. Conf. MEMS*, Hyogo, Japan, 2007.

[24] J. C. Chaston, "Reaction of Oxygen with the Platinum Metals," *Platinum Metals Rev.,* vol. 8, no. 2, pp. 50-54, 1964.

[25] Y. Abe, M. Kawamura and K. Sasaki, "Preparation of PtO and α-PtO2 Thin Films by Reactive Sputtering and Their Electrical Properties," *Jpn. J. Appl. Phys.,* vol. 38, no. 1, pp. 2092-2096, 1999.

[26] D. J. Dickrell and M. T. Dugger, "Electrical Contact Resistance Degradation of a Hot-Switched Simulated Metal MEMS Contact," *IEEE Trans. Components Packaging Technol.,* vol. 30, no. 1, pp. 75-80, 2007.

[27] M. P. de Boer, D. A. Czaplewski, M. S. Baker, S. L. Wolfley and J. A. Ohlhausen, "Design, Fabrication, Performance and Reliability of Pt- and RuO2-coated Microrelays Tested in Ultra-High Purity Gas Environments," *J. Micromech. Microeng.,* vol. 22, p. 105027, 2012.

[28] H. Zhong, S.-H. Hong, Y.-S. Suh, H. Lazar, G. Heuss and V. Misra, "Properties of Ru-Ta Alloys as Gate Electrodes for NMOS and PMOS Silicon Devices," in *IEDM Tech. Dig.*, Washington, DC, USA, 2001.

[29] M. Tapajna, E. Dobrocka, A. Paskaleva, K. Husekova, E. Atanassova and K. Frohlich, "Electrical Characterization of Ru-and RuO2/Ta2O5 Gate Stacks for Nanoscale DRAM Technology," in *Int. Conf. Adv. Semicond. Dev. Microsys.*, Smolenice, Slovakia, 2008.

[30] T. Yokokawa, T. Yano, C. Kawakita, K. Hinohara and T. Kobayashi, "Thickness of Ruthenium Oxide Film Produced by the Surface Deactivation Treatment of Ruthenium-plated Contact Reed Switches," in *Proc. IEEE 35th Holm Conf. Electrical Contacts*, Chicago, IL, USA, 1989.

[31] T. Umemoto, T. Takeuchi and R. Tanaka, "The Behavior of Surface Oxide Film on Ruthenium and Rhodium Plated Contacts," *IEEE Trans. Components, Hybrids, and Manufacturing Technol.,* vol. 1, no. 1, pp. 103-107, 1978.

[32] F. Ke, J. Miao and J. Oberhammer, "A Ruthenium-Based Multimetal-Contact RF MEMS," *IEEE/ASME J. MEMS,* vol. 17, no. 6, pp. 1447-1459, 2008.

[33] D. A. Czaplewski, G. A. Patrizi, G. M. Kraus, J. R. Wendt, C. D. Nordquist, S. L. Wolfley, M. S. Baker and M. P. de Boer, "A Nanomechanical Switch for Integration with CMOS Logic," *J. Micromech. Microeng.,* vol. 19, p. 085003, 2009.

[34] L. Krusin-Elbaum, M. Wittmer and D. S. Yee, "Characterization of Reactively Sputtered Ruthenium Dioxide for Very Large Scale Integrated Metallization," *Appl. Phys. Lett.,* vol. 50, no. 26, pp. 1879-1881, 1987.

[35] T. Brat, N. Parikh, N. S. Tsai, A. K. Sinha, J. Poole and C. Wickersham Jr., "Characterization of Titanium Nitride Films Sputter Deposited from a High Purity Titanium Nitride Target," *J. Vac. Sci. Technol. B,* vol. 5, no. 6, pp. 1741-1747, 1987.

[36] G. Lemperibre and J. M. Poitevin, "Influence of the Nitrogen Partial Pressure on the Properties of D.C.-Sputtered Titanium and Titanium Nitride Films," *Thin Solid Films,* vol. 111, pp. 339-349, 1984.

[37] C. Ernsberger, J. Nickerson, A. Miller and D. Banks, "Contact Resistance Behavior of Titanium Nitride," *J. Vac. Sci. Technol. A,* vol. 3, no. 6, pp. 2303-2307, 1985.

[38] D. Seneviratne, G. N. Nielson, S. Takahashi, G. Barbastathis and H. L. Tuller, "On the Use of Titanium Nitride as Structural Material for Nano-Electro-Mechanical Systems (NEMS)," in *Proc. IEEE Conf. Nanotechnol.*, Nagoya, Japan, 2005.

[39] D. Lee, W. S. Lee, J. Provine, J.-O. Lee, J.-B. Yoon, R. T. Howe, S. Mitra and H.-S. P. Wong, "Titanium Nitride Sidewall Stringer Process for Lateral Nanoelectromechanical Relays," in *Proc. IEEE 23rd Int. Conf. MEMS*, Wanchai, Hong Kong, 2010.

[40] W. W. Jang, J. O. Lee, J.-B. Yoon, M. S. Kim, J.-M. Lee, S.-M. Kim, K.-H. Cho, D.-W. Kim, D. Park and W.-S. Lee, "Fabrication and Characterization of a Nanoelectromechanical Switch with 15-nm-thick Suspension Air Gap," *Appl. Phys. Lett.,* vol. 92, no. 10, p. 103110, 2008.

[41] H. K. Chiu, T. L. Lin, Y. Hu, K. C. Loeu, H. C. Lin, M. S. Tsai and T. Y. Huang, "Characterization of Titanium Nitride Etch Rate and Selectivity to Silicon Dioxide in a Cl2 Helicon-wave Plasma," *J. Vac. Sci. Technol. A,* vol. 19, no. 2, pp. 455-459, 2001.

[42] J. Schimkat, "Contact Materials for Microrelays," in *11th Int. Workshop MEMS*, Heidelberg, Germany, 1998.

[43] L. Marot, G. de Temmerman, P. Oelhafen, G. Covarel and A. Litnovsky, "Rhodium Coated Mirrors Deposited by Magnetron Sputtering for Fusion Applications," *Rev. Sci. Instrum.,* vol. 78, no. 10, p. 103507, 2007.

[44] J. C. Chaston, "The Oxidation of the Platinum Metals," *Platinum Metals Rev.,* vol. 19, no. 4, pp. 135-140, 1975.

[45] P. Walker and W. H. Tarn, CRC Handbook of Metal Etchants, Boca Raton, FL: CRC Press, 1990.

[46] R. H. Horng, D. S. Wuu, L. H. Wu and M. K. Lee, "Formation Process and Material Properties of Reactive Sputtered IrO2 Thin Films," *Thin Solid Films,* vol. 373, no. 1-2, p. 231–234, 2000.

[47] Y. Hayakawa, S. Kohiki, M. Arai, H. Yoshikawa, S. Fukushima, K. Wagatsuma, M. Oku and F. Shoji, "Electronic Structure and Electrical Properties of Amorphous OsO2," *Phys. Rev. B,* vol. 59, p. 11125, 1999.

[48] B. D. Craig and D. S. Anderson, Handbook of Corrosion Data, Materials Park, OH: ASM International, 1995.

[49] F. K. Chowdhury, H. Pourzand and M. Tabib-Azar, "Investigation of Contact Resistance Evolution of Ir, Pt, W, Ni, Cr, Ti, Cu and Al Over Repeated Hot-Contact Switching for NEMS Switches," in *Proc. IEEE 26th Int. Conf. MEMS*, Taipei, Taiwan, 2013.

[50] T. Aaltonen, M. Ritala, V. Sammelselg and M. Leskela, "Atomic Layer Deposition of Iridium Thin Films," *J. Electrochem. Soc.,* vol. 151, no. 8, pp. G489-G492, 2004.

[51] J. Hämäläinen, T. Sajavaara, E. Puukilainen, M. Ritala and M. Leskelä, "Atomic Layer Deposition of Osmium," *Chem. Mater.,* vol. 24, no. 1, pp. 55-60, 2012.

[52] A. Carton, C. G. Christodoulou, C. Dyck and C. Nordquist, "Investigating the Impact of Carbon Contamination on RF MEMS Reliability," in *IEEE Antennas Propagation Soc. Inter. Symp.*, Albuquerque, NM, 2006.

[53] W. Pan and S. B. Desu, "Reactive Ion Etching of RuO2 Films: The Role of Additive Gases in O2 Discharge," *Phys. Stat. Sol. (a),* vol. 161, pp. 201-216, 1997.

[54] C. C. Hsu, J. W. Coburn and D. B. Graves, "Etching of Ruthenium Coatings in O2- and Cl2-containing Plasmas," *J. Vac. Sci. Technol. A,* vol. 24, no. 1, pp. 1-8, 2006.

[55] E.-J. Lee, J.-W. Kim and W.-J. Lee, "Reactive Ion Etching Mechanism of RuO2 Thin Films in Oxygen Plasma with the Addition of CF4, Cl2, and N2," *Jpn. J. Appl. Phys.,* vol. 37, no. 5A, pp. 2634-2641, 1998.

[56] H. W. Kim, "Characteristics of Ru Etching using ICP and Helicon O2/Cl2 Plasmas," *Thin Solid Films,* vol. 475, pp. 32-35, 2005.

[57] T. Yunogami and K. Nojiri, "Anisotropic Etching of RuO2 and Ru with High Aspect Ratio for Gigabit Dynamic Random Access Memoy," *J. Vac. Sci. Technol. B,* vol. 18, no. 4, pp. 1911-1914, 2000.

[58] I.-R. Chen, Y. Chen, L. Hutin, V. Pott, R. Nathanael and T.-J. King Liu, "Stable Ruthenium-Contact Relay Technology for Low-Power Logic," in *17th Int. Conf. Solid-State Sens., Actuators Microsys. (TRANSDUCERS)*, Barcelona, Spain, 2013.

Chapter 3

Stable Ruthenium-Contact Relay Technology

3.1 Introduction

Nano-electro-mechanical (NEM) relays have been identified as a possible candidate to replace MOSFET switches as the building block for future low-power digital integrated circuit (IC) applications because of their desirable characteristics, namely zero leakage and abrupt turn-ON/turn-OFF behavior [1]. Earlier demonstration of zero-leakage NEM relays employed tungsten (W) as the contacting electrode material for robustness against physical wear and micro-welding [2]. To be practical for IC applications, relays must operate with ON-state resistance (R_{ON}) lower than ~10 kΩ. An issue for W as the contacting electrode, however, is surface oxide formation leading to a gradually increased R_{ON} over time, which eventually leads to circuit failure.

To improve the lifetime of relay-based circuits, a contacting electrode material that forms a conductive native oxide is desirable [3, 4]. In chapter 2, ruthenium (Ru) has been identified as a suitable candidate to replace tungsten (W) as the contacting material [3]. Ru is an attractive candidate because both Ru and its native oxide ruthenium oxide (RuO_2) are hard, stable and electrically conductive so that its R_{ON} does not increase significantly with exposure to air [5, 6]. Key process integration challenges were identified and solutions were developed for integrating Ru into the existing relay process flow. In this chapter, an integrated Ru-contact relay process flow is presented. Ru-contact relays fabricated using this flow were characterized and benchmarked against W-contact relays.

3.2 Ruthenium-Contact Relay Fabrication Process

3.2.1 Tungsten- *vs.* Ruthenium-Contact Relay Comparison

To provide a valid comparison between W-contact and Ru-contact relay performance, both types of devices were fabricated together using identical fabrication processes in the UC Berkeley Marvell Nanofabrication Laboratory except for the fabrication steps pertaining to the contacting layers (i.e. electrode and channel). Figure 3.1 shows the schematic cross-section along the relay contacting regions, illustrating the various material layers and device operation. In the ON-state, the channel contacts the source/drain electrodes to provide a low-resistance conduction path between them. Therefore, the contacting materials are the top material of the electrode layer and the bottom material of the channel layer. These materials should be identical to avoid extra contact resistance and electrostatic attractive force due to work-function mismatch. Materials and nominal thicknesses for each layer were summarized in Table 3.1. The materials and layer thicknesses of W-contact relays were similar to that described in [1], while Ru thicknesses were designed based on the experimental results presented in chapter 2.

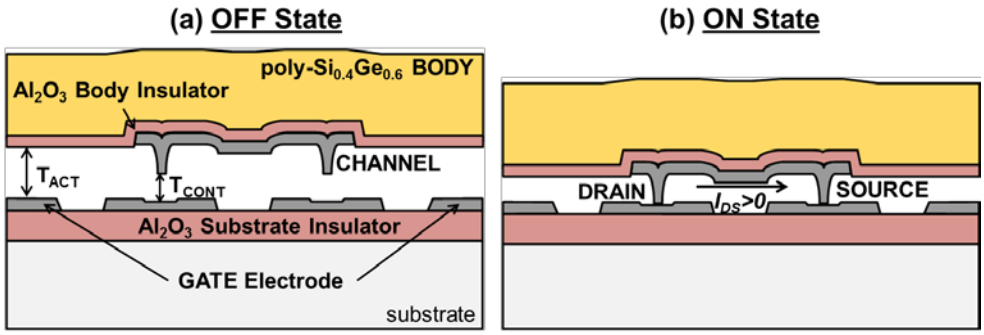


Figure 3.1. Schematic cross-sections along the relay contacting regions illustrating the various layers of the 6-T relay (a) in the OFF-state and (b) in the ON-state.

TABLE 3.1

MATERIALS AND LAYER THICKNESSES COMPARISON

Layer	W-Contact	Ru-Contact
Fixed Electrode	70 nm W	60 nm Ru
Actuation Gap (T_{ACT})	150 nm SiO_2	
Contact Gap (T_{CONT})	75 nm SiO_2	
Channel	70 nm W	15 nm Ru / 70 nm W
Body Insulator	50 nm Al_2O_3	
Body Structure	1.1 µm poly-$Si_{0.4}Ge_{0.6}$	

3.2.2 Integrated Process Flow

An integrated process flow for fabricating both W-contact and Ru-contact relays is illustrated in Figure 3.2. First, 80 nm of aluminum oxide (Al_2O_3) is deposited via atomic layer deposition (ALD) to provide electrical isolation from the underlying silicon substrate. Next, the electrode layer (W or Ru) is deposited by DC magnetron sputtering and patterned using Rohm Haas UV 210-0.6 positive photoresist as masking layer and the Applied Materials Centura decoupled plasma source (DPS) etcher. Because Ru dry etch process erodes photoresist quickly, a hard mask must be used to pattern the Ru electrodes. Low temperature oxide (LTO) deposited by low-pressure chemical vapor deposition (LPCVD) at 400°C was used as the hard mask and the pattern was transferred from photoresist to LTO hard mask using the Centura magnetically enhanced reactive ion etcher. Since Ru cannot withstand the oxygen plasma during photoresist ashing process, photoresist is removed using PRS-3000 stripper solution prior to Ru dry etch in the Centura DPS etcher. For Ru electrodes, post-etch cleaning using diluted hydrochloric acid (HCl) and hydrogen peroxide (H_2O_2) solution at 37%-HCl:30%-H_2O_2:H_2O = 1:1:20 was performed prior to hard-mask removal using vaporized HF.

The air-gap thickness in the contacting regions (T_{CONT}) is made smaller than the actuation air-gap thickness (T_{ACT}) by using the bi-layer sacrificial silicon-dioxide (SiO_2) process described in [1]. Specifically, T_{CONT} is formed with 75 nm LTO and T_{ACT} is formed with an additional 75 nm LTO (i.e. 150 nm LTO in total). This dimpled contact design is beneficial to precisely define the area of the contacting region for each source/drain terminal (0.6 μm × 0.6 μm in this design), and it serves to reduce the hysteresis voltage and pull-in delay.

Integrating Ru as the metallic channel material proved to be a significant challenge and was discussed in detail in chapter 2. In the final integrated flow, a bi-layer channel comprising a thin (~15 nm) Ru bottom layer and a thicker (70 nm) W top layer—each vacuum annealed for 30 minutes at 400ºC—was employed as the channel material. W serves as both the dry-etch hard mask for Ru and the bulk material for current conduction.

After channel formation, Al_2O_3 is deposited by ALD to electrically insulate the channel from the body structure, preventing current flow between the body and source/drain terminals. Anchor/via regions are then defined by etching holes through the Al_2O_3 body insulator and sacrificial LTO layers, to anchor the structural layer(s) and to provide for electrical connection between the electrode and structural layers. Polycrystalline silicon-germanium (poly-$Si_{0.4}Ge_{0.6}$) is then deposited by LPCVD at 410ºC to ensure compatibility with CMOS back-end process. The poly-SiGe layer is heavily doped *in situ* by incorporating boron dopants, to serve as both the movable structure and the body terminal. A relatively thick poly-SiGe layer is employed to suppress the strain gradient to an acceptable value, preventing excessive out-of-plane deflection of the movable structure. Finally, the sacrificial LTO layers are selectively removed using anhydrous HF vapor to release the body structure.

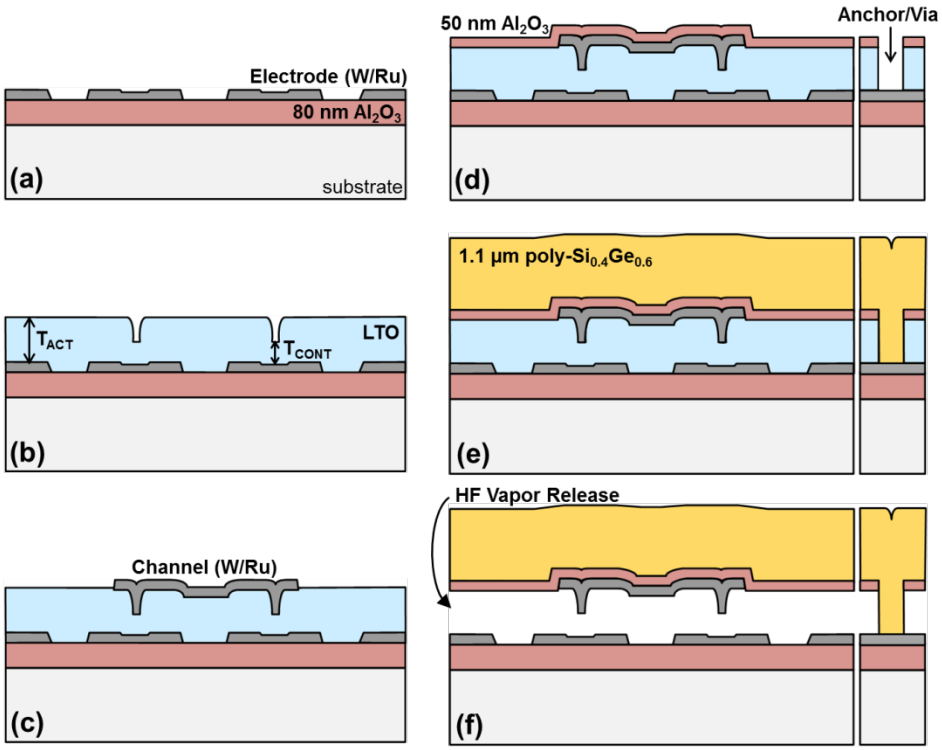


Figure 3.2. Integrated relay fabrication process, with (d)-(f) showing the anchor/via region. (a) Formation of isolation layer and gate/source/drain electrodes. (b) Bi-layer sacrificial SiO_2 process with formation of contact dimples. (c) Formation of channel layer. (d) Deposition of body insulator layer followed by etching of anchor/via holes. (e) Formation of body structure. (f) Structural layer release.

3.3 Ruthenium-Contact Relay Characterization Results

3.3.1 Microscopy Results

Figure 3.3 shows a schematic layout and a plan-view scanning electron microscopy (SEM) image of a 6-terminal (6-T) Ru-contact relay design in this work. Two sets of source/drain electrodes are present on a single relay structure, allowing a more compact circuit design. The body structure (denoted by orange-colored regions) consists of a vertically movable plate suspended at each corner by folded-flexure beams anchored to the substrate. This beam design mitigates undesirable effects of residual stress upon release of the structure. The body structure is separated from gate, source and drain electrodes (denoted by silver-colored regions) by an air gap. The lateral dimensions of the main portion of the body plate are 15µm × 15µm; the extensions on each side serve to increase the actuation area to reduce the switching voltages.

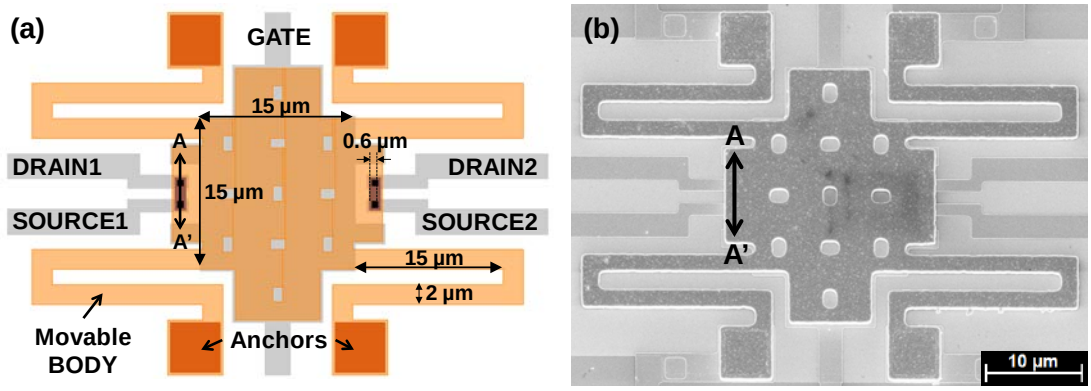


Figure 3.3. Plan-view of a 6-T Ru-contact relay in this work. A-A' indicate the location across one set of channel and dimples (ref. Figure 3.1). (a) Schematic layout with key terminals and dimensions labeled. (b) SEM micrograph of a relay after HF vapor release.

Figure 3.4 shows the SEM micrograph of a released Ru-contact relay in tilted cross-sectional view along a channel, across the contact dimples (A-A' in Figure 3.3). Focused ion beam (FIB) milling is used to provide an accurate cut across the channel/dimple region. The contact air gap between the channel and source/drain electrodes can be clearly seen in the cross-sectional view. The air gap at the contact dimples is smaller than other regions as designed in the bi-layer sacrificial LTO process.

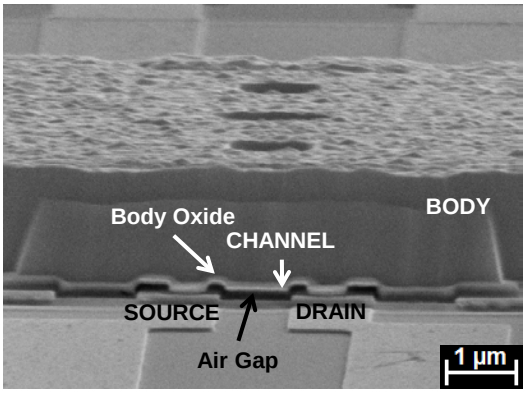


Figure 3.4. Cross-sectional view of a released Ru-contact relay under SEM.

Figure 3.5 shows the white-light interferometry topograph of a released Ru-contact 6-T relay. The result showed a flat structural plate at the center and minimum out-of-plane deflection at the four folded flexures. The strain gradient of the structural stack (body Al_2O_3 insulator and poly-$Si_{0.4}Ge_{0.6}$ structure) can be calculated from the measured out-of-plane bending of the folded flexures and is measured to be -4.1×10^{-4}/µm in this sample. Low strain gradient (usually less than 1×10^{-3}/µm) is beneficial for maintaining the contact air gap to its designed thickness and therefore lower operating voltages.

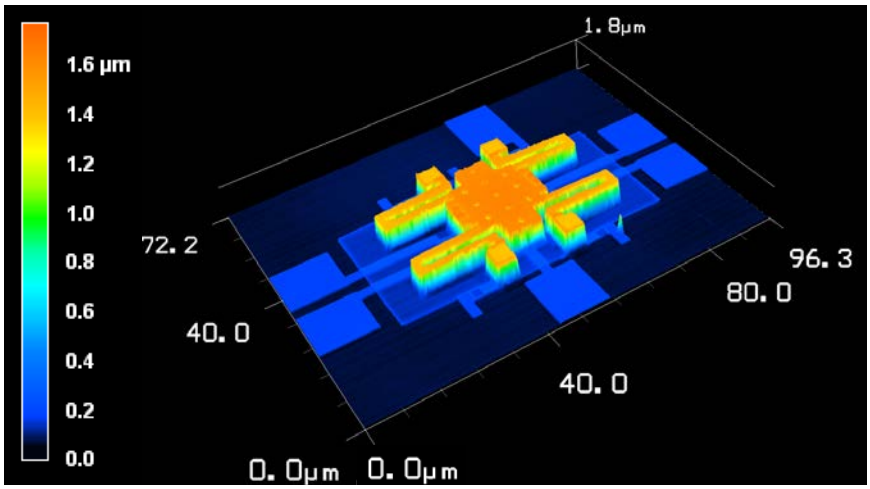


Figure 3.5. Interferometry measurement result of a released Ru-contact 6-T relay using Keyence white-light confocal microscope.

3.3.2 Single-Relay Electrical Characterization Results

Figure 3.6 shows typical measured current-*vs.*-voltage (I_{DS}-V_G) curves for a Ru-contact relay, exhibiting immeasurably low OFF-state leakage and abrupt turn-ON/turn-OFF behavior. I_{DS1} and I_{DS2} denote measured current for each of the source/drain electrode set during the same V_G sweep, showing both source/drain sets switch together. Gate current remains below noise level throughout the sweep, indicating the effectiveness of the insulating body oxide. The nominal switching voltages for this relay are V_{PI} = 8.9 V (pull-in voltage) and V_{RL} = 7.9 V (release voltage).

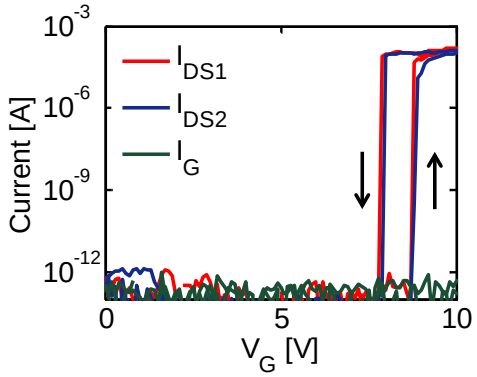


Figure 3.6. Measured I-V characteristics of a Ru-contact relay, showing zero OFF-state leakage and abrupt switching behavior for both sets of source/drain electrodes. V_{DS} = 2 V and V_B = 0 V.

Figure 3.7 shows how the relay switching voltages can be reduced by applying a body bias (V_B) [1]. Since parasitic source/drain actuation is minimized in the 6-T relay design by minimizing channel and gate electrode overlap, the shifts in V_{PI} and V_{RL} each are equal in magnitude to V_B [7]. The hysteresis voltage $V_{PI} - V_{RL}$ remains constant with different V_B. For proper operation, V_{RL} must be greater than zero so that the relay is in the OFF-state when V_G = 0 V. Thus, hysteresis voltage $V_{PI} - V_{RL}$ ultimately sets a lower limit for the operating voltage (V_{DD}) of relay-based integrated circuits.

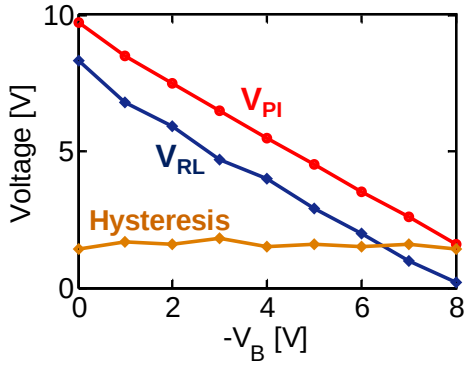


Figure 3.7. Dependence of pull-in (V_{PI}) and release (V_{RL}) voltages on body bias (V_B).

Figure 3.8 shows the I_{DS}-V_G characteristics of the same relay during over consecutive sweeps. The result shows stable operating voltages and ON-state currents. Hysteresis voltage $V_{PI} - V_{RL}$ remains constant (~1 V) over consecutive sweeps, indicating sub-1V operation for relay-based circuits is possible.

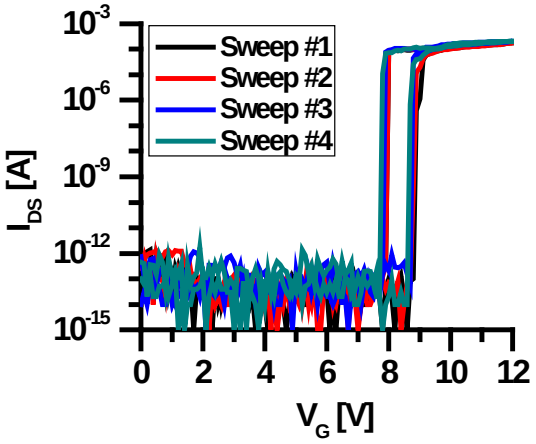


Figure 3.8. I_{DS}-V_G characteristics for the same source-drain set over four consecutive sweeps.

3.3.3 Evolution of ON-state Resistance for Ru-Contact Relays

The key issue of W-contact relays is native oxide formation at the relay contacts leading to increased R_{ON} during hot-switching, where a direct current flows between the source and drain electrodes whenever the relay is ON. The oxide formation process is exacerbated by the Joule heating at contacting surfaces causing elevated local temperature [2]. Note that hot-switching is more stressful than typical operations in a digital logic circuit, where a relay conducts current only for a relatively short period of time whenever it is turned ON, to charge or discharge a load capacitance. Therefore hot-switching can be regarded as the worst-case analysis for relay circuit lifetime. For Ru-contact relays, contact oxidation should yield a hard and conductive RuO_2 oxide. Therefore, the characteristics of Ru-contact relays should remain consistent over time and eliminating a key obstacle for achieving reliable relay-based circuits.

Figure 3.9 shows the test setup for monitoring R_{ON} for a relay [8]. The square-wave input signal v_i is sent to gate electrode to turn the relay ON and OFF. An external load resistor R_L connects the power supply voltage V_{DD} and drain terminal of the relay, thus current i_o flows between drain and source terminals whenever the relay is ON. Since the resistance between relay's drain/source terminals (R_{DS}) and R_L forms a voltage divider, R_{DS} can be determined by monitoring $v_o = V_{DS}$ on the oscilloscope.

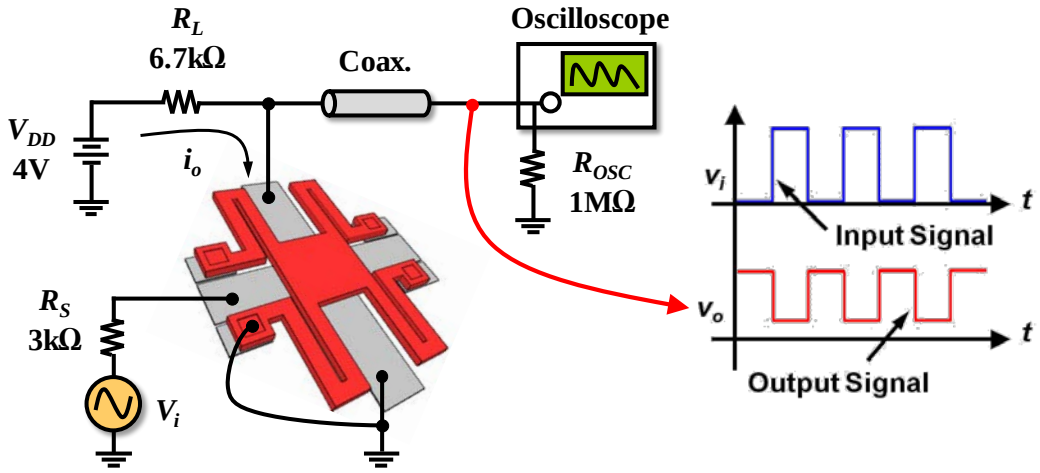


Figure 3.9. Schematic showing the setup for monitoring relay's output resistance and time-domain waveforms illustrating input-output relationship [8].

Figure 3.10 compares the stability of R_{ON} for Ru-contact vs. W-contact relays as they undergo hot-switching cycles in vacuum (5 µTorr). For this measurement, V_G is cycled between 0 V and 12 V at 5 kHz to turn the relay ON and OFF repeatedly. V_{DS} is fixed at 4 V to operate the relays in hot-switching mode. Although R_{ON} increases sooner (within the first 2 million switching cycles) for the Ru-contact relay, it stabilizes at an acceptable level of ~9 kΩ. In contrast, R_{ON} for the W-contact relay increases rapidly to above 10 kΩ after ~25 million switching cycles. These results suggest that RuO_2 formation is self-limited and does not severely inhibit current conduction (unlike WO_x formation for W-contact relays).

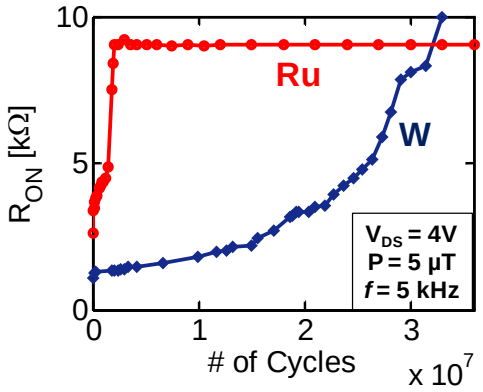


Figure 3.10. R_{ON} evolution with the number of hot-switching cycles.

Figure 3.11 shows how V_{PI}, V_{RL} and R_{ON} evolve when a relay is exposed to room ambient conditions without switching in-between measurements. R_{ON} for the W-contact relay gradually increases over time due to native oxide formation, while R_{ON} for the Ru-contact relay is almost constant. V_{PI} for both types of relays is fairly stable over the entire measurement regardless of native oxide formation, but V_{RL} for both W-contact and Ru-contact relays gradually increase with exposure to air. This phenomenon can be explained by the reduced surface adhesive force from metallic surfaces to oxide surfaces. Therefore the hysteresis voltage $V_{PI} - V_{RL}$ reduces over time for both types of relays. Figure 3.12 shows the I_{DS}-V_G relationship for a Ru-contact relay after exposure to ambient air, showing the effect of reduced adhesive force due to surface oxide formation.

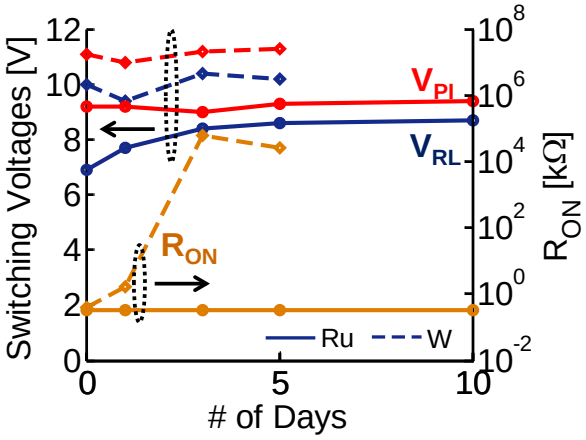


Figure 3.11. V_{PI}, V_{RL} and R_{ON} evolution with exposure to ambient conditions for Ru-contact (solid) and W-contact (dash) relays. Measurements made immediately after release correspond to 0 days of air exposure.

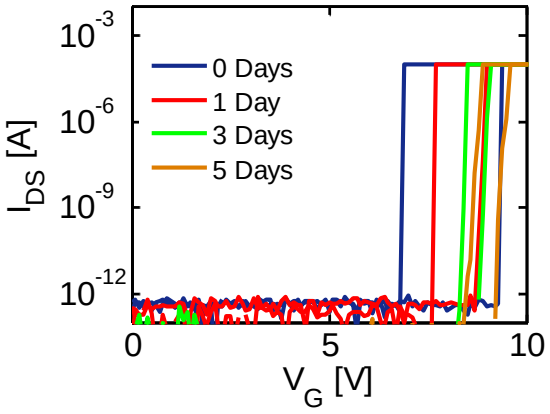


Figure 3.12. I_{DS}-V_G relationship for a Ru-contact relay after exposure to air ambient. The relay under test was not actuated in between measurements. The current compliance limit was set at 0.1 mA.

Figure 3.13 shows that sub-1V operation of a Ru-contact relay is possible with reduced surface adhesive force and body biasing. The hysteresis voltage was reduced from ~1 V to ~0.5 V after 3 days of exposure in ambient. With V_B = 7.1 V, V_{PI} is reduced to 0.7 V and V_{RL} is reduced to 0.2 V. Note that relay turn-ON and turn-OFF transitions shows slight non-abruptness due to the formation of native oxide (i.e. current flows by tunneling in the ON-state).

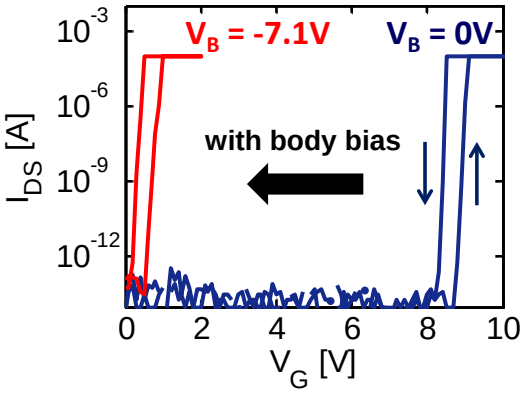


Figure 3.13. Measured I_{DS}-V_G characteristics for Ru-contact relays after 3 days of exposure to air, showing sub-1V operation with body biasing. The current compliance limit was set at 0.1 mA.

3.3.4 Variations of Ruthenium-Contact Relays

Table 3.2 shows statistics for measured relay switching voltages from a single wafer. The nominal V_{PI} and V_{RL} values are defined as the pull-in and release voltages when no body bias is applied (V_B = 0 V). For circuit applications, it is important to understand the yield and variations of fabricated devices on a single chip. It is shown that V_{PI} can be reduced by biasing the body terminal (Figures 3.7 and 3.11). For a single relay, the hysteresis voltage $V_{PI} - V_{RL}$ sets the V_G lower-bound for proper relay operation. For integrated circuit application with a single supply voltage (V_{DD}), V_{DD} must be able to operate all devices on the chip at the same time. This can be achieved by supplying proper body bias to each relay in the circuit, or increasing V_{DD} to accommodate the variation in hysteresis for different relays. The first option is not practical for a large-scale integrated circuit, so ultimately the difference between maximum V_{PI} and minimum V_{RL} across all relays sets the lower limit for V_{DD}. For the wafer measured in Table 3.2, V_{DD} > 3.8 V is required to ensure proper circuit operation.

TABLE 3.2

STATISTICS OF KEY RU-CONTACT RELAY CHARACTERISTICS

	Average	Maximum	Minimum	Standard Deviation
Nominal V_{PI} [V]	8.67	9.9	8.2	0.84
Nominal V_{RL} [V]	7.11	8.4	6.1	0.99
$V_{PI} - V_{RL}$ [V]	1.56	2.7	0.9	0.53
Welding V_{DS} [V]	7.84	10.5	6.4	0.95

Another important consideration for relay-based integrated circuit is the drain-to-source voltage difference upon closing that results in micro-welding (i.e. a stuck-ON failure). As discussed in chapter 1, micro-welding occurs due to material transfer (due to high local temperature) between the contacting surfaces causing the channel layer to fuse with source/drain electrodes. The probability of micro-welding occurring is exponentially related to V_{DS} [2]. Since in most circuits a single supply V_{DD} is used for both gate and drain-source bias, the minimum value of V_{DS} that causes micro-welding sets the upper-bound for V_{DD}. For the wafer measured in Table 3.2, V_{DD} should not exceed 6.4 V. Further design and process improvements should aim to reduce variations in switching voltages so that V_{DD} can be reduced.

3.4 Oxidation of Ruthenium-Contact Relays

Ru-contact relays show desirable characteristics such as stable operating voltages V_{PI} and V_{RL}, as well as stable ON-state resistance over time. However, the turn-ON transition was not fully abrupt for some Ru-contact relays when they were actuated for the first time after HF vapor release. Figure 3.14 describes the non-abruptness of the first turn-ON transition for some Ru-contact relays. Although I_{DS} reached 10-100 nA after pull-in at V_{PI} = 9.4 V, I_{DS} did not hit the compliance limit at 0.1 mA until 10.4 V. The channel layer clearly touched source/drain electrodes after pull-in to have substantial current conduction, but some thin, non-conductive layer was present at the contacts. This is similar to the "oxide break" procedure for W-contact relays, as WO_x native oxide was present at the contacts and required high source-to-drain bias to break down the native oxide layer [4].

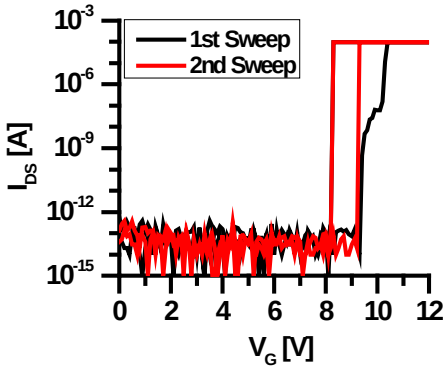


Figure 3.14. I_{DS}-V_G sweeps for a Ru-contact relay immediately after dry release in HF vapor, showing non-abrupt turn-ON for the first sweep. V_{DS} was kept at 2 V for both sweeps and current compliance limit was set at 0.1 mA. Note abrupt and stable turn-OFF behavior was observed for both sweeps.

To achieve large-scale relay-based circuits, this non-ideality during first actuation is undesirable because it requires either additional circuitry (which implies significant area penalty) to perform "oxide break" procedure, or high initial V_{DD} to ensure breaking all native oxide at the contacts (which increases risk of welding). Unlike W-contact relays, the native oxide RuO_2 for Ru-contact relays should not hinder current conduction. Two other possible explanations for this non-conductive layer are examined below.

First, noble metals such as ruthenium and platinum are known to be susceptible to carbon contamination from the environment, forming frictional polymer layers at contacting surfaces [9]. Figure 3.15 shows the contact resistance evolution of noble metal contacts in air, in which Ru degraded the fastest among all tested noble metals. In addition, photoresist may introduce additional carbon contaminants during lithographic steps which significantly enhance frictional polymer buildup. Additional cleaning steps were applied after electrode etch and after dimple etch to fully remove any photoresist residue at the contacting surface.

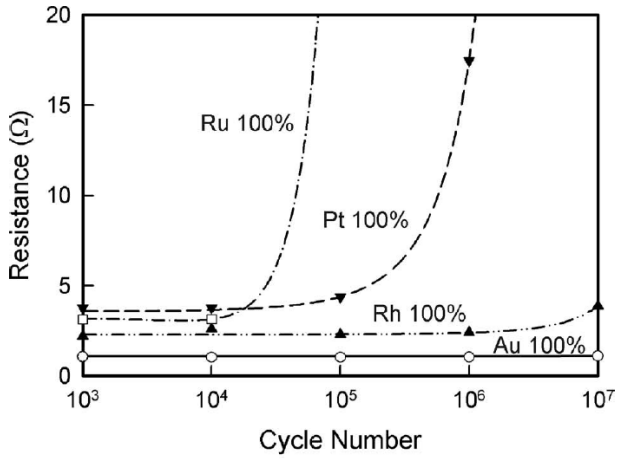


Figure 3.15. Measured contact resistance evolution curves of noble metals in ambient air [9].

Second, the existence of non-stoichiometric RuO_x is possible at the dimple contacting surfaces. Figure 3.16 shows the comparison between Ru contact resistances after exposure to air at different temperatures [10]. In low temperature environment, electron spectroscopy for chemical analysis (ESCA) showed that a mixture of non-conductive RuO and RuO_2 exists at the contacts after 618 hours of air exposure. In a heated environment >300ºC, ESCA confirmed that stoichiometric RuO_2 is the predominant species so the contact resistance remains low after air exposure. This is consistent with the observation that breaking down native oxide is not needed for Ru-contact relays once achieving abrupt switching behavior, while "oxide break" procedure was needed for W-contact relays after each air exposure (Figure 3.11). While ruthenium contacting surface layers can initially contain non-stoichiometric RuO_x (before any switching events), the elevated local temperature due to current conduction in the ON-state helps forming a stoichiometric RuO_2 oxide layer at the contacting surfaces.

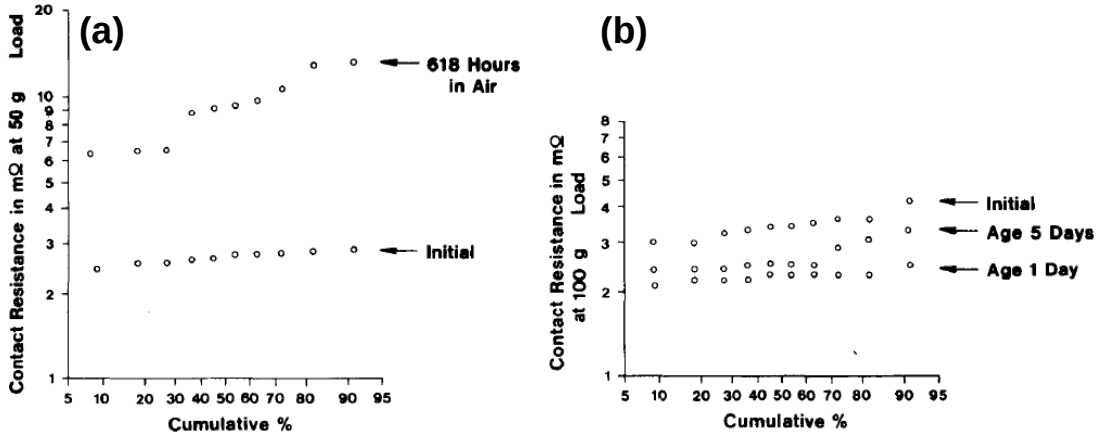


Figure 3.16. Contact resistance of ruthenium after exposure to air (a) at room temperature, and (b) at 300ºC [10].

To overcome initial non-stoichiometric RuO_x formation, post-release O_2 anneal was attempted on Ru-contact relays. It is estimated that 0.5-1 nm of RuO_2 can be formed on the ruthenium surfaces after 1 hour of O_2 annealing at 400ºC in a furnace [11]. Note that the annealing temperature must be below 410ºC to preserve the CMOS-compatibility of the relay fabrication process. Although the RuO_2 layer formed by this method is extremely thin, it has been shown that thin RuO_2 prepared by direct oxidation of ruthenium exhibits similar contact resistance as non-oxidized ruthenium metal [12]. Another advantage of RuO_2 is the improved immunity to hydrocarbon contamination, eliminating the need to isolate relays in an ultra-clean environment [11].

Figure 3.17 shows the I_{DS}-V_G characteristics of a Ru-contact relay after furnace anneal (400ºC, 1 hour). Results showed a nearly abrupt switching behavior even for the first sweep, and stable V_{PI}, V_{RL}, and R_{ON} for subsequent sweeps. Higher V_{PI}, V_{RL}, and hysteresis voltage were also observed in Figure 3.17 due to increased strain gradient (in negative direction) for poly-$Si_{0.4}Ge_{0.6}$-based structural stack after furnace annealing. Confocal microscope measurements confirmed that the increased negative strain gradient caused the end of folded flexures to touch the Al_2O_3 substrate, increasing T_{ACT} and therefore increasing operating voltages. Oxidized relays were also found to weld more easily at V_{DS} ~ 5 V, as opposed to ~ 8 V for non-annealed relays. This observation showed that the activation energy of RuO_2 is lower than Ru and is consistent with earlier observations. These tradeoffs must be considered when designing the post-release annealing process for Ru-contact relays.

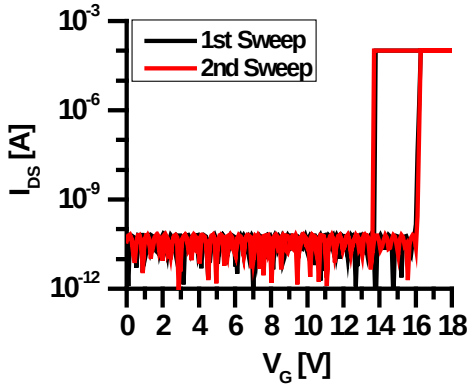


Figure 3.17. I_{DS}-V_G sweeps for a Ru-contact relay after furnace annealing. V_{DS} was kept at 2 V and current compliance limit was set at 0.1 mA. Note the noise floor is higher due to shorter integration time during electrical measurements.

3.5 Summary

A full process flow for fabricating Ru-contact relays was presented and Ru-contact microscale logic relays were demonstrated for the first time. Microscopy and interferometry measurements confirmed that the Ru-contact relays were fabricated with designed dimensions and low strain gradient ($<1\times10^{-3}$/μm). Electrical characterization showed reasonably low V_{PI} (<10 V), low hysteresis voltage (~1 V), and low R_{ON} (<10 kΩ). W-contact relays and Ru-contact relays which underwent identical process steps except for the electrode/channel layers were compared against each other. Ru-contact relays showed significantly improved contact resistance stability through hot-switching cycles, as well as better R_{ON} stability when exposed to air. Relays exposed to ambient also showed a lower surface force at contacts due to oxide formation, leading to reduced hysteresis voltage. The reduced hysteresis enabled sub-1V operation via body biasing; hence the Ru-contact relays show promise for future ultra-low-power digital logic applications. Further process and design improvements should aim to reduce device-to-device variation, so that circuit-level V_{DD} reduction is possible.

Post-release oxidation of Ru contacts can further improve the stability of Ru-contact relays during first few sweeps after HF vapor release. While the stability of Ru-contact relays can be improved via furnace O_2 annealing, the strain gradient of the structural layer stack and micro-welding worsen. These tradeoffs must be carefully controlled when optimizing the Ru-contact relay fabrication process.

3.6 References

[1] R. Nathanael, V. Pott, H. Kam, J. Jeon and T.-J. King Liu, "4-Terminal Relay Technology for Complementary Logic," in *IEDM Tech. Dig.*, Washington, D.C., USA, 2009.

[2] H. Kam, E. Alon and T.-J. King Liu, "A Predictive Contact Reliability Model for MEM Logic Switches," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2010.

[3] I.-R. Chen, Y. Chen, L. Hutin, V. Pott, R. Nathanael and T.-J. King Liu, "Stable Ruthenium-Contact Relay Technology for Low-Power Logic," in *17th Int. Conf. Solid-State Sens., Actuators Microsys. (TRANSDUCERS)*, Barcelona, Spain, 2013.

[4] Y. Chen, R. Nathanael, J. Jeon, J. Yaung, L. Hutin and T.-J. King Liu, "Characterization of Contact Resistance Stability in MEM Relays With Tungsten Electrodes," *IEEE/ASME J. MEMS*, vol. 21, no. 3, pp. 511-513, 2012.

[5] D. A. Czaplewski, G. A. Patrizi, G. M. Kraus, J. R. Wendt, C. D. Nordquist, S. L. Wolfley, M. S. Baker and M. P. de Boer, "A Nanomechanical Switch for Integration with CMOS Logic," *J. Micromech. Microeng.*, vol. 19, p. 085003, 2009.

[6] F. Ke, J. Miao and J. Oberhammer, "A Ruthenium-Based Multimetal-Contact RF MEMS," *IEEE/ASME J. MEMS*, vol. 17, no. 6, pp. 1447-1459, 2008.

[7] J. Jeon, R. Nathanael, V. Pott and T.-J. King Liu, "Four-Terminal Relay Design for Improved Body Effect," *IEEE Elec. Dev. Lett.*, vol. 31, no. 5, pp. 515-517, 2010.

[8] Y. Chen, R. Nathanael, J. Yaung, L. Hutin and T.-J. King Liu, "Reliability of MEM Relays for Zero Leakage Logic," in *Proc. SPIE Conf.*, San Francisco, CA, USA, 2013.

[9] L. Chen, H. Lee, Z. J. Guo, N. E. McGruer, K. W. Gilbert, S. Mall, K. D. Leedy and G. G. Adams, "Contact Resistance Study of Noble Metals and Alloy Films using a Scanning Probe Microscope Test Station," *J. Appl. Phys.*, vol. 102, no. 7, p. 074910, 2007.

[10] S. P. Sharma and L. L. Hines, "Oxidation of Ruthenium," *IEEE Trans. Components, Hybrids, and Manufactutung Technol.*, vol. 6, no. 1, pp. 89-92, 1983.

[11] M. P. de Boer, D. A. Czaplewski, M. S. Baker, S. L. Wolfley and J. A. Ohlhausen, "Design, Fabrication, Performance and Reliability of Pt- and RuO2-coated Microrelays Tested in Ultra-High Purity Gas Environments," *J. Micromech. Microeng.*, vol. 22, p. 105027, 2012.

[12] R. G. Vadimsky, R. P. Frankenthal and D. E. Thompson, "Ru and RuO2 as Electrical Contact Materials: Preparation and Environmental Interactions," *J. Electrochem. Soc.: Solid State Sci. Technol.*, pp. 2017-2023, 1979.

Chapter 4

Scaled Relay Structure for Integrated Circuit Applications

4.1 Introduction

Despite its relatively large footprint compared to a transistor, a relay can be useful in addressing the energy efficiency limit of CMOS integrated circuits by rethinking circuit-level design techniques [1, 2]. Low operating voltages for relays (i.e. pull-in voltage V_{PI} and hysteresis voltage $V_{PI} - V_{RL}$) are critical for energy efficient circuit operation and high relay endurance [3]. However, the first prototype logic relays are plagued by strain gradient present in the structural layer stack. Reducing relay operating voltage is difficult without first addressing the strain gradient issue. Furthermore, scaling of the device footprint is important for implementing VLSI relay circuits. Design and process modifications are needed for achieving scaled relay technology operating at low voltage.

In this chapter, process and device design improvements to relay technology are discussed with the fabrication of relay-based VLSI circuits in mind. The theoretical basis for strain gradient is studied and modifications to the structural film are demonstrated to provide for lower operating voltage with a more compact device layout. Fabrication of relay VLSI circuits is examined from a process integration perspective, and the relay process flow was refined to meet the additional requirements imposed for fabricating a relay-based microcontroller comprising >12,000 relays.

4.2 Low-Voltage Relay Technology via Strain Gradient Control

4.2.1 Relay Operating Voltage

As discussed in chapter 1, it is desirable to minimize relay operating voltage in order to minimize energy consumption, reduce switching delay, and improve relay endurance [3]. The pull-in voltage (V_{PI}) of a relay depends on a number of design parameters, as indicated by equation 4.1 [4]:

$$V_{PI} \propto \sqrt{\frac{EWH^3T_{ACT}^3}{\varepsilon_0 L^3 A_{ACT}}}, \tag{4.1}$$

where E and H are the Young's modulus and thickness of the structural material, respectively, T_{ACT} is the actuation gap thickness, A_{ACT} is the actuation area, ε_0 is the permittivity of air, and W and L are the width and length of the suspension beams, respectively.

To reduce V_{PI}, one can design the relay according to the following guidelines: increase the lateral dimensions (L, A_{ACT}), reduce the vertical dimensions (H, T_{ACT}), or change the structural stack to a softer (i.e. lower E) material. Increasing lateral dimensions generally is not desirable since it increases the device footprint. Finding materials with lower E can often lead to complex process integration issues and degraded mechanical strength. The benefit of reducing E is also limited in terms of scalability. Thus, it is generally more convenient to reduce the vertical dimensions of the relays to achieve low V_{PI}. However, simply reducing structural stack thickness may cause several issues if the structural stack has non-zero strain gradient. The effect of strain gradient within the structural stack is discussed in the following section.

4.2.2 Strain Gradient Induced Structure Bending

In general, it is essential to minimize the strain gradient of a thin-film structure since it will bend out-of-plane upon release if a strain gradient exists within the film. The out-of-plane deflection may degrade device performance or result in non-functional devices. Figure 4.1 illustrates the effect of excessive strain gradient in the structural film of NEMS relays. If the structural film has positive strain gradient, the released structure has a concave upward shape. Structural film with high positive strain gradient may result in non-functional devices, either because the contact dimples become stuck to the source/drain electrodes (illustrated in Figure 4.1a) or the body structure touches the underlying gate electrode at the center and prevents the contact dimples from landing on the source/drain electrodes. If the structural film has negative strain gradient, the released structure has a concave downward shape, and the contact and actuation gaps may significantly increase in size (Figure 4.1b). This may leads to prohibitively high operating voltages due to the large T_{ACT} (equation 4.1). For reliable and energy-efficient NEM relay operations, the strain gradient of the structural film should be minimized.

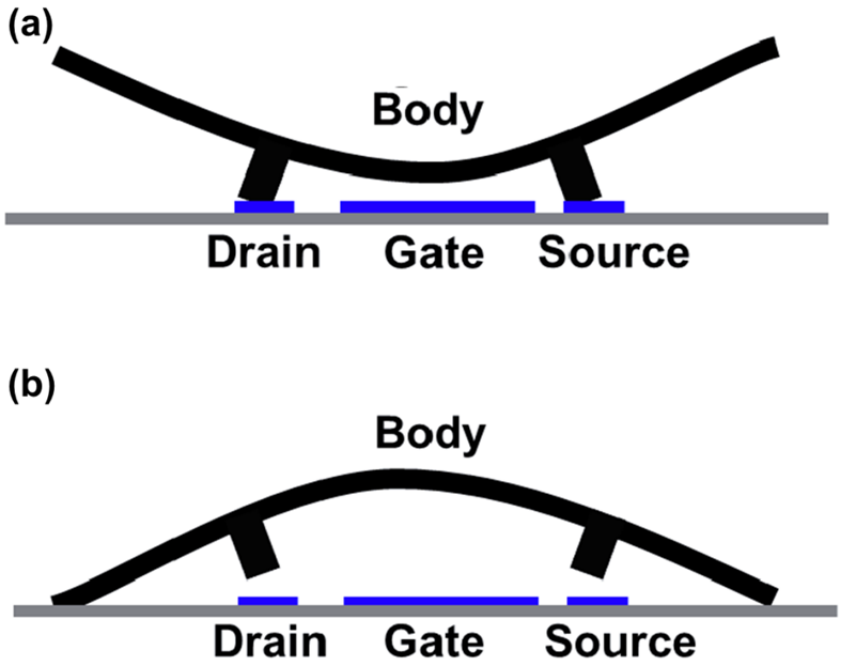


Figure 4.1. Simplified cross-sectional view of a NEM relay structure with large (a) positive and (b) negative strain gradient. The undesirable effects of high strain gradient are illustrated. (Figure modified from [5].)

Figure 4.2 shows the out-of-plane deflection (Δz) of a simple cantilever beam with thickness H and length L in relation to the radius of curvature of the structural film (ρ). For a simple cantilever beam with $L >> \Delta z$ and uniform non-zero strain gradient throughout the film, the bending can be approximated by the following governing equation:

$$\Delta z = \frac{1}{2}\frac{L^2}{\rho} = \frac{1}{2}\Gamma L^2, \tag{4.2}$$

where Γ is the average strain gradient of the structural film [6].

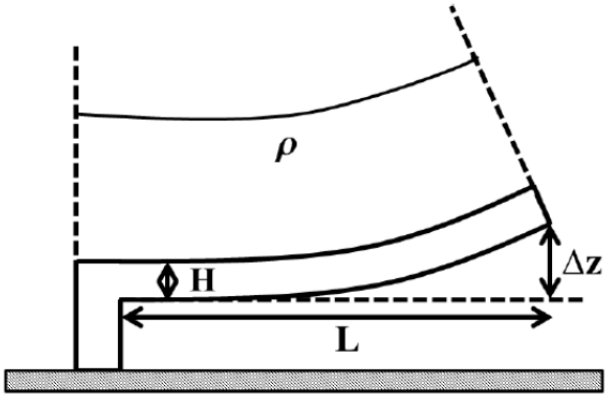


Figure 4.2. Schematic sideview of a cantilever beam structure with out-of-plane deflection [5].

Previous efforts to reduce out-of-plane deflection of relay structures, which comprise a heavily doped polycrystalline silicon-germanium (poly-SiGe) thin film, have focused on optimizing the process of low-pressure chemical vapor deposition (LPCVD) for poly-SiGe. The deposition process optimization efforts are described in great detail in [5] and [7] for various thicknesses of poly-SiGe film. The factors which can affect the strain gradient within a poly-SiGe film include dopant concentration, deposition temperature, deposition pressure, etc. [8, 9]. The prototype logic relay technology used a thick (>1 μm) film of doped poly-$Si_{0.4}Ge_{0.6}$ as the structural material in order to minimize the effect of strain gradient, and yielded relays with switching voltages much greater than 5 V [10]. However, it is difficult to produce a thinner poly-SiGe film with low strain gradient without complicated post-deposition treatments [5]. In the subsequent sections, relays with reduced operating voltages will be demonstrated using strain gradient control techniques other than optimizing the poly-SiGe deposition process.

4.3 Relay Structural Stack Development for Foundry Fabrication

In addition to scaling of vertical relay dimensions to reduce operating voltage, scaling of the device footprint should also be considered when advancing relay technology. To achieve this goal, the logic relay process technology was transferred to industry collaborators, to allow relay devices with scaled footprint to be fabricated in a foundry environment. Due to the difference in fabrication tools and restrictions to avoid contamination, several process modifications were required and integration challenges were addressed.

4.3.1 Process Limitations and Design Modifications

Figure 4.3 shows the schematic cross-sectional view along the channel region for a foundry-fabricated relay. The structure is mostly similar to the relay structure fabricated in the UC Berkeley Marvell Nanofabrication Laboratory (discussed in chapters 1 and 3) with the differences highlighted in this section. Additional interconnect and inter-metal dielectric Al_2O_3 layers were added underneath the device structures to implement integrated circuits. The interconnect technology for relay-based integrated circuits will be discussed in detail in section 4.6. The sacrificial oxide layers were deposited via plasma-enhanced chemical vapor deposition (PECVD) with tetra-ethyl-ortho-silicate (TEOS) and oxygen (O_2) as the gaseous sources.

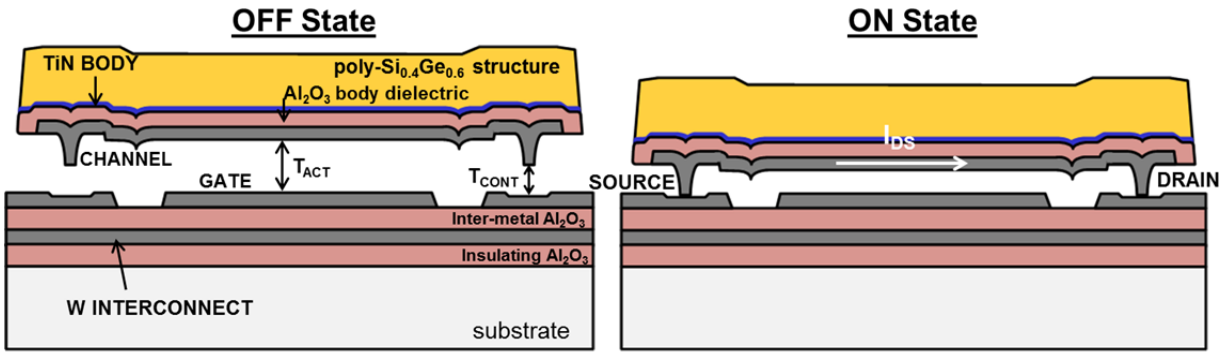


Figure 4.3. Schematic cross-sections of a foundry-fabricated 4-T relay. (a) In the OFF-state, an air gap separates the channel from the source and drain electrodes. (b) In the ON-state, the channel forms a pathway for current to flow between the source and drain electrodes. (Figure modified from [11])

The most challenging process limitations encountered during the technology transfer to the foundry were related to the structural stack development. The rapid thermal chemical vapor deposition (RT-CVD) process used to deposit poly-SiGe was limited to 100 nm in film thickness and did not use *in-situ* doping. To ensure that the body structure is sufficiently conductive for uniform charge distribution at the SiGe-Al_2O_3 interface, a thin (10 nm thick) layer of conductive titanium nitride (TiN) formed by atomic layer deposition (ALD) was inserted between the Al_2O_3 body dielectric layer and the poly-SiGe structural layer. Theoretically, a ~10x thinner poly-SiGe layer should lead to ~30x reduction in V_{PI} (cf. equation 4.1). However, the measured V_{PI} was in excess of 20 V, and the resultant high voltage sustained across the Al_2O_3 body dielectric caused it to break down. The high V_{PI} can be attributed to a significantly increased T_{ACT} due to negative strain gradient. The benefit from scaling H is not observable since T_{ACT} increased to be more than 10x the nominal designed thickness.

Figure 4.4 shows white-light interferometry measurements of cantilever beams fabricated with the 40 nm Al_2O_3 / 10 nm TiN / 100 nm poly-SiGe structural stack. The results suggested that for long cantilevers, the base portion (i.e. close to anchors) of the beam was stuck on the substrate due to a compliant beam (with low effective spring constant, k_{eff}) and the tip part of the beam was arched up due to negative strain gradient. Dramatic out-of-plane deflection was observed, with the highest portion of the beam ~1.8 µm higher than the base. The average strain gradient Γ of the cantilever beam can be deduced using equation 4.2. For cantilevers with the shape shown in Figure 4.4, the length L used for strain gradient calculation should exclude the portion of the beam which is stuck down, and should be equal to half of the arch width, as indicated on Figure 4.4b.

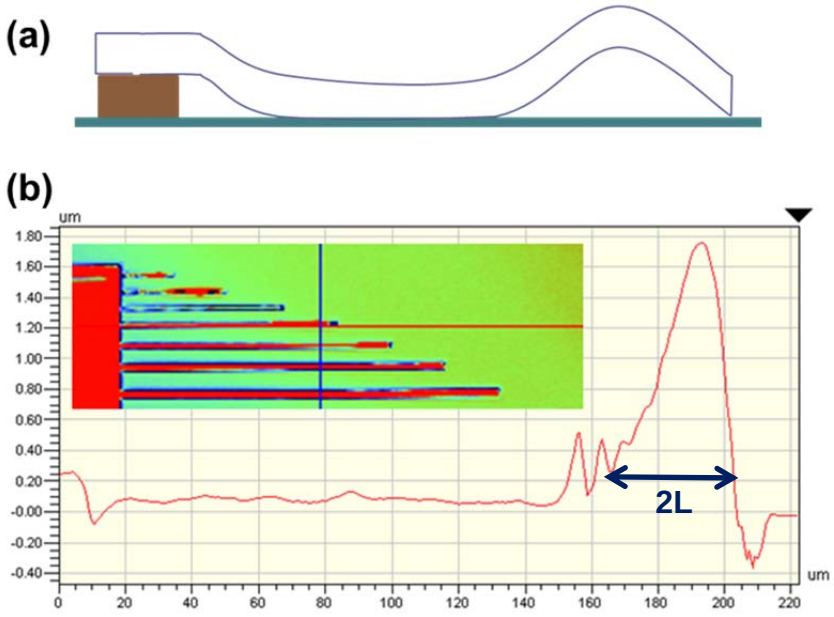


Figure 4.4. Profile of test structure cantilever beams formed with the Al_2O_3/TiN/poly-SiGe structural stack. (a) Simplified cross-sectional schematic view showing beam bending suggested by white light interferometry, with majority of the cantilever beams stuck to substrate and the tip region showing a concave downward shape. (b) White light interferometry topograph and cross-sectional structural height measurement. The highest part of the arch was ~1.8 µm higher than the stuck-to-substrate region. The effective beam length (= 2L) used for strain gradient calculation is noted on the figure.

Figure 4.5 shows the calculated strain gradient from cantilever beam test structures for the 40 nm Al_2O_3 / 10 nm TiN / 100 nm poly-SiGe structural stack. The average strain gradient among beams ofr different lengths was -1.03×10^{-3} µm^{-1}. Ideally the gradient should be much lower than 10^{-3} µm^{-1} in order to achieve low operating voltages. Additional process development efforts were undertaken to reduce the strain gradient to an acceptable level.

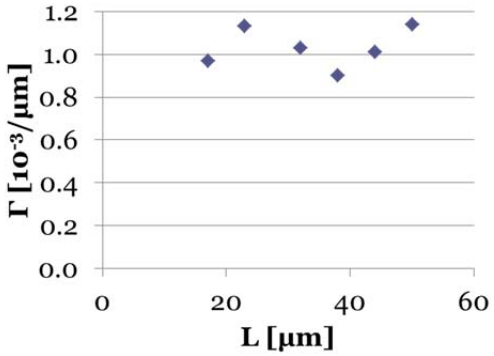


Figure 4.5. Calculated strain gradient for cantilevers of various beam lengths for the structural stack comprising a 100 nm-thick RT-CVD poly-SiGe film.

4.3.2 Stress Mismatch in Foundry-Fabricated Structural Films

In order to address the strain gradient issue in foundry-fabricated relays, it is important to understand the origin of strain gradient in the structural stack. For a simple cantilever structure with bending moment M in the vertical direction, a thinner structural layer can result in greater out-of-plane deflection Δz [6]:

$$\Delta z \propto \frac{ML^2}{EWH^3}. \tag{4.3}$$

For a complex multi-layer structural stack such as in the relay structure, the strain gradient cannot be easily predicted. Figure 4.6 shows the residual stress as a function of poly-SiGe thickness. The local residual stress (σ) is compressive at a roughly constant level for poly-SiGe thickness up to 2 μm. Since strain gradient Γ is related to the residual stress gradient by material constant E:

$$\Gamma = \frac{d\sigma}{dz}\frac{1}{E}, \tag{4.4}$$

a roughly uniform σ should yield a low-strain-gradient poly-SiGe film.

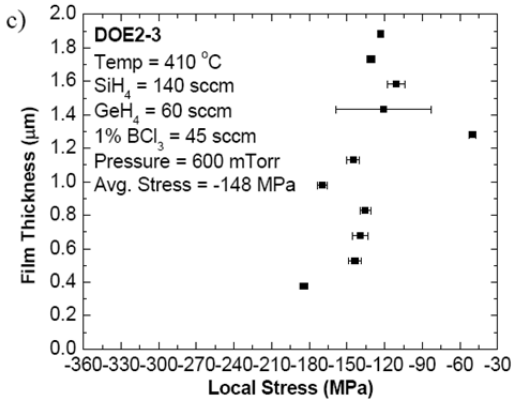


Figure 4.6. Local residual stress profile within a 2 μm-thick poly-SiGe thin film, showing compressive stress throughout the film and low stress variance at different depths within the film [7].

Furthermore, the low-temperature poly-SiGe deposition process typically forms a film that is amorphous at the bottom and eventually becomes polycrystalline at the top [7]. For SiGe thickness less than 500 nm, the film is largely amorphous, which generally yields low strain gradient due to its uniform microstructure.

Equation 4.4 shows that the average strain gradient in the film can be calculated from the stress profile. Figure 4.7 shows the measured average residual stress for the three different materials, with tensile (positive) residual stress for the 40 nm Al_2O_3 and 10 nm TiN films and compressive (negative) residual stress for the 100 nm poly-SiGe film. It is obvious that the strain gradient is negative from the bottom to the top of the structural stack. While the exact stress profile is unknown, the strain gradient can be estimated by assuming uniform stress throughout each film. The estimated strain gradient is -8.4×10^{-4} μm^{-1}, which is close to the measured -1.03×10^{-3} μm^{-1} value.

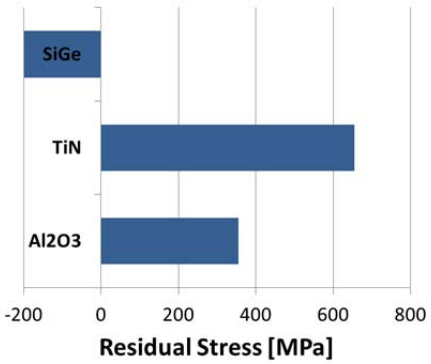


Figure 4.7. Measured residual stress of the three films within the structural stack.

4.3.3 Addressing Stress Mismatch

As discussed in section 4.3.2, the strain gradient of a multi-layer structural stack can be estimated by measuring the local residual stress for each layer within the stack. From a strain gradient perspective, it is clearly undesirable for a structural stack to consist of a strong compressive film at the bottom and a strong tensile film at the top, or vice versa. To address the stress mismatch issue present in the foundry-fabricated structural stack, as shown in Figure 4.7, it is desirable to find a tensile top film to reduce the strain gradient induced by the tensile bottom Al_2O_3 film (as the Al_2O_3 body dielectric is not easily replaceable due to process compatibility reasons). The tensile film on the top, which will serve as the stress compensation layer, must also be electrically conductive to allow the structure to be biased using a probe. A thin (10 nm) TiN layer deposited via atomic layer deposition (ALD) was selected as the stress compensation layer. Unfortunately, the high tensile stress from ALD TiN films over-compensated the stress and resulted in a large positive strain gradient. Figure 4.8 shows a tilted scanning electron microscopy (SEM) image of a released relay with 10 nm ALD TiN on the top of the structural stack. The effect of positive strain gradient can be clearly seen, with the folded flexure beams bending upward. Such bending can be confirmed by the interferometry measurement in Figure 4.9. The out-of-plane deflection at the end of folded flexures was ~3 μm, and the center plate was touching the gate electrode. No current could be measured from the relays with large positive strain gradient since the contact dimples are unable to touch the underlying source and drain electrodes. Pre-release and post-release thermal annealing experiments were performed to reduce the strain gradient, but these attempts were largely unsuccessful.

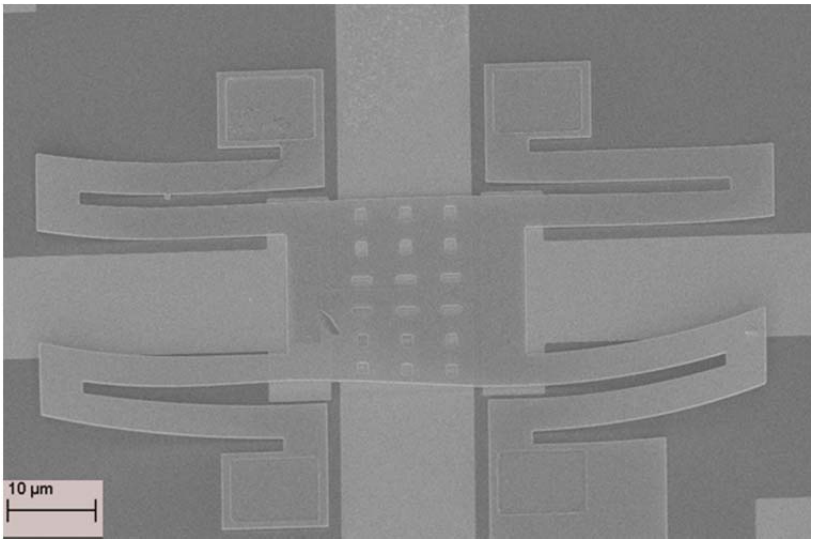


Figure 4.8. Tilted SEM micrograph of a relay with positive strain gradient due to stress mismatch. The ends of the folded flexure suspesion beams are bent upwards and the center of structure touched the underlying electrode layer.

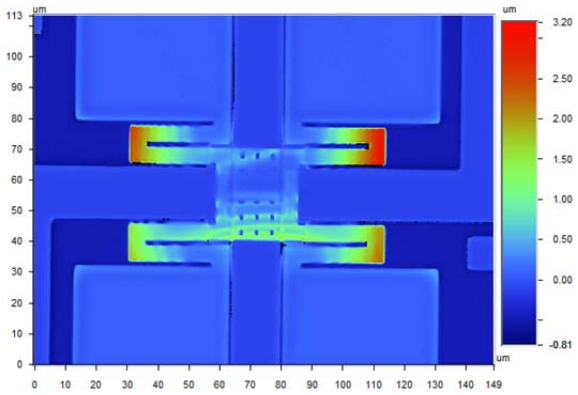


Figure 4.9. Interferometry measurement of a relay with a top TiN stress compensation layer. The positive strain gradient caused the ends of the folded flexures to be ~3 µm higher than in the center of the plate.

To fine-tune the stress profile of the structural stack, alternative methods of stress matching were explored. In the end, a two-step poly-SiGe deposition process was utilized to address this challenge. This resulted in a 10 nm ALD TiN film at the bottom and a roughly 200 nm of poly-$Si_{0.4}Ge_{0.6}$ film being deposited. Figure 4.10 shows the interferometry measurement result comparison between the single-step, ~100 nm and the two-step, ~200 nm poly-SiGe structures. The single-step poly-SiGe process resulted in significant downward bending from the center of structural stack to the end of folded flexures, which likely touched the Al_2O_3 substrate. The estimated T_{ACT} of this relay was >500 nm, which is much larger than the sacrificial oxide thickness (totaling 200 nm). The two-step poly-SiGe process resulted in a rather flat structure, with T_{ACT} estimated to be close to the designed 200 nm value. The relays fabricated using the two-step poly-SiGe deposition process will be characterized in section 4.4.

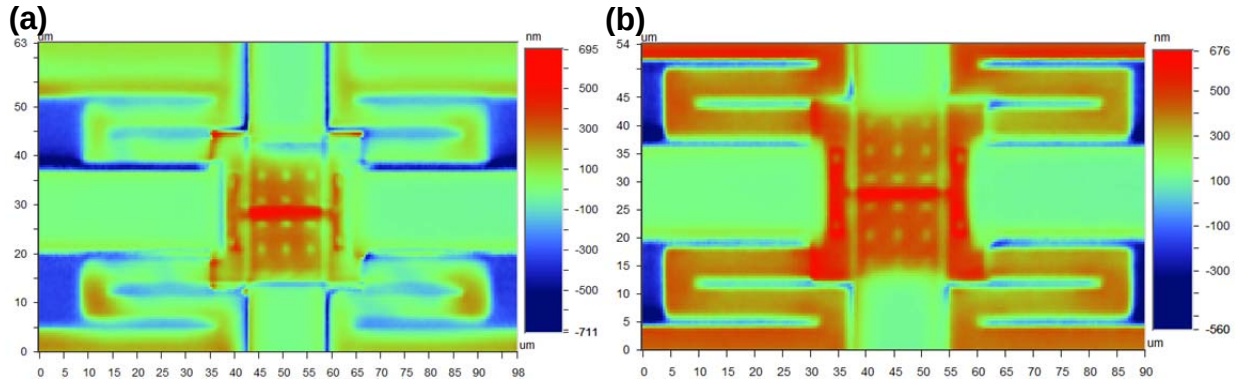


Figure 4.10. White light interferometry measurement of a released relay from (a) single-step 100 nm poly-SiGe deposition, showing concave downward shape and (b) two-step poly-SiGe deposition totaling ~200 nm, showing relatively flat center plate and folded flexures.

4.4 Characterization of Foundry-Fabricated Relays

4.4.1 Microscopy Results

Both baseline 4-terminal (4-T) and scaled 6-terminal (6-T) NEM relay designs, as discussed in chapter 1, were fabricated using the improved structural stack with ~200 nm of poly-$Si_{0.4}Ge_{0.6}$ as the main structural layer. The lateral dimensions of the center plate in the movable body structure are 30µm × 30µm for the 4-T relay design, which is similar to the design described in [10]. The 6-T design features the most scaled relay footprint to date, with 7.5µm × 7.5µm lateral dimensions for the movable center plate.

Figure 4.11 shows the SEM image of a released 4-T relay with the improved structural stack. Figure 4.12 shows the 3-D surface topography of a released relay, from which the strain gradient is deduced to be well below 10^{-3} μm^{-1}. The relatively low strain gradient is beneficial in preventing the increase of T_{ACT} upon release. T_{ACT} can also be gauged from Figure 4.12, which is not much larger than designed (~200 nm).

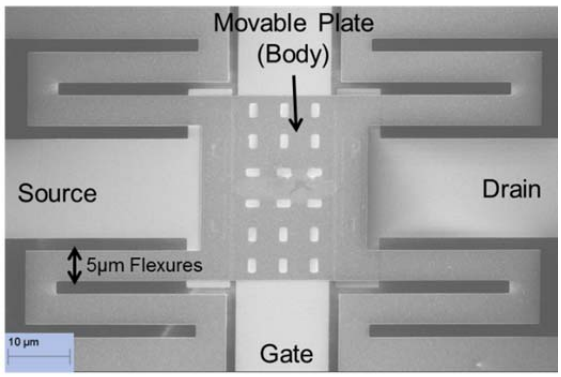


Figure 4.11. SEM image of a 4-T relay with improved structural stack [11].

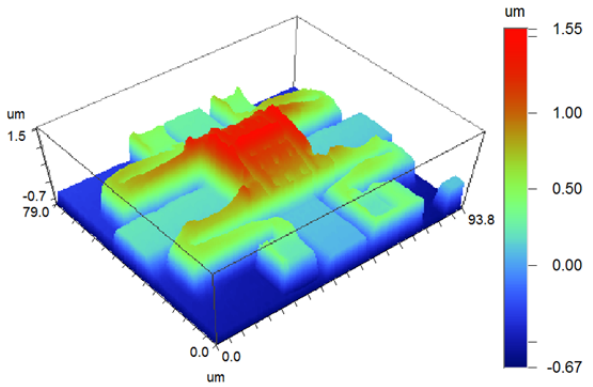


Figure 4.12. White-light interferometry topograph of a 4-T relay, showing that the released structure has relatively small strain gradient (-7×10^{-4} μm^{-1}) [11].

Figure 4.13 shows the SEM image of a released 6-T relay in this work, with all lateral dimensions scaled from the large baseline 4-T design. The two channels, which are narrow metallic layers attached to the underside of the movable body structure via an intermediary Al_2O_3 body dielectric layer, serves to bridge the source and drain electrodes when the relay is in the ON-state and are labeled in Figure 4.13. The out-of-plane deflection in this scaled structure is also less than for the baseline design, due to the increased rigidity for scaled lateral dimensions.

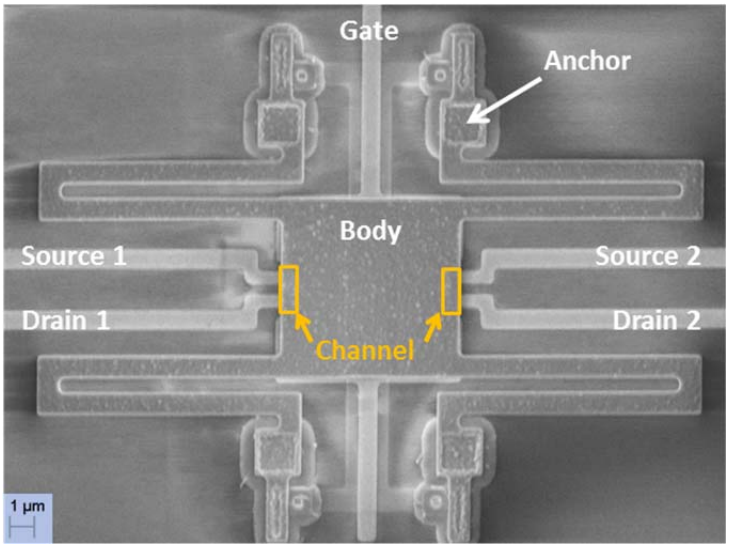


Figure 4.13. SEM image of a scaled 6-T relay with improved structural stack [11].

4.4.2 Electrical Characterization Results

Figure 4.14 shows the measured current-*vs*.-voltage (I_{DS}-V_G) curves for the baseline 4-T relay design (SEM micrograph shown in Figure 4.11). The operating voltages are low due to reduced strain gradient in the structural stack, with V_{PI} = 5.28 V and the hysteresis voltage $V_{PI} - V_{RL}$ = 0.48 V. The low hysteresis is particularly interesting as it allows the gate voltage (V_G) required to turn ON the relay to be further reduced by applying a negative voltage bias to the body electrode [10, 12]. In this case, V_{PI} can be reduced to <1 V with V_B = -4 V, indicating possible sub-1V circuit operation. For proper circuit operation, V_{RL} must be greater than 0 V; thus, the hysteresis voltage sets a lower limit for V_{PI} and hence the operating voltage (V_{DD}).

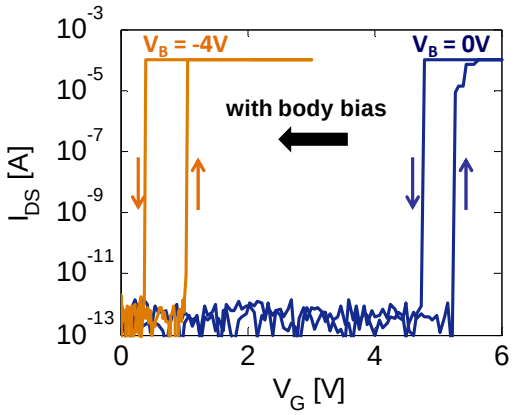


Figure 4.14. Measured I_{DS}-V_G characteristics for a 4-T relay, showing the effect of body biasing to reduce the switching voltages. The current compliance limit was set at 100 µA [11].

Figure 4.15 shows the SEM micrograph and measured I_{DS}-V_G characteristics for the 6-T relay (SEM micrograph shown in Figure 4.13). V_{PI} is larger (8.8 V) for this device because it has a 16x smaller actuation area. The lower ON-state drive current (i.e. higher ON-state resistance R_{ON}) and the non-abrupt switching behavior are due to the fact that the contacting electrode materials are RuO_2.

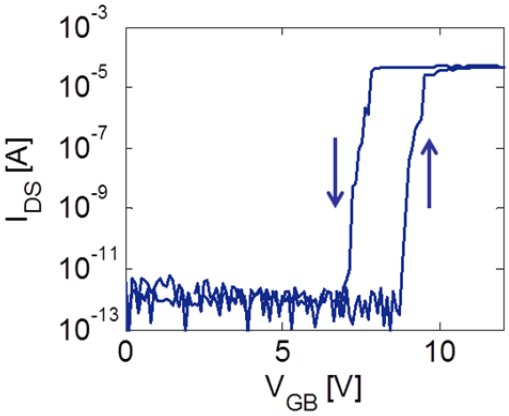


Figure 4.15. Experimental results for a 6-T relay with scaled lateral dimensions. (a) SEM image with the channel regions indicated. (b) Measured I_{DS}-V_G characteristics [11].

4.4.3 Temperature Dependence of Switching Voltages

The relays fabricated by the foundry have a complex multi-layer structural stack comprising of RT-CVD poly-SiGe, ALD TiN, and ALD Al_2O_3 layers. Thus, it is important to consider the mismatch in thermal expansion coefficient (α) between different materials, which may cause the operating voltages to depend strongly on the device operating temperature. Table 4.1 tabulates the thermal expansion coefficient of the materials in the structural stack. Although TiN has a large thermal expansion coefficient mismatch to both adjacent layers, the relay operating voltages are not expected to drift significantly with temperature since the TiN layer is very thin and the thermal expansion coefficient of the two thicker layers (i.e. poly-SiGe and Al_2O_3) closely match each other. Figure 4.16 confirms that the relay exhibits stable V_{PI} and V_{RL} at different operating temperatures.

TABLE 4.1

THERMAL EXPANSION COEFFICIENT OF RELEVANT MATERIALS

	α [$\times 10^{-6}$ K^{-1}]
Poly-SiGe	4.13
TiN	9.35
Al_2O_3	5.40

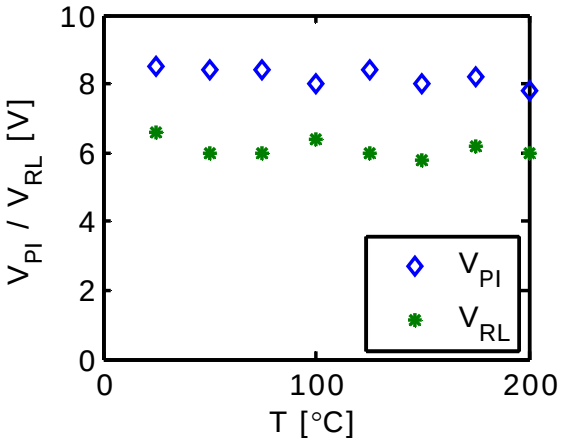


Figure 4.16. Measured switching voltages as a function of temperature, showing little variation. Electrical measurements were performed in N_2-purged chamber with a heated chuck. Device under test was the scaled 6-T relay [11].

4.5 Process Developments for Reducing Relay Operating Voltage

From the theoretical predictions in section 4.2 and experimental efforts in sections 4.3 and 4.4, it is clear that stress matching throughout the structural stack is essential for achieving low operating voltages for relay technology. In this section, strain gradient reduction is further explored via alternative non-SiGe structural materials and design improvements.

4.5.1 Metallic Structural Stack Development

To achieve low operating voltage for relay technology, alternative structural stacks are explored to replace the conventional SiGe/Al_2O_3-based structural stack. Desirable properties for the main structural layer include good electrical conductivity, low Young's modulus, high fracture strength, high yield strength, low processing temperature (<400ºC) for CMOS compatibility, etc. Metal and metal alloys can potentially fulfill these requirements since the processing temperature required for most physical vapor deposition (PVD) methods is generally low. Due to their high conductivity, metallic structures can be potentially much thinner than polycrystalline materials, leading to operating voltage reduction. For some metallic materials, the Young's modulus (E) or material hardness can also be smaller than poly-SiGe, which is around 150 GPa. Furthermore, the stress of metallic thin films often exhibit strong dependence on deposition condition and can potentially be tuned to match the stress of the body dielectric material. On the other hand, the stress of metallic thin films without proper tuning can be >10x larger than polycrystalline and amorphous silicon-germanium films, which can lead to adhesion and fracture issues [13].

Table 4.2 summarizes the metallic structural materials under consideration along with the body dielectric material in the structural stack. One of the most widely used materials with low Young's modulus is aluminum (Al), but the yield strength of pure Al is generally too low for practical use. It is found that the incorporation of scandium (Sc) can significantly improve the mechanical strength of Al without significantly increases the hardness [14]. Shape-memory alloys (SMA) such as nickel-titanium (Ni-Ti) alloys are attractive for MEMS applications due to their superelasticity, high strength (as high as 8% deformation), and low effective hardness [15, 16]. $TiAl_3$ has been proposed for bimorph MEMS structures due to its temperature stability, controllable stress and negligible stress gradient [17]. Finally, Al and AlN sputter-deposited in succession without breaking vacuum can potentially achieve better stress matching between metal and dielectric layers.

TABLE 4.2

METALLIC STRUCTURAL STACKS UNDER CONSIDERATION

Structure	Dielectric	*E* [GPa]	Summary
Al-Sc	Al_2O_3	~110	Film attacked during HF vapor release process
Ni-Ti	Al_2O_3	45-75	High-temperature annealing required
$TiAl_3$	Al_2O_3	216	Stress is tunable by varying deposition pressure
Al	AlN	70	Potentially good stress-matching

Unfortunately, Al-Sc and Ni-Ti alloys were found to be incompatible with the existing relay process flow. Figure 4.17 shows a fabricated Al-Sc test structure after being subjected to an HF vapor release process, clearly showing that the Al-Sc film was attacked. Films with different deposition conditions and different Sc compositions were also tested with similar results. For Ni-Ti alloys to exhibit desirable shape memory alloy properties, careful post-deposition high temperature annealing (>600ºC for several hours) is required [15]. Such high processing temperature is not compatible with CMOS back-end-of-line (BEOL) fabrication process.

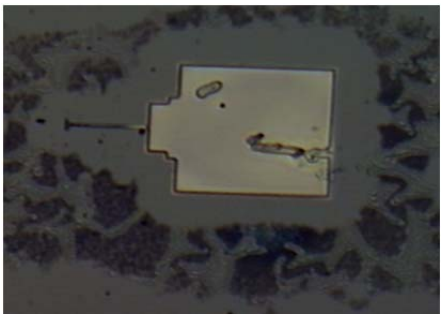


Figure 4.17. Optical micrograph of an Al-Sc thin film test structure after HF vapor release.

Initial experimental efforts indicated that $TiAl_3$-Al_2O_3 and Al-AlN stacks can potentially achieve low strain gradient throughout the structural stack. Figure 4.18 shows the deposition rate of $TiAl_3$ thin film deposited via a Randex Sputtering System and the estimated strain gradient of the $TiAl_3$-Al_2O_3 stack from interferometry measurements at various deposition pressures. The residual stress of $TiAl_3$ film can be tuned to match the stress of ALD Al_2O_3 film at elevated deposition pressure. Similarly, the strain gradient of an Al-AlN stack can be tuned by varying the deposition process conditions. Additional experimental efforts are required to further evaluate potential candidates.

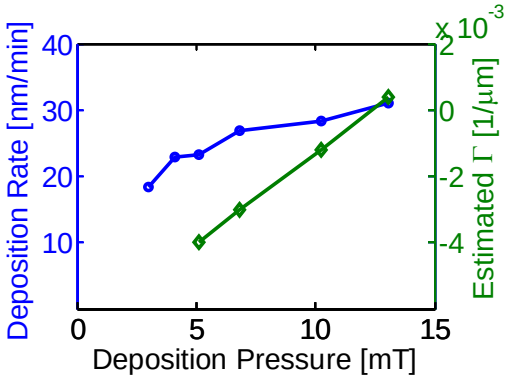


Figure 4.18. Deposition rate of $TiAl_3$ and strain gradient of $TiAl_3$-Al_2O_3 structural stack with $TiAl_3$ thin film deposited at various pressures.

4.5.2 Partial Removal of Body Insulator Layer

The strain gradient issue of the structural stack arises primarily from the stress mismatch between the body insulator Al_2O_3 layer and the main structural poly-SiGe layer. The average strain gradient in the poly-SiGe film, gauged from Figure 4.6, is actually fairly low. The effect of the Al_2O_3 body insulator layer can be minimized through design improvements. Figure 4.19 illustrates the design efforts to mitigate the strain gradient issue. Body insulator layer is essential in the center plate area for electrically separating the underlying channel strips from the body terminal, and to prevent current flow between gate and body terminals should the they accidentally touch each other. Body insulator is not necessary in the folded flexure area, but was not etched away for process simplicity reasons. The folded flexures exhibited the most out-of-plane deflection due to the strain gradient within the structural stack (ref. Figures 4.9 and 4.10a). In the improved design, the body insulator was selectively removed in the folded flexure regions in order to minimize the out-of-plane bending of the relay structure.

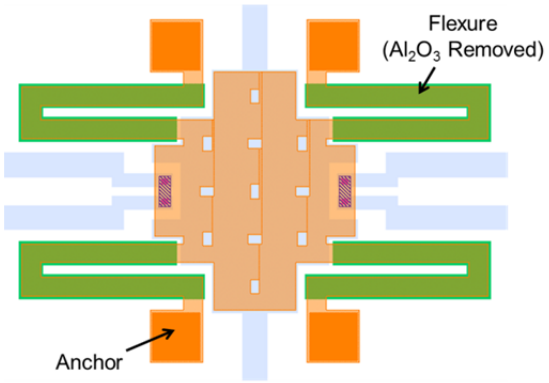


Figure 4.19. Simplified layout view of the relay design. The body insulator layer was removed in the folded flexure regions (green shaded).

Figure 4.20 compares the electrical measurement results of relays with and without body insulator in the folded flexure regions. In the original design (Figure 4.20a), V_{PI} is 13.5 V and the hysteresis voltage is extremely high because the ends of the flexures touch the substrate in the ON-state resulting in additional adhesion forces. Note the poly-SiGe film was heavily doped in this fabrication run so that the TiN layer was not necessary for electrical conduction, but the poly-SiGe film was not optimized to reduce strain gradient. For relays with identical poly-SiGe film and body insulator removed in the flexure region (Figure 4.20b), V_{PI} (6.9 V) and hysteresis voltage (<0.5 V) both significantly decreased, indicating successful reduction in out-of-plane deflection.

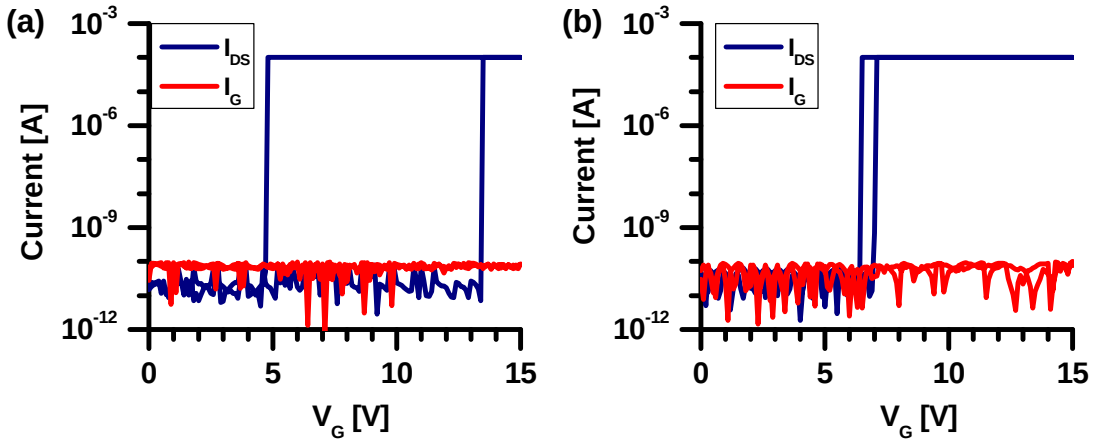


Figure 4.20. Relay I_{DS}-V_G characterisitcs for (a) original design in which poly-SiGe was covered with underlying Al_2O_3 body insulator throughout the structure, and (b) improved design in which the body insulator layer was removed in the folded flexure region.

4.6 Interconnect Technology for Relay-Based Integrated Circuits

Scaled relay technology has been shown to be a promising candidate for future energy-efficient digital logic applications. Process integration and design challenges have been overcome to achieve a reliable low-voltage relay technology while maintaining zero OFF-state leakage and abrupt switching characteristics. Several key digital logic blocks have been experimentally demonstrated using relays [1, 2]. To realize the full potential of logic relay technology, relay-based VLSI circuits must be demonstrated. Figure 4.21 shows the die photo of a relay-based microcontroller circuit with functional blocks labeled. Interconnects are required to wire the relays together appropriately. In this section, process requirements and challenges for relay interconnect technology are discussed.

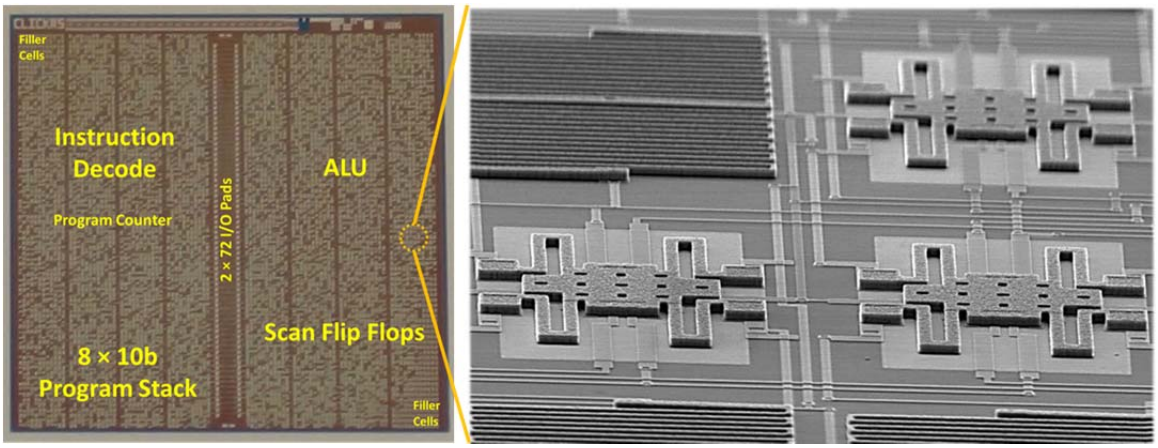


Figure 4.21. (Left) Die photo of a relay-based microcontroller featuring >12,000 relays. Main circuit functional blocks are labeled. (Right) Tilted SEM micrograph inside the microcontroller region, showing relay matrix and complex interconnect routing between relays.

4.6.1 Additional Process Requirements

Unlike conventional CMOS circuits, relay interconnects are built beneath the active device structure. This configuration also allows relays to be built on top of the CMOS "back-end-of-line" interconnect structures, to form CMOS-NEMS hybrid circuits. For process simplicity, only one extra level of interconnect is added between the Al_2O_3 substrate insulator and electrode metal layers in this work. Two additional layers and lithography masks, one for the conductive interconnect layer and one for the inter-metal dielectric (IMD) layer, are required to construct the interconnects.

In this work, 50-70 nm of W thin film was selected for the interconnect layer and ~50 nm of Al_2O_3 insulator was selected for the inter-metal dielectric (IMD) layer. Following the deposition of Al_2O_3 layer for substrate isolation, W thin film is deposited and patterned to form interconnects. A second layer of Al_2O_3 was then deposited via ALD to serve as the IMD layer. Vias are then opened on the IMD layer to allow electrical connection between interconnect and electrode layers, and relay structures are subsequently built using the integrated process flow discussed in section 3.2. The electrode layer, besides serving as biasing terminals for relays and landing pads for dimpled contacts, can also be patterned into thin metal lines for inter-relay electrical connection. Thus, the relays in microcontroller are connected via a two levels of (interconnect/electrode) metal lines with an insulating IMD layer in-between. Figure 4.22 shows the two-level metal lines with bottom interconnect lines running vertically and top electrode lines running horizontally. In regions where both interconnect and electrode lines are absent, the substrate is covered by two layers (substrate isolation and IMD) of Al_2O_3 insulator totaling ~130 nm in thickness.

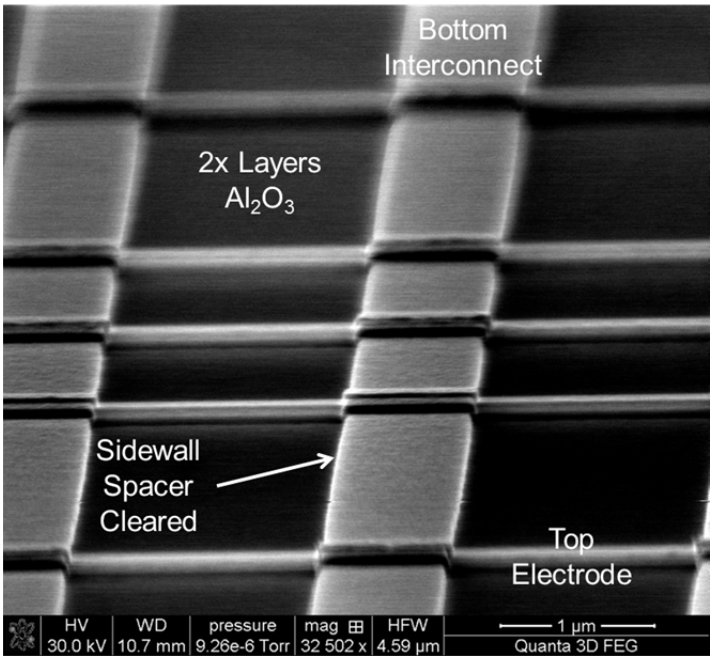


Figure 4.22. Tilted SEM micrograph showing the interconnect-electrode metal line matrix. Electrode sidewall stringers are notably absent along interconnect lines after etch process improvements.

From the process perspective, one immediate concern for this two-level metal line matrix is the sidewall spacer "stringers" when patterning electrode lines. Since the electrode layer is now deposited on an uneven surface with interconnect patterns, stringers can be formed along the edges of the interconnect lines after patterning the electrode layer. These stringers would result in undesired low-resistance current paths between electrode lines and must be removed. This challenge was addressed by adjusting the electrode etch recipe for lower directionality and longer overetch. Note that the stringers are not observed in Figure 4.22 after the etch process optimization.

4.6.2 Inter-Metal Dielectric Breakdown

The initial microcontroller fabrication run did not produce functional circuits as designed. Resistive connections between terminals were found instead of the desired switching behavior of relays. Figure 4.23 shows part of the microcontroller circuit in which the labeled relay was padded out along with many (>100) similar relays in parallel to allow for direct measurement of electrical device characteristics using the input/output pads. Measurements showed the collective resistance between parallel relays' gate and drain terminals is 296 kΩ, indicating that the IMD is leaky.

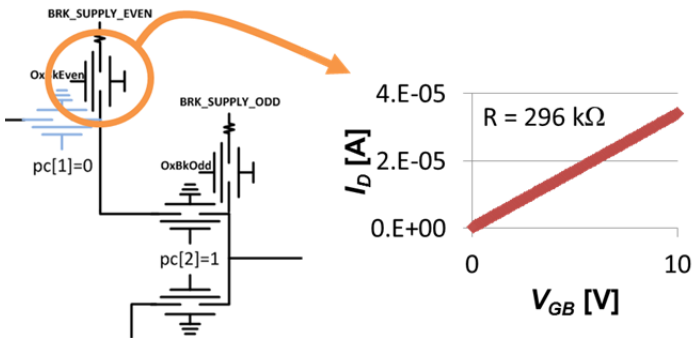


Figure 4.23. Partial circuit diagram showing the padded-out relay and the electrical measurement result with devices in parallel sharing the same set of I/O pads. The result clearly shows resistive behavior between gate and drain terminals of the parallel-connected relays.

A plausible explanation for the resistive behavior is due to IMD breakdown in the regions where the electrode metal lines cross over the interconnect metal lines (without vias, so that the IMD layer should insulate the two metal lines), and this theory was later confirmed via short-loop experiments. Figure 4.24 shows similar gate oxide breakdown behavior for CMOS circuits due to the so-called antenna effect. During the metal line plasma etch process, the metal lines act as antennas collecting charge from the plasma, resulting in large electric field across thin dielectric layers such as gate oxide. Although the IMD layer in the relay integrated-circuit process is not as thin as a CMOS gate oxide layer, the dielectric constant of Al_2O_3 is much larger than SiO_2 and the dielectric strength (i.e. breakdown electric field) of Al_2O_3 and SiO_2 are comparable (~5×10^6 V/cm). For relay circuits, the effect is the most prominent for long electrode lines with few crossovers to interconnect lines, since there is a higher amount of charge collected and the field across the IMD is concentrated at the few crossover regions. Note that the dielectric breakdown only happens during the overetch step of the electrode plasma etch process. Before the electrode layer is physically separated into lines and pads, the electrode layer is effectively a large equipotential metal pad, and the underlying interconnect lines share the same potential (i.e. no electric field is present) due to via connections.

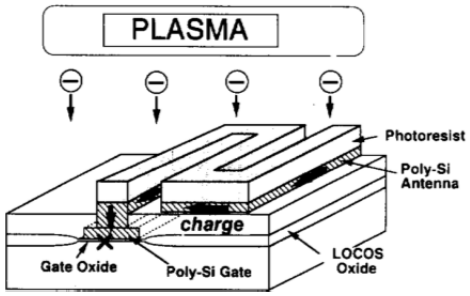


Figure 4.24. Schematic cross-section of CMOS circuits illustrating antenna breakdown effect at the gate oxide. Similar breakdown occurred at relay electrode-interconnect crossovers [18].

Design and process modifications were performed on relay circuits to mitigate plasma-induced dielectric breakdown in the IMD layer. Long electrode wires were rerouted and divided into shorter wires to minimize charge collection. A bi-layer electrode process was developed to eliminate electrode exposure to plasma during the overetch step.

4.6.3 Bi-Layer Electrode Development

Figure 4.25a shows a schematic cross-sectional illustration of the bi-layer electrode structure, with a top Ru layer serving as the contacting material and a bottom metal layer. After patterning Ru using a low-temperature oxide (LTO) hard mask, the bottom metal layer was etched using wet etchant solutions to form electrode lines and pads. Since the interconnect and electrode layers were still at the same electric potential at the end of Ru plasma etch process, plasma-induced dielectric breakdown is eliminated. The bottom metal layer should adhere well to both Ru and Al_2O_3, be able to withstand the Ru plasma etch process, and should be etched in a wet etchant that does not attack Ru. Nickle (Ni), aluminum (Al) and tungsten (W) were selected based on these requirements. Table 4.3 summarizes the process development results for bi-layer electrodes with various bottom metal layers. Ni was not completely etched away resulting insubstantial surface leakage current between electrodes on the substrate. Al was damaged during the LTO hard mask deposition process (in an LPCVD furnace at 400ºC) and hillocks were visible under an optical microscope, as shown in Figure 4.25b. After patterning the Al bottom metal layer, many electrode lines were found to be >100x more resistive than as deposited. Process development was more successful for a wet-etched W bottom layer, as the W layer can be removed from the field regions with small residue hillocks remaining on the substrate. Measurements showed negligible surface leakage, indicating the hillock residues were not shorting the electrode lines. Test structure characterization showed antenna-induced dielectric breakdown was successfully eliminated and the electrode-interconnect crossover points were showing good dielectric integrity.

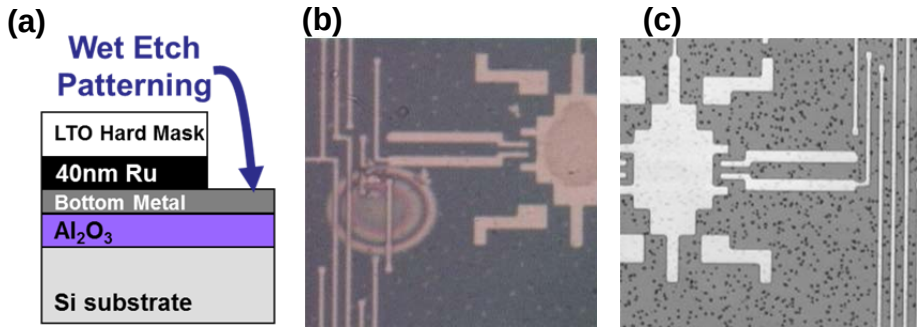


Figure 4.25. Bi-layer electrode process development. (a) Schematic illustrating electrode structure and indicating the use of a wet etch step after Ru plasma etching. (b) Microscope image showing damage to Al bottom metal layer after LPCVD furnace run. (b) Image showing hillock residues after wet etching with W as the bottom metal layer.

TABLE 4.3

BI-LAYER ELECTRODE PROCESS DEVELOPMENT RESULTS

Metal	Thickness	Etchant	Time	Summary
Ni	~20 nm	$HCl + HNO_3$	5 min.	Cannot remove Ni completely
Al	~20 nm	H_3PO_4-based Mix (50ºC)	20 sec.	Al damaged in LTO furnace (400ºC)
W	~20 nm	30%-H_2O_2 (50ºC)	30 sec.	OK; residues on the substrate

4.7 Summary

Relays with low pull-in and hysteresis voltages were demonstrated by optimizing the strain gradient and therefore minimizing the out-of-plane deflection of the structural stack. The theoretical origin of strain gradient was discussed and the results demonstrated the importance of stress matching between different layers in the structural stack. Relay design and process modifications were made while transferring the relay technology for fabrication in a foundry. Microscopy and electrical characterization showed that the foundry-fabricated relays have low strain gradient ($<1\times10^{-3}/\mu m$), low V_{PI} (~5 V), low hysteresis voltage (<1 V), and good V_{PI} stability across a wide range of operating temperatures. Scaled relays with the smallest layout footprint demonstrated to date have been fabricated using the foundry relay process flow. Low strain gradient metallic structural materials and design modifications for minimizing relay operating voltage were also investigated to significantly reduce V_{PI} and hysteresis voltages of relays.

In addition to the technology developments, relay-based VLSI circuits were designed and fabricated. Process challenges for fabricating VLSI circuits were identified and solutions were proposed. Plasma-charging-induced inter-metal dielectric breakdown was a significant challenge, and was solved by developing a bi-layer electrode process with the bottom W layer wet etched. These improvements to logic relay technology represent significant steps toward future low-cost and energy-efficient electronic systems.

4.8 References

[1] F. Chen, M. Spencer, R. Nathanael, C. Wang, H. Fariborzi, A. Gupta, H. Kam, J. Jeon, T.-J. King Liu, D. Markovic, V. Stojanovic and E. Alon, "Demonstration of Integrated Micro-Electro-Mechanical (MEM) Switch Circuits for VLSI Applications," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, San Francisco, CA, USA, 2010.

[2] M. Spencer, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. King Liu, D. Markovic, E. Alon and V. Stojanovic, "Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications," *IEEE J. Solid-State Circuits,* vol. 46, no. 1, pp. 308-320, 2011.

[3] H. Kam, E. Alon and T.-J. King Liu, "A Predictive Contact Reliability Model for MEM Logic Switches," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2010.

[4] P. M. Osterberg and S. D. Senturia, "M-TEST: A Test Chip for MEMS Material Property Measurement Using Electrostatically Actuated Test Structures," *IEEE/ASME J. MEMS,* vol. 6, no. 2, p. 107, 1997.

[5] J. Yaung, "NEM Relay Scaling for Ultra-low Power Digital Logic," Ph.D. Dissertation, University of California, Berkeley, 2014.

[6] S. D. Senturia, Microsystem Design, New York: Springer, 2004.

[7] C. W. Low, "MEMS with CMOS Electronics Novel Processes for Modular Integration of Silicon-Germanium," Ph.D. Dissertation, University of California at Berkeley, 2000.

[8] K. Nunan, G. Ready, P. Garone, G. Sturdy and J. Sledziewski, "Developing a Manufacturable Process for the Deposition of Thick Polysilicon Films for Micro Machined Devices," in *Proc. IEEE/SEMI Adv. Semicond. Manufact. Conf. Workshop*, Boston, MA, USA, 2000.

[9] T. Van der Donck, J. Proost, C. Rusu, K. Baert, C. Van Hoof, J.-P. Celis and A. Witvrouw, "Effect of Deposition Parameters on the Stress Gradient of CVD and PECVD Poly-SiGe for MEMS Applications," in *Proc. SPIE Conf.*, Denver, CO, USA, 2004.

[10] R. Nathanael, V. Pott, H. Kam, J. Jeon and T.-J. King Liu, "4-Terminal Relay Technology for Complementary Logic," in *IEDM Tech. Dig.*, Washington, D.C., USA, 2009.

[11] I.-R. Chen, L. Hutin, C. Park, R. Lee, R. Nathanael, J. Yaung, J. Jeon and T.-J. King Liu, "Scaled Micro-Relay Structure with Low Strain Gradient for Reduced Operating Voltage," *Electrochem. Soc. Trans.,* vol. 45, p. 101, 2012.

[12] J. Jeon, R. Nathanael, V. Pott and T.-J. King Liu, "Four-Terminal Relay Design for Improved Body Effect," *IEEE Elec. Dev. Lett.,* vol. 31, no. 5, pp. 515-517, 2010.

[13] J. Lai, "Novel Processes and Structures for Low Temperature Fabrication of Integrated Circuit Devices," Ph.D. Dissertation, University of California, Berkeley, 2008.

[14] Y. V. Milman, "High-Strength Aluminum Alloys," in *Metallic Materials with High Structural Efficiency*, Dordrecht, the Netherlands, Kluwer Academic Publishers, 2004, pp. 139-150.

[15] Y. Fu, H. Du, W. Huang, S. Zhang and M. Hu, "TiNi-based Thin Films in MEMS Applications: A Review," *Sens. Actuators A,* vol. 112, pp. 395-408, 2004.

[16] H. Kahn, M. A. Huff and A. H. Heuer, "The TiNi Shape-memory Alloy and its Applications for MEMS," *J. Micromech. Microeng.,* vol. 8, pp. 213-221, 1998.

[17] X. X. Qu, Q. X. Zhang, Q. B. Zou, N. Balasubramanian, P. Yang and K. Y. Zeng, "Characterization of TiAl Alloy Films for Potential Application in MEMS Bimorph Actuators," *Mater. Sci. Semicond. Processing,* vol. 5, no. 1, pp. 35-38, 2002.

[18] Y. Uraoka, K. Eriguchi, T. Tamaki and K. Tsuji, "Evaluation Technique of Gate Oxide Damage," *IEEE Trans. Semicond. Manufacturing,* vol. 7, no. 3, pp. 293-297, 1994.

Chapter 5

Nanomechanical Switch Designs to Overcome the Surface Adhesion Energy Limit

5.1 Introduction

Miniature mechanical switches have attracted significant attention for future energy-efficient digital logic integrated circuits due to their zero OFF-state leakage and abrupt switching characteristics [1]. Theoretical studies and experimental efforts have been undertaken to investigate nanometer-scale mechanical (nanomechanical) switches driven by electrostatic [2-4], piezoelectric [5], or magnetic forces [6], because the benefits of miniaturization include lower mechanical delay for faster circuit operation and lower operating voltage for lower switching energy [2, 7]. Furthermore, researchers have been investigating nanomechanical memory devices due to their superior scalability, low leakage, and non-volatility [8, 9]. Since a mechanical switch operates by making and breaking physical contact between conductive electrodes, researchers have studied contact scaling properties and closing/opening dynamics in order to predict its scaling limit [7, 10, 11]. It is generally believed that contact adhesion sets a lower limit for the switching energy of a mechanical switch [7, 11, 12].

In this chapter, compact (<1 μm^2 footprint), low-voltage (<0.1 V) nanomechanical switch designs that can overcome the contact adhesion switching energy limit are proposed. The proposed new switch designs utilize quantum mechanical tunneling as the conduction mechanism in ON-state. A model is developed to predict the switching energy of nanomechanical switches, and is used to analyze both conventional and tunneling switch designs. The proposed new switch design can be used for both logic and memory operations with slight alteration in design parameters. Initial experimental efforts in demonstrating the proposed tunneling switch design are also discussed. Finally, the total energy consumption of nanomechanical switches during one switching cycle is analyzed.

5.2 Modeling Methodology

In general, three types of force affect a nanomechanical switch: an applied force that actuates the suspended structure (i.e. actuator), surface adhesive force (F_{adh}) at the physical contact(s), and the spring restoring force (F_{spring}) of the suspended structure. The governing equations for these forces and their corresponding potential energies are modeled to assess the energy efficiency of nanomechanical switches of various designs [13].

5.2.1 Surface Adhesive Force

Due to surface roughness, the real contact area (A_c) usually is a small fraction of the apparent contact area (A_{cont}) [14]. F_{adh} includes van der Waals force, capillary force, and material bonding [10, 12]. For a metal-to-metal contact, which is desirable for low ON-state resistance, the metallic bonding force originating from electron interaction is dominant [7, 15]. The surface energy and force between metal interfaces can be modeled using the following universal relationship [16, 17]:

$$F_{adh}\left(d_{cont}\right) = 2\gamma A_c\left(\frac{d_{cont} - D_0}{\lambda_M}\right) \times \exp\left(-\frac{d_{cont} - D_0}{\lambda_M}\right) \tag{5.1}$$

$$E_{adh}\left(d_{cont}\right) = -2\gamma A_c\left(1 + \frac{d_{cont} - D_0}{\lambda_M}\right) \times \exp\left(-\frac{d_{cont} - D_0}{\lambda_M}\right), \tag{5.2}$$

where γ is the surface energy density, d_{cont} is the distance between the contacting electrodes, D_0 is the contact distance in equilibrium, and λ_M is a characteristic decay length related to the Thomas-Fermi screening length [16]. Thus the energy to separate two metal surfaces is $E_{adh}(\infty) - E_{adh}(D_0) = 2\gamma A_c$. λ_M is typically 0.5-1.5 Å for bulk materials [17], but is larger for a confined contact volume due to reduced electron density [18].

5.2.2 Spring Restoring Force

In general, the force that counteracts movement of a mechanical actuator away from its equilibrium position can be modeled as a spring restoring force with effective spring constant k_{eff}. The linear spring force F_{spring} and corresponding energy E_{spring} can be modeled using conventional Hooke's law:

$$F_{spring} = -k_{eff}\left(\Delta x\right) \tag{5.3}$$

$$E_{spring} = \frac{1}{2}k_{eff}\left(\Delta x\right)^2, \tag{5.4}$$

where Δx is the displacement of the suspended nanomechanical actuator.

The effective spring constant k_{eff} of a mechanical actuator differs with design, and generally depends on the physical geometric parameters and the properties of materials that constitute the actuator. For example, k_{eff} of a simple rectangular cantilever comprising homogeneous material actuated in the vertical direction can be modeled as:

$$k_{eff} = \frac{EWH^3}{4L^3}, \tag{5.5}$$

where E is the Young's modulus of the material, and W, L, H are the lateral width, length, and vertical height (thickness) of the rectangular cantilever beam.

5.2.3 Electrostatic Force

In this work, the applied force that actuates a nanomechanical switch is modeled as a parallel-plate electrostatic actuator, comprising an air gap between the capacitively coupled plate electrodes. The electrostatic force (F_{elec}) and energy (E_{elec}) can be analytically modeled as:

$$F_{elec} = \frac{\varepsilon_0 A_{act} V^2}{2d_{act}^2} \tag{5.6}$$

$$E_{elec} = -\frac{\varepsilon_0 A_{act} V^2}{2d_{act}}, \tag{5.7}$$

where ε_0 is the permittivity of air, d_{act} is the distance between the suspended actuator and actuation electrode (filled with air), A_{act} is the overlapping capacitive area, and V is the applied voltage across the air-gap of thickness d_{act}.

Although electrostatic force is assumed herein to be the actuation mechanism, the switch model can be easily adapted by replacing the electrostatic force equation with the appropriate governing equation, e.g. for piezoelectric force or magnetic force. Electrostatic actuation has the advantage of producing a relatively large force with a small actuator, and the actuation mechanism is highly scalable. Alternative mechanisms could be attractive in the future if a desirable material set can be found to effectively actuate switches with highly scaled dimensions.

5.3 Analysis of Conventional Switch Design

Conventional switch designs are analyzed herein to fully understand the relevant forces and potential energy of nanomechanical switches. Figure 5.1 illustrates the operation of a conventional 3-terminal mechanical switch design, showing the relevant forces and geometrical design parameters. In the OFF-state, a contact air gap separates the movable suspended electrode (which has an effective spring constant k_{eff}) from the fixed contacting electrode. When a sufficiently large voltage is applied between the suspended electrode and the actuator electrode ($V > 0$), $F_{elec} \geq F_{spring}$ such that the suspended electrode comes into contact with the contacting electrode so that the switch is turned ON. To turn OFF the switch, the applied voltage is removed

($V = 0$) and $F_{spring} > F_{adh}$ is required to break the contact. This means that F_{elec} must be greater than F_{adh}, and therefore contact adhesion sets a lower limit for the switching energy [7, 12]. Note that, as fabricated ($V = 0$), the actuation gap and area are larger than the contact gap and area, respectively (i.e. $g_{act} > g_{cont}$ and $A_{act} > A_{cont}$), for reliable low-voltage operation [19].

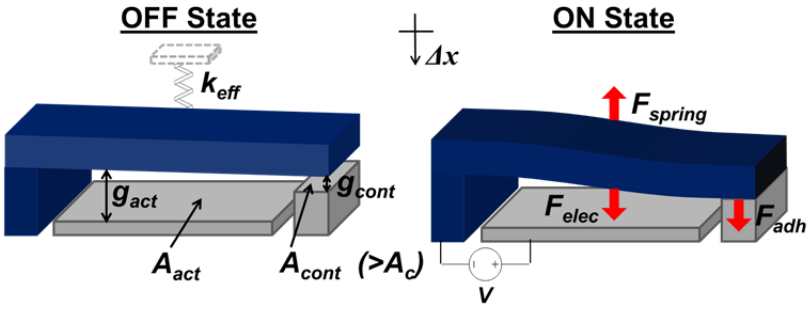


Figure 5.1. Isometric view of a conventional nanomechanical switch used for benchmarking. Key dimensions are labeled and relevant forces exerted on the actuator (indicated by red arrows) are illustrated. The actuator in this illustration is actuated vertically downwards [13].

Figure 5.2 shows how the net force on the suspended electrode ($F_{net} = F_{spring} + F_{elec} + F_{adh}$) depends on Δx, modeled using equations 5.1, 5.3, 5.6 and parameter values $A_{act} = 0.7$ µm^2, $g_{act} = 17$ Å, $A_c = 10$ nm^2 (note this number is much smaller than drawn contact area A_{cont}), $g_{cont} = 5$ Å and $k_{eff} = 195$ N/m. $V = 0.2$ V is applied to turn ON the switch. For the conventional switch design, $d_{cont} = D_0 + g_{cont} - \Delta x$ (ref. equation 5.1) and $d_{act} = D_0 + g_{act} - \Delta x$ (ref. equation 5.6). While aggressively scaled, these geometric dimensions are attainable with a state-of-the-art fabrication process today. When a sufficiently large actuation voltage ($V = 0.2$ V) is applied (ON-state), $F_{net} > 0$ for all $\Delta x < g_{cont}$ so that the suspended electrode moves into contact with the contacting electrode. When no voltage is applied (OFF-state), F_{spring} restores the suspended actuator back to $\Delta x \sim 0$, corresponding to the stable operating point where $F_{net} = 0$ and $dF_{net}/d(\Delta x) < 0$. Note that both conditions must be satisfied (zero force and negative force gradient) in order for the actuator to be stable at the corresponding position.

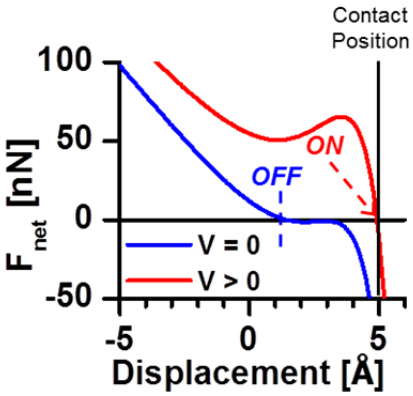


Figure 5.2. Net force (F_{net}) *vs.* displacement Δx curves for a conventional nanomechanical switch design [13].

Figure 5.3 shows the potential energy (E) plot, modeled using equations 5.2, 5.4, 5.7 and parameters and switching conditions corresponding to Figure 5.2. Local energy minima are observed at the stable operating points. The dynamic switching energies E_{off} and E_{on} can be calculated from the energy difference between ON-state and OFF-state displacements on the $V = 0$ (OFF) and $V > 0$ (ON) curves, respectively. In this design, the switch requires E_{on} = 19.03 aJ to turn ON and E_{off} = 3.95 aJ to turn OFF, for total energy of 22.98 aJ. Note that these energy values only accounts for the mechanically stored energy lost during switching and does not include the electrical energy required to charge the capacitive actuator. The total energy consumed by a nanomechanical switch during one switching cycle will be revisited in section 5.6. As explained in section 5.2.1, the minimum switching energy (i.e. surface adhesion energy) is $2\gamma A_c$, which is 22 aJ for aluminum (Al) contacting electrodes with γ = 1.1 J/m^2 and λ_M = 1.2 Å [20].

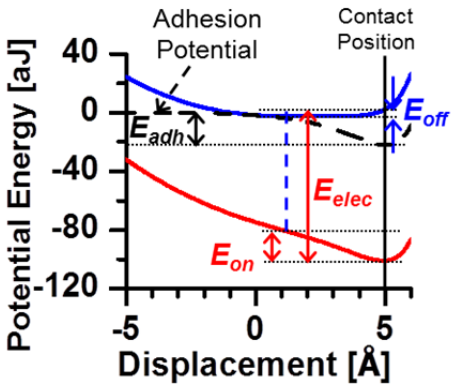


Figure 5.3. Potential energy profiles of a conventional nanomechanical switch, showing minima at $\Delta x \sim 0$ Å for OFF-state and Δx = 5 Å (in contact) for ON-state [13]. The electrostatic energy required to charge the capacitive actuator (E_{elec}) is also labeled.

5.4 Nanomechanical Tunneling Switch Design

Figure 5.4 illustrates the operation of a proposed tunneling switch design in which the actuator electrode and contacting electrode are located on opposite sides of the suspended electrode. The movable electrode has lower k_{eff} (172 N/m) compared to the conventional design so that F_{adh} actuates it close to contact without an applied voltage; F_{adh} and F_{spring} reach a balance within 1 Å of contact to allow for significant electron conduction via tunneling, so that this switch is normally ON (as fabricated). To turn OFF the switch, electrostatic force is applied to actuate the suspended electrode away from the contacting electrode and thereby reduce the tunneling current. Since F_{elec} and F_{spring} work together to counterbalance F_{adh}, less electrostatic force is needed to operate the switch. In the conventional design, $F_{elec} > F_{adh}$ is required to successfully operate the switch; such requirement is alleviated in this normally ON design. Note that while only 3-terminal switch designs are presented, 4-terminal switch designs that mimic transistor operation can be easily achieved by having two contacting electrodes and inserting an insulator to electrically insulate the tip of actuator (which serves as the "channel" bridge between two contacting electrodes) from the region overlapping with actuation electrode [21].

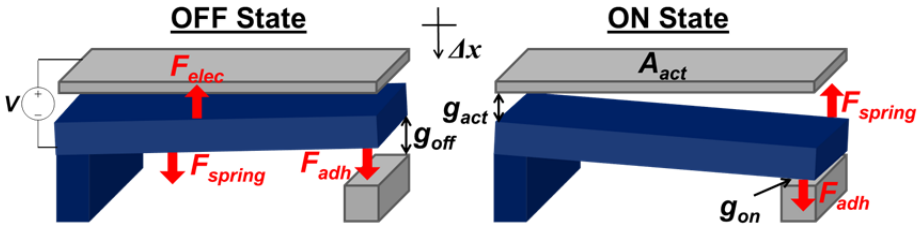


Figure 5.4. Isometric view of a tunneling nanomechanical switch in ON- and OFF-states. The switch in this illustration is turned ON by actuating the movable electrode vertically downwards with F_{adh} [13].

Figures 5.5 and 5.6 show the net force and potential energy plots for the tunneling switch design, respectively. $V = 0.1$ V is applied to turn OFF the switch. Note that $F_{net} = F_{spring} - F_{elec} + F_{adh}$ in the tunneling switch design due to the different electrode configuration. For the purpose of comparison, the actuation and contact design parameters (γ, λ_M, g_{cont}, g_{act}, A_c, and A_{act}) of this tunneling switch are taken to be identical to those of the conventional switch design in the previous section. Stable operating point and energy minima are found near contact ($\Delta x \sim g_{cont} - 1$ Å) with zero applied voltage, indicating $F_{adh} = F_{spring}$ balance is achieved with ~1 Å away from physical contacting position. With a small applied voltage (0.1 V), a stable operating point is reached near $\Delta x = 0$ for the OFF-state. Lower switching energy is achieved with this design ($E_{on} = 1.39$ aJ, $E_{off} = 1.90$ aJ) because the spring restoring force effectively reduces the depth of the potential well due to adhesive force (depicted by the dashed line in Figure 5.6) and prevents the suspended electrode from coming into contact with the contacting electrode (i.e. $\Delta x < g_{cont}$). The tradeoff is increased ON-state resistance due to the tunneling conduction mechanism. The tunneling current across an air gap is given by equation 5.8:

$$I_{tunnel} = CAV \exp\left(-ad_{cont}\sqrt{B}\right), \tag{5.8}$$

where $C \approx 3.16\times10^{13}$ A/m^2-V, A is the tunneling area, V is the applied voltage across contacting surfaces, $a = 10.25$ nm^{-1}, and B is the average barrier for an electron at the Fermi energy [22]. As a lower-bound $A = A_c = 10$ nm^2 and $B = 4.28$ eV (for Al contacts), R_{ON} can be calculated as $V/I_{tunnel} \approx 26.4$ kΩ. The small displacement (~4 Å) yields an ON/OFF current ratio of ~10^4; larger ON/OFF ratio is possible by tuning geometric parameters and material properties of the switch.

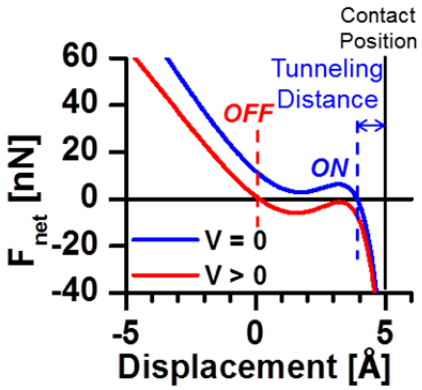


Figure 5.5. Force-*vs.*-Δx dependence of the proposed tunneling switch [13].

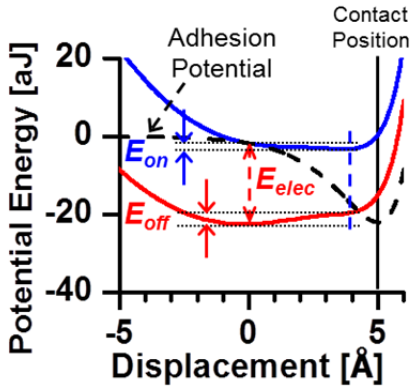


Figure 5.6. Potential energy of the tunneling nanomechanical switch system, showing minima near $\Delta x \sim 0$ Å for OFF-state ($V > 0$) and $\Delta x \sim 5$ Å (in contact) for ON-state ($V = 0$) [13]. The electrostatic energy required to charge the capacitive actuator (E_{elec}) is also labeled.

5.5 Complementary Tunneling Switch Design

5.5.1 Logic Operation

Figure 5.7 illustrates the operation of a complementary switch design with a set of actuation and contacting electrodes located on each side of the suspended electrode. The actuation electrodes are biased at the supply voltage (V_{DD}) and ground, while a variable input voltage is applied to the suspended structure. The suspended structure is actuated by electrostatic force from one contacting electrode to the other as the applied voltage switches between ground and V_{DD}. The gap between the suspended structure and the nearside contacting electrode is ~1 Å to allow electron conduction via tunneling, similar to the nanomechanical switch design discussed in section 5.4. The suspended structure is relatively stiff (i.e. large k_{eff}) in this design since F_{spring} needs to balance $F_{elec} + F_{adh,net}$ to avoid physical contact between the nearside contacting electrode ($g_{on} = 0$), which would require higher energy to break away. The switch is in logic operational mode since the suspended structure would return to the center position if all applied voltages are removed (due to large k_{eff} and $F_{adh,net} = 0$ at center position).

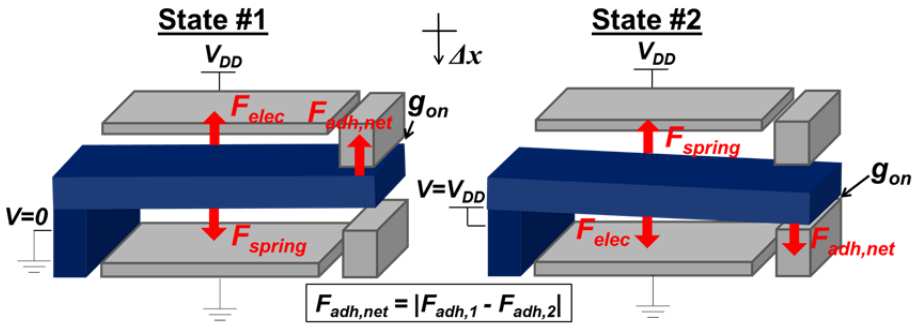


Figure 5.7. Isometric view of the complementary tunneling switch design in the two states, with applied voltage 0 and V_{DD}, respectively [13].

The 5-terminal switch design in Figure 5.7 can be engineered into 7-terminal switch design by separating the actuation terminals (the suspended structure and actuation electrodes) and the current conduction path (two contacting electrodes on each side of suspended electrode with "channel" tip bridging in between). Similar to the discussion in section 5.4 for transforming a 3-terminal switch into a 4-terminal switch, an insulator block can be inserted into the suspended structure near the tip to electrically insulate the channel tip from rest of the actuator. The 4-terminal (ref. section 5.4) and 7-terminal designs with actuation terminals separated from current conduction path is desirable for more versatile logic circuit applications.

Figures 5.8 and 5.9 show the force and energy modeling results, respectively, for a complementary switch design with actuator and contacting electrodes located on both sides of the suspended electrode. The supply voltage V_{DD} assumed in this model is 50 mV. Again, the actuation and contact design parameters (γ, λ_M, g_{cont}, g_{act}, A_c, and A_{act}) for this switch design are taken to be identical to those of the conventional switch design in section 5.3 to allow a fair comparison, and k_{eff} of this design is 183 N/m. The energy required to toggle between the two states (E_{switch}) is 2.21 aJ, significantly lower than $2\gamma A_c$ (22 aJ) due to the reduced potential well depth and non-contact operation.

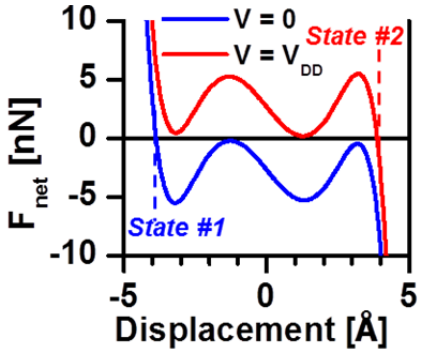


Figure 5.8. Force-*vs*.-Δx dependence of the complementary tunneling switch. The position of two complementary states are labeled and are ~1 Å away from the physical contacting positions (Δx = 5 Å and Δx = -5 Å) [13].

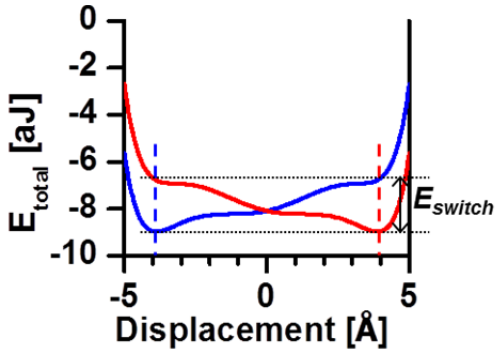
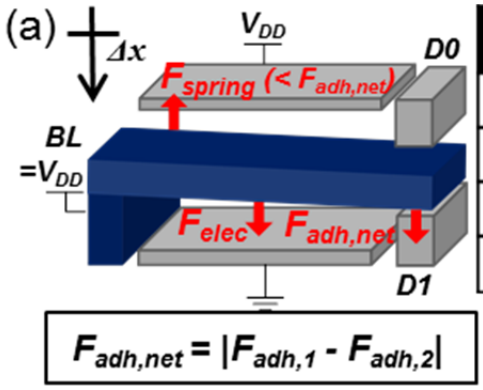


Figure 5.9. Potential energy profiles of the complementary tunneling switch system, showing minima near Δx = 5 Å and Δx = -5 Å for the two states [13].

5.5.2 Non-Volatile Switch Design

Figure 5.10 shows a complementary tunneling switch designed to operate as a non-volatile memory (NVM) cell, and the relevant biasing schemes. The device structure is identical to the structure shown in Figure 5.7, but k_{eff} is smaller (173 N/m) to allow the suspended structure to stay within tunneling distance to the nearside contacting electrode even when no voltages are applied. The suspended structure serves as the bit line (BL) and the two actuation electrodes are connected to V_{DD} and ground. The two contacting electrodes D1 and D0 correspond to '1' and '0' states, respectively.

During SET operation (shown in Figure 5.10a), BL = V_{DD} and the suspended structure moves to a position close to the D1 contacting electrode, achieving low R_{ON} between BL and D1 through tunneling. Similarly, during RESET operation BL = 0 and the structure moves close to contact with the D0 electrode. Stored data can be read by biasing the contacting electrodes D1 = V_{DD} and D0 = 0, transferring the voltage from D1/D0 to the floating BL. The key design parameter is k_{eff} for the suspended structure, to achieve a delicate balance between $F_{adh,net}$ and F_{spring} at a position near the D1/D0 electrodes when no voltages are applied to any of the terminals (i.e. during HOLD operation). V_{DD} is assumed to be 80 mV in this design.



(b)	BL	D0	D1	State
SET	V_{DD}	floating		'1'
RESET	GND	floating		'0'
READ	read	GND	V_{DD}	same
HOLD	floating			same

Figure 5.10. Complementary tunneling switch operated as a NVM cell: (a) illustration of cell structure during SET operation, showing various terminals and forces, and (b) biasing schemes.

Figures 5.11 and 5.12 show the force and energy modeling results, respectively, for the NVM cell during SET and HOLD operations. Note that the modeling results for RESET operation are simply anti-symmetric to the SET operation curves. During SET operation, the suspended structure is actuated electrostatically to a stable operating point ~0.5 Å away from the D1 contacting electrode. During HOLD, the suspended electrode moves slightly away from D1 to a stable operating point with g_{on} < 1 Å ('1' state). Compared to the logic mode operation, the potential well created by adhesion is larger due to smaller g_{on} and the required energy to switch between states is higher (E_{on} + E_{off} = 5.96 aJ) but still significantly lower than $2\gamma A_c$ (22 aJ).

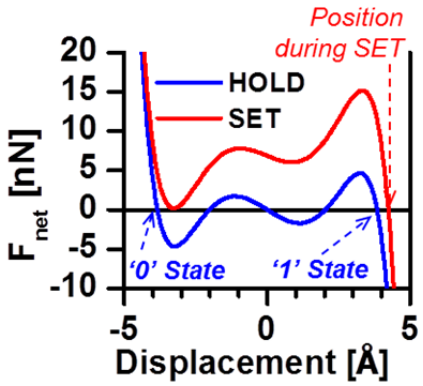


Figure 5.11. Force-*vs.*-Δ*x* dependence of the complementary tunneling switch in NVM mode.

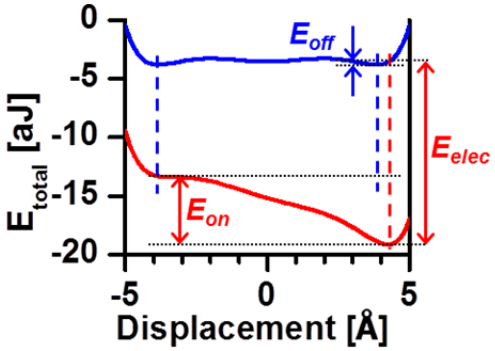


Figure 5.12. Potential energy profiles of the NVM cell during HOLD and SET operations. During HOLD, the suspended electrode is kept at local energy minima near Δ*x* = -5 Å and 5 Å ('0' and '1' states, respectively), hence the non-volatility. The electrostatic energy required to charge the capacitive actuator (E_{elec}) is also labeled.

5.5.3 Initial Experimental Results

To experimentally demonstrate complementary tunneling nanomechanical switches, a simple two-mask process has been designed and prototype switches have been fabricated. After depositing a Al_2O_3 substrate isolation layer, a thick (>500 nm) sacrificial SiO_2 layer is deposited and structural anchors are patterned using the anchor mask. The structural layer (e.g. Al in this experiment) is then deposited and patterned using the structure mask. The switches are then released in HF vapor which removes SiO_2 and suspends the movable structure (i.e. unanchored region). Figure 5.13 shows the layout view of the laterally actuated switch design. The movable beam is suspended between two actuation electrodes G_L and G_R, and k_{eff} of the suspended structure is mainly controlled by the design of folded flexure. The actuation electrodes, contacting electrodes (D_{L1}, D_{L2}, D_{R1}, D_{R2}), and one end of the flexure are all anchored to the substrate. Laterally actuated switch design is selected since it requires the fewest number of masks to fabricate. All electrodes can be defined by a single structure mask in a laterally actuated switch design, unlike vertically actuated switch design where complex process tuning is required to fabricate electrodes overhanging the moveable structure. As discussed in the modeling efforts,

it is critical to fabricate deep sublithographic gaps between the head of suspended beam and the contacting electrodes in order to achieve energy-efficient operation. The key design here is that the head of suspended beam and contacting electrodes are drawn to be connected on the mask. Sublithographic gaps will be formed in those connected regions through alternative methods.

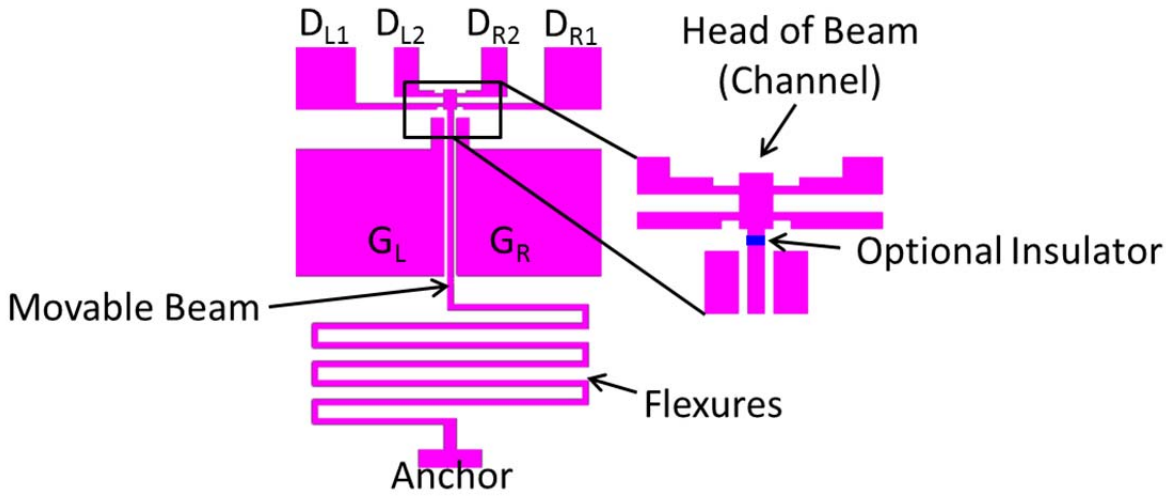


Figure 5.13. Schematic layout view of the complementary nanomechanical switch design. The switch actuates laterally by biasing actuation electrodes G_L and G_R. The head of the suspended beam is drawn to be connected to the anchored contacting electrodes. An optional mask for insulating channel from rest of the movable beam is also labeled.

An optional insulator block can be inserted to the movable structure to electrically insulate the channel (i.e. head of beam) from the rest of movable beam and forming a 7-terminal switch. indicated in Figure 5.13. The optional insulator mask was not used in the initial experimental efforts for process simplicity, thus the fabricated switch is essentially a 5-terminal switch.

The initial experiments formed the sublithographic gaps by overexposure during the structure lithography step and overetch in the Al plasma etcher. Figure 5.14 shows the scanning electron microscopy (SEM) images of the fabricated switch after HF vapor release process. While sublithographic gaps were indeed formed, the gap size was not controllable and was still too large to allow tunneling. Experimental efforts are underway to achieve controllable gap formation in deep sublithographic regime (i.e. a few angstroms).

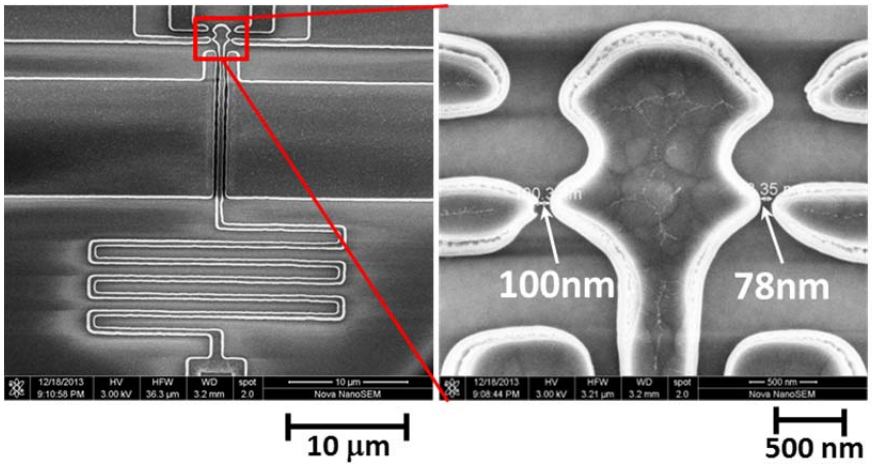


Figure 5.14. SEM micrographs of a released complementary nanomechanical switch. The lithographic limit of this process was 250 nm. Sublithographic gaps are clearly seen between head of suspended beam and contacting electrodes.

5.6 Total Energy Consumption of Nanomechanical Switches

As shown in sections 5.3-5.5, designing the nanomechanical switch so that electrostatic force counteracts the contact adhesive force is beneficial in reducing the mechanically stored energy lost by actuator movement. However, the energy consumption of nanomechanical switches from an electronic circuit standpoint involves the electrostatic energy (E_{elec}) required to charge the capacitor across g_{act}, which is labeled in Figures 5.3, 5.6, and 5.12. The minimum total energy consumed by a conventional nano-electro-mechanical switch is four times the adhesion energy [2] and is 88 aJ for the contact model parameters values used in this study. Table 5.1 summarizes the energy consumption over one switching cycle for the switch designs discussed in above. The mechanically stored energy is deduced from the switching energy in Figures 5.3, 5.6, 5.9, and 5.12. The electrostatic energy is the energy stored in the air-gap capacitor when voltage is applied; this energy is supplied from the voltage source external to the system, and will be dissipated when switch is turned OFF. Therefore E_{elec} represents the total switching energy of nanomechanical switches from a circuit perspective. By preventing physical contact and utilizing tunneling as the conduction mechanism, the total energy consumption can be lower than the surface adhesion energy, which represents more than 4x improvement in energy efficiency. For comparison, the switching energy of a state-of-art transistor is 100 aJ [23]. The energy consumption of nanomechanical switches can be further reduced by scaling switch dimensions, optimizing design parameters, and investigating alternative contact materials. If an alternative actuation mechanism is used, the model presented here can be adjusted by applying relevant governing equations, and the switching energy of a nanomechanical switch can be calculated using an analysis similar to the method set forth in this chapter.

TABLE 5.1

ENERGY CONSUMPTION OF NANOMECHANICAL SWITCHES

Switch Design	Conventional	Tunneling	Complementary	
			Logic	NVM
Mechanically Stored Energy [aJ]	22.98	3.29	2.21	5.96
Electrostatic Energy [aJ]	102.44	18.12	8.97	15.49
Adhesion Energy [aJ]	22.00			

5.7 Summary

The surface adhesion energy limit for a nanomechanical switch can be overcome by designing it to be normally ON so that spring restoring force effectively reduces the actuation force required to counteract the contact adhesive force. If the suspended structure is sufficiently stiff to prevent physical contact, then the total switching energy can be >4x lower than the contact adhesion energy. The design of k_{eff} is critical, as surface adhesion force is utilized for turning the switch ON and an overly stiff spring prevents the structure being actuated by adhesion force. The tradeoff for this tunneling-mode design is larger ON-state resistance (on the order of 10 kΩ) and reduced ON/OFF current ratio (~10^4).

Complementary tunneling switch designs are also proposed and can be operated in logic and NVM modes by adjusting the k_{eff}. A fabrication process flow and test structures were designed to demonstrate complementary nanomechanical switches. Initial experimental efforts were undertaken to form air gaps in deep sublithographic regime to allow for energy-efficient operation. The total energy consumed in one switching cycle is compared for the various nanomechanical switch designs. The results show significant energy savings for the proposed tunneling switch designs, as compared to both conventional nanomechanical switch designs and state-of-art transistors.

5.8 References

[1] M. Spencer, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. King Liu, D. Markovic, E. Alon and V. Stojanovic, "Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications," *IEEE J. Solid-State Circuits,* vol. 46, no. 1, pp. 308-320, 2011.

[2] H. Kam, T.-J. King Liu, V. Stojanovic, D. Markovic and E. Alon, "Design, Optimization, and Scaling of MEM Relays for Ultra-Low-Power Digital Logic," *IEEE Trans. Elec. Dev.,* vol. 58, no. 1, pp. 236-250, 2011.

[3] S. Chong, B. Lee, S. Mitra, R. T. Howe and H.-S. P. Wong, "Integration of Nanoelectromechanical Relays with Silicon nMOS," *IEEE Trans. Elec. Dev.,* vol. 59, no. 1, pp. 255-258, 2012.

[4] T. He, R. Yang, V. Ranganathan, S. Rajgopal, M. A. Tupta, S. Bhunia, M. Mehregany and P. X.-L. Feng, "Silicon Carbide (SiC) Nanoelectromechanical Switches and Logic Gates with Long Cycles and Robust Performance in Ambient Air and at High Temperature," in *IEDM Tech. Dig.*, Washington, DC, USA, 2013.

[5] U. Zaghloul and G. Piazza, "Sub-1-volt Piezoelectric Nanoelectromechanical Relays With Millivolt Switching Capability," *IEEE Elec. Dev. Lett.,* vol. 35, no. 6, pp. 669-671, 2014.

[6] D. Niarchos, "Magnetic MEMS: Key Issues and Some Applications," *Sens. Actuators A,* vol. 106, no. 1-3, pp. 255-262, 2003.

[7] C. Pawashe, K. Lin and K. Kuhn, "Scaling Limits of Electrostatic Nanorelays," *IEEE Trans. Elec. Dev.,* vol. 60, no. 9, pp. 2936-2942, 2013.

[8] L. Hutin, W. Kwon, C. Qian and T.-J. King Liu, "Electromechanical Diode Cell Scaling for High-Density Nonvolatile Memory," *IEEE Trans. Elec. Dev.,* vol. 61, no. 5, pp. 1382-1387, 2014.

[9] S. W. Lee, S. J. Park, E. Campbell and Y. W. Park, "A Fast and Low-power Microelectromechanical System-based Non-volatile Memory Device," *Nat. Comm.,* vol. 2, p. 220, 2011.

[10] B. Jensen, K. Huang, L. L.-W. Chow and K. Kurabayashi, "Adhesion Effects on Contact Opening Dynamics in Micromachined Switches," *J. Appl. Phys.,* vol. 97, p. 103535, 2005.

[11] A. Knoll, D. Grogg, M. Despont and U. Duerig, "Fundamental Scaling Properties of Electro-mechanical Switches," *New J. Phys.,* vol. 14, p. 123007, 2012.

[12] J. Yaung, L. Hutin, J. Jeon and T.-J. King Liu, "Adhesive Force Characterization for MEM Logic Relays with Sub-micron Contacting Regions," *IEEE/ASME J. MEMS,* vol. 23, no. 1, pp. 198-203, 2014.

[13] I.-R. Chen, C. Qian, E. Yablonovitch and T.-J. King Liu, "Nanomechanical Switch Designs to Overcome the Surface Adhesion Energy Limit," *to be published,* 2014.

[14] B. N. J. Persson, "Contact Mechanics for Randomly Rough Surfaces," *Surface Sci. Rep.,* vol. 61, no. 4, pp. 201-227, 2006.

[15] A. Banerjea, J. Ferrante and J. R. Smith, "Adhesion at Metal Interfaces," in *Fundamentals of Adhesion*, New York, Plenum Press, 1991, pp. 325-348.

[16] J. H. Rose, J. Ferrante and J. R. Smith, "Universal Binding Energy Curves for Metals and Bimetallic Interfaces," *Phys. Rev. Lett.,* vol. 47, no. 9, pp. 675-678, 1981.

[17] J. H. Rose, J. Ferrante and J. R. Smith, "Universal Features of Bonding in Metals," *Phys. Rev. B,* vol. 28, no. 4, pp. 1835-1845, 1983.

[18] A. Schirmeisen, G. Cross, A. Stalder, P. Grutter and U. Durig, "Metallic Adhesion and Tunnelling at the Atomic Scale," *New J. Phys.,* vol. 2, p. 29, 2000.

[19] F. Chen, H. Kam, D. Markovic, T.-J. King Liu, V. Stojanovic and E. Alon, "Integrated Circuit Design with NEM Relays," in *Proc. IEEE/ACM Int. Conf. Computer Aided Design*, San Jose, CA, USA, 2008.

[20] J. Israelachvili, Intermolecular & Surface Forces, 3rd. Ed., New York: Academic Press, 2011.

[21] R. Nathanael, V. Pott, H. Kam, J. Jeon and T.-J. King Liu, "4-Terminal Relay Technology for Complementary Logic," in *IEDM Tech. Dig.*, Washington, DC, USA, 2009.

[22] E. C. Teague, "Room Temperature Gold-vacuum-gold Tunneling Experiments," *J. Res. Natl. Bur. Stand.,* vol. 91, no. 4, pp. 171-233, 1986.

[23] "International Technology Roadmap of Semiconductor," 2013. [Online]. Available: http://www.itrs.net/Links/2013ITRS/Summary2013.htm.

Chapter 6

Conclusion

6.1 Contributions of This Work

This dissertation aims at advancing relay technology to make it suitable for future ultra-low-power swarm information processing, as conventional CMOS technology is faced with the challenge of fundamentally limited energy efficiency. Relays are attractive for this application due to their essentially zero leakage current and perfectly abrupt switching between ON/OFF-states, which enables them in principle to overcome the energy efficiency limit of CMOS technology by eliminating OFF-state leakage power. This work focuses on addressing two major challenges for NEM relay technology development: improving relay reliability and scaling relay operating voltages. Solutions are proposed and demonstrated via material and process integration efforts. The dynamic switching energy limit of generalized nanomechanical switches is also explored and energy-efficient switch designs are proposed.

Prototype logic relays employing tungsten (W) as the contacting material suffer from ON-state resistance (R_{ON}) instability due to native oxide formation (i.e. WO_x) at the contacting surfaces [1]. Alternative contacting material candidates are examined and the results indicated that ruthenium (Ru) offers the best combination of conductive native oxide (i.e. RuO_2), good hardness, excellent thermal stability, and CMOS compatible process. Integration challenges for implementing Ru as the contacting material, including poor adhesion to adjacent films, plasma etching rate optimization and residue cleaning, and lithography incompatibility are resolved by refining the device fabrication process flow. A fully integrated process flow for fabricating Ru-contact relays is then presented and successfully fabricated Ru-contact relays are characterized. The results confirmed that Ru-contact relays achieve sufficiently low R_{ON} with superior stability when compared to W-contact relays, as well as low pull-in and hysteresis voltages. The results pave a promising pathway to future ultra-low-power relay-based digital logic.

High-voltage operation is a major concern for relay endurance and energy efficiency [2]. For the logic relays in this work, the high operating voltage originates from strain gradient in the relay structure, due to stress mismatch between the different layers in the structural stack. Relay designs and process flow are modified to achieve better stress matching in the structural stack. Characterization of relays with a low-strain-gradient structural stack yielded relatively low pull-in voltage (~5 V), low hysteresis voltage (<1 V), and good temperature stability. Furthermore, relays with scaled footprint and interconnect technology for relay circuits are demonstrated. These advancements to relay technology are important for future VLSI circuit demonstration.

To explore the ultimate limit of nanomechanical switches, a model is derived to predict the dynamic switching energy limit. Contrary to the general belief, the energy consumption of nanomechanical switches can be lower than the surface adhesion energy. The surface adhesion energy limit can be overcome by designing normally-ON switches so that spring restoring force reduces the actuation force required to switch states. New switch designs are proposed and the results are benchmarked to the conventional design with similar dimensions.

As we move into the era of ubiquitous computing and swarm information processing, energy-efficient switching devices will become ever more important [3]. With further improvements in scaling, variability and packaging, NEM relay technology can be a compelling alternative to CMOS technology for ultra-low-power applications.

6.2 Recommendation for Future Work

While this work shows advancements in several critical areas for NEM relay technology, there remains much to be done to realize mass production for relay-based VLSI circuits. The relays need to be smaller, more energy efficient, and more reliable to achieve their full potential. This section highlights potential research topics for future NEM relay technology, including theoretical investigations and experimental demonstrations. The list is by no means complete, as more challenges will arise as we move toward circuit- and system-level demonstrations of NEM relay technology. Nevertheless it is important to present the most critical challenges in the immediate future to guide research efforts.

6.2.1 Demonstration of Relay-Based VLSI Circuits

While the efforts to develop a reliable interconnect layer underneath relays for circuit implementation is presented in this work, fabricating relay-based VLSI circuits remains a challenge for the near future. Smaller scale circuits have been demonstrated in [4-7], but integrating large-scale functional blocks requires co-optimization of relay development, circuit design, and interconnect design efforts. Figure 6.1 shows the layout view of the latest relay-based microcontroller design, with two levels of interconnects. Yield and variability are important issues to address. Ru-contact relays offers stable R_{ON}, but endurance must be further

improved by reducing the operating voltage. To achieve lower relay operating voltages, an advanced structural stack with even lower strain gradient must be developed and the variability of the fabricated devices must be controlled. Friction polymer formation must be further reduced by thorough cleaning and hermetically sealed packaging solutions [8, 9]. Finally, reducing the 6-terminal relay footprint can be beneficial for compact circuit demonstration and energy scaling [10].

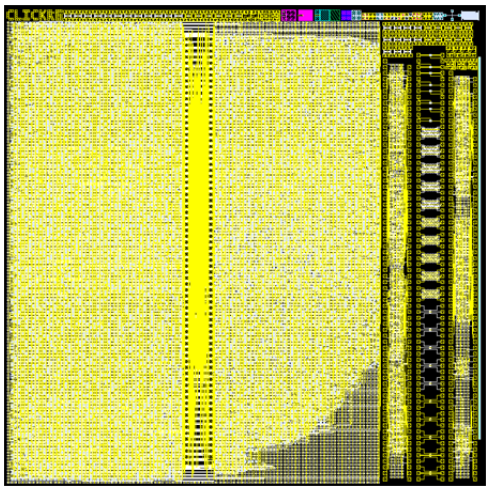


Figure 6.1. Die photo of the latest relay-based microcontroller design. The dimension of this chip is roughly 1 cm × 1 cm.

6.2.2 Nanomechanical Switch for Overcoming Surface Adhesion

Preliminary force and energy models are presented in this work for a generalized nanomechanical switch, and initial efforts toward experimental demonstration of an energy efficient switch are presented. A more thorough and sophisticated model can be developed by taking into account more detailed physical interactions in the system, and more performance metrics such as speed can be predicted. The new switch designs for overcoming surface adhesion limit are yet to be optimized, and sensitivity analysis will be needed to guide the optimization efforts. Near-term experimental demonstrations should focus on forming deep sublithographic air gaps at the contacts, perhaps by looking into techniques of forming air gaps in CMOS back-end interconnects [11, 12].

6.2.3 Monolithic Integration with CMOS Technology

Monolithic integration of NEM relays with CMOS technology offers a hybrid approach to energy efficient computing while maintaining the computational speed of CMOS transistors. Modular integration of relays on top of fully fabricated CMOS transistors and interconnect (i.e. a "MEMS-last" approach) will open up new horizons for system-on-a-chip applications that take advantage of both the superior speed of CMOS transistors and unique characteristics (e.g. ultra-low leakage power) of NEM relays [13]. It is important to constrain the process thermal budget of the NEM relay process flow to not exceed the limit imposed by the interconnects. Figure 6.2 shows the vision for relay-CMOS integration, with relays and transistors interconnected via the metallization stack in-between. This modular and monolithic integration allows the processes for CMOS transistors and NEM relays to be independently optimized while minimizing interconnect parasitics [13]. This integration approach is very attractive for low-power ubiquitous computing applications, and should be strongly considered for NEM relay technology.

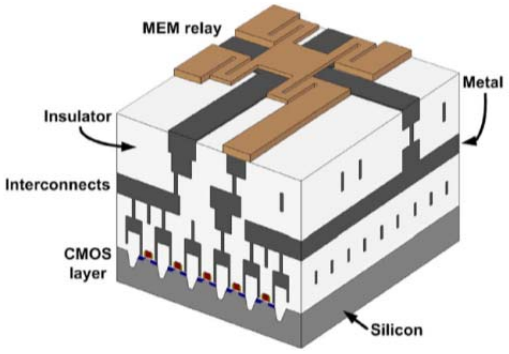


Figure 6.2. 3-D schematic of relay-last integration with CMOS circuitry.

6.3 References

[1] Y. Chen, R. Nathanael, J. Jeon, J. Yaung, L. Hutin and T.-J. King Liu, "Characterization of Contact Resistance Stability in MEM Relays With Tungsten Electrodes," *IEEE/ASME J. MEMS*, vol. 21, no. 3, pp. 511-513, 2012.

[2] O. Y. Loh and H. D. Espinosa, "Nanoelectromechanical Contact Switches," *Nat. Nanotech.*, vol. 7, no. 5, pp. 283-295, 2012.

[3] J. M. Rabaey, "The Swarm at the Edge of the Cloud—A New Perspective on Wireless," in *Symp. VLSI-C*, Honolulu, HI, USA, 2011.

[4] F. Chen, H. Kam, D. Markovic, T.-J. King Liu, V. Stojanovic and E. Alon, "Integrated Circuit Design with NEM Relays," in *Proc. IEEE/ACM Int. Conf. Computer Aided Design*, San Jose, CA, USA, 2008.

[5] F. Chen, M. Spencer, R. Nathanael, C. Wang, H. Fariborzi, A. Gupta, H. Kam, J. Jeon, T.-J. King Liu, D. Markovic, V. Stojanovic and E. Alon, "Demonstration of Integrated Micro-Electro-Mechanical (MEM) Switch Circuits for VLSI Applications," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, San Francisco, CA, USA, 2010.

[6] M. Spencer, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. King Liu, D. Markovic, E. Alon and V. Stojanovic, "Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 308-320, 2011.

[7] H. Fariborzi, F. Chen, R. Nathanael, I.-R. Chen, L. Hutin, R. Lee, T.-J. King Liu and V. Stojanovic, "Relays do not Leak–CMOS does," in *50th Design Automation Conf.*, Austin, TX, USA, 2013.

[8] L. Chen, H. Lee, Z. J. Guo, N. E. McGruer, K. W. Gilbert, S. Mall, K. D. Leedy and G. G. Adams, "Contact Resistance Study of Noble Metals and Alloy Films using a Scanning Probe Microscope Test Station," *J. Appl. Phys.*, vol. 102, no. 7, p. 074910, 2007.

[9] E. S. Park, J. Jeon, V. Subramanian and T.-J. King Liu, "Inkjet-printed Microshell Encapsulation: A New Zero-level Packaging Technology," in *Proc. IEEE 25th Int. Conf. MEMS*, Paris, France, 2012.

[10] J. Yaung, "NEM Relay Scaling for Ultra-low Power Digital Logic," Ph.D. Dissertation, University of California, Berkeley, 2014.

[11] L. G. Gosset, V. Arnal, C. Prindle, R. Hoofman, G. Verheijden, R. Daamen, L. Broussous, F. Fusalba, M. Assous, R. Chatterjee, J. Torres, D. Gravesteijn and K. C. Yu, "General Review of Issues and Perspectives for Advanced Copper Interconnections using Air Gap as Ultra-low K Material," in *Proc. IEEE Int. Interconnect Technol. Conf.*, Burlingame, CA, USA, 2003.

[12] K. Schuegraf, M. C. Abraham, A. Brand, M. Naik and R. Thakur, "Semiconductor Logic Technology Innovation to Achieve Sub-10 nm Manufacturing," *IEEE J. Elec. Dev. Soc.*, vol. 1, no. 3, pp. 66-75, 2013.

[13] G. K. Fedder, R. T. Howe, T.-J. King Liu and E. P. Quevy, "Technologies for Cofabricating MEMS and Electronics," *Proc. IEEE*, vol. 96, no. 2, pp. 306-322, 2008.