Novel Processes for Poly-Si Thin-Film Transistors on Plastic Substrates

by

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Abstract

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Flat panel display costs have been decreasing rapidly in recent years, due to swift progress in thin-film transistor (TFT) processing technology. The next step to a lower cost and more versatile display is the fabrication of displays on flexible plastic substrates. In order to realize this goal, high performance devices need to be fabricated in a process compatible with the low thermal budget of these substrates. Plastic compatible polycrystalline silicon (poly-Si) TFT processes are widely known, but several crucial steps have not been adapted to the low-temperature substrates. This work seeks to address several of the limiting factors in the plastic-compatible poly-Si TFT process.

Poly-Si devices have a large number of crystalline defects, which are typically made electrically inactive through a hydrogen plasma annealing process. However, hydrogen plasma annealing requires temperatures not compatible with low-cost plastic substrates. This work demonstrates an alternative passivation technique, implanting an impurity into the amorphous silicon film immediately after deposition. During subsequent laser crystallization, the impurity species is able to diffuse to grain boundaries and passivate defects, achieving an effect similar to hydrogen passivation. Performance and reliability of

this defect passivation process is compared with hydrogen plasma passivation in low and high temperature fabrication processes.

Two other novel processes were investigated. A reactively sputtered gate dielectric layer was used to replace one deposited with a more conventional high density plasma. Device performance was limited compared with high-quality SiO_2 deposition processes, but was sufficient for demonstration of passivation effects in a plastic-compatible process using the previously described technique.

Finally, the use of a visible copper vapor laser as an alternative to UV excimer laser for crystallization of amorphous silicon was demonstrated. Uniformity of fabricated devices without any passivation treatment was far superior when the copper vapor laser was used for crystallization. This is due both to its better pulse energy stability and to the lower sensitivity of the process at longer wavelengths.

Professor Tsu-Jae King Liu
Dissertation Committee Chair

To my wonderful friends and family.

Contents

List of Figures

List of Tables

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Chapter 1

Introduction

1.1 Display Technologies

1.1.1 Cathode Ray Tubes to Flexible Displays

Cathode ray tube displays (CRTs) were invented and made practical in the final years of the 19th century, before semiconductors, electronics, or even electrons were well understood. The operation of a magnetically guided electron beam exciting a phosphor layer was an important tool in the discovery of the subatomic nature of the electron [1]. Simple oscilloscopes were constructed with CRTs to understand the properties of the first vacuum tube electronic devices, allowing design of the first analog electronics. By the 1950s, CRT technology and vacuum tube electronics had advanced to the point where electronic displays for use in the home were practical, revolutionizing contemporary society. Today, due to the long history of the CRT and the relatively simple technology involved, costs have descended to the point where even large, high-quality displays are inexpensive.

The drawback of CRT displays is their physical size. There is a minimum depth associated with the geometry of the display area, causing a CRT to have an undesirably large footprint and total volume. A schematic diagram of a CRT is seen in Fig. 1.1 [2]. The deflecting coils can only bend electrons up to a maximum angle, so the minimum tube

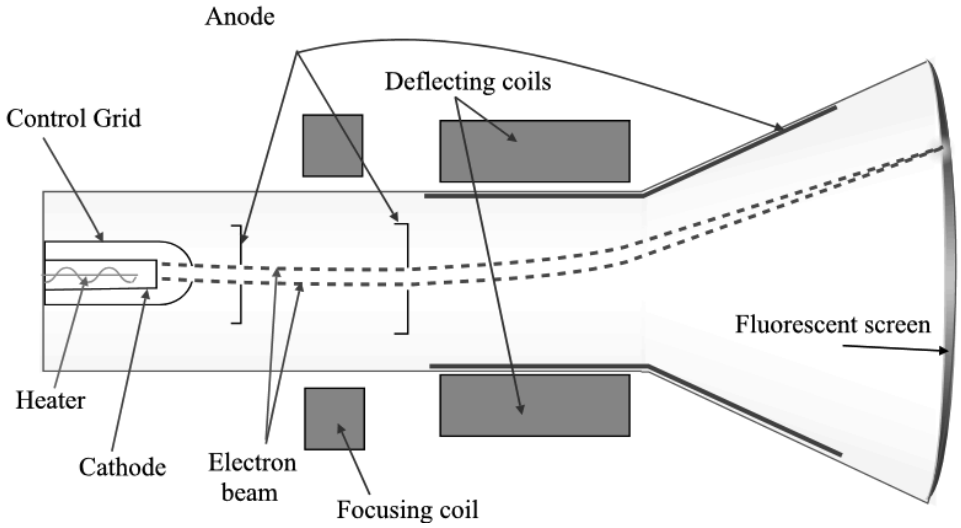

Figure 1.1. A cathode ray tube display [2].

depth is set by the maximum vertical or horizontal distance the electrons need travel, plus the depth of the electron gun. Since the depth is related to the display width and height, very large displays would necessarily have a massive total volume and are thus not practical. Ever since the popularization of the CRT, there has been a search for a display technology which is flat, and does not have the same constraint on total volume.

Both plasma display panels and liquid crystal displays have been investigated for over 20 years as flat replacements to a CRT. Recently they have left the research lab and entered mainstream consumer electronics, selling approximately $7.7 billion and $69.8 billion respectively in 2006 [3]. A number of new technologies remain over the horizon, including organic light-emitting diode displays, field-emission displays, and electrophoretic "e-paper" displays.

Looking further into the future, one can imagine a world where information display has become ubiquitous. Displays may be found not just in computer monitors and televisions, but replacing billboards, covering walls, and appearing on consumer products and even clothing. These applications require the displays to not only be flat, but extremely inexpensive, flexible, and self-contained. Flexibility is desirable not just because of the

new applications it may enable but because manufacturing on a flexible plastic substrate can be much less expensive than manufacturing on a glass substrate, thanks to roll-to-roll processing technology. A self-contained display, with no parts external to the display panel itself, is desirable to minimize costs and total unit size. For instance, even if a display can be built and integrated into a piece of clothing, it loses its usefulness if it requires bulky external control electronics.

Realizing these goals requires two directions of improvement in process technology. First, the display process must be modified such that it includes transistors capable of data processing on the panel itself. Second, the process for fabricating the display, along with the data-processing devices, must not damage the flexible substrate it is created on. This imposes a temperature limit on the device fabrication. The following section will review the requirements on the device performance, and the technologies which have been proposed to achieve that performance.

1.1.2 Liquid Crystal Display Technology

Presently, the leading flat panel display technology is the active matrix liquid crystal display (AM-LCD), comprising approximately 84% of the total flat panel display market [3]. AM-LCDs are found in televisions, desktop and laptop computer displays, cell phones, handheld electronics, and many more devices. Each pixel of an AM-LCD consists of a light valve, using a liquid crystal to modulate the pixel transmittance; a color filter, to select the pixel color; and a thin film transistor circuit, to apply the correct electric field to the liquid crystal.

A cross-section of a liquid crystal light valve is shown in Fig. 1.2 [4]. The liquid-crystal layer and two orthogonal polarizing filters transmit or block light depending on the potential applied to electrodes in front of and behind the liquid crystal. With no potential applied, the liquid crystal naturally twists, acting as a waveguide for the light and allowing it to pass through both polarizers. Application of a vertical electric field through the liquid crystal causes it to untwist, stopping light from passing through both filters. In front of the liquid

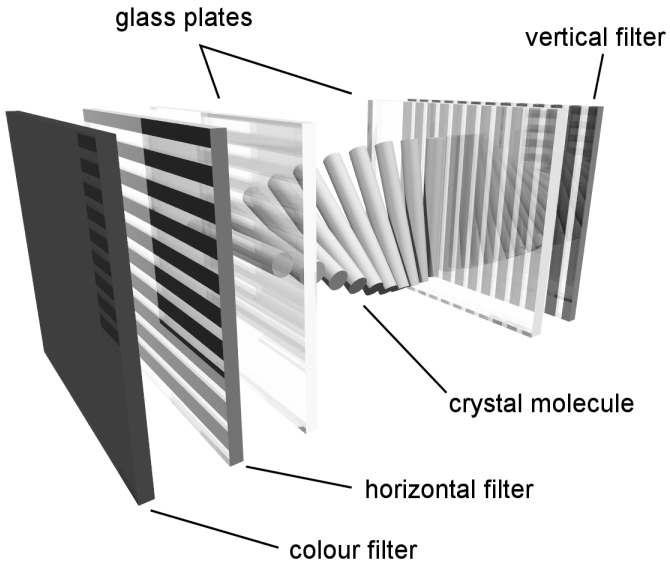

Figure 1.2. A liquid crystal light modulator [4].

crystal sits a color filter, allowing only one color of light to be transmitted by each pixel. Formation of three differently colored sub-pixels allows three colors of light to be modulated independently.

The AM-LCD pixel is shown in Fig. 1.3 from an electrical circuit point of view. Metal lines for each row and column are drawn along the display, with a thin-film transistor (TFT) at each intersection. Typically, the TFT gates are connected to the row lines, such that every TFT in a given row is turned on simultaneously. The column lines are connected to the TFT source, and the liquid crystal to the TFT drain, such that when the TFT is turned on, the voltage on the column line is passed to the liquid crystal capacitance. One row is enabled at a time, and data are sent to that entire row by the column lines. The row is disabled, the data on the column lines are changed, and the next row is enabled, allowing the entire display to be drawn row by row. An extra storage capacitor, C_S is used to increase the pixel capacitance to reduce the voltage change due to TFT leakage during the scan time, when the other rows are sequentially enabled. Without the TFT, it would be impossible to fabricate a large high-contrast display while still controlling the display as a matrix [5].

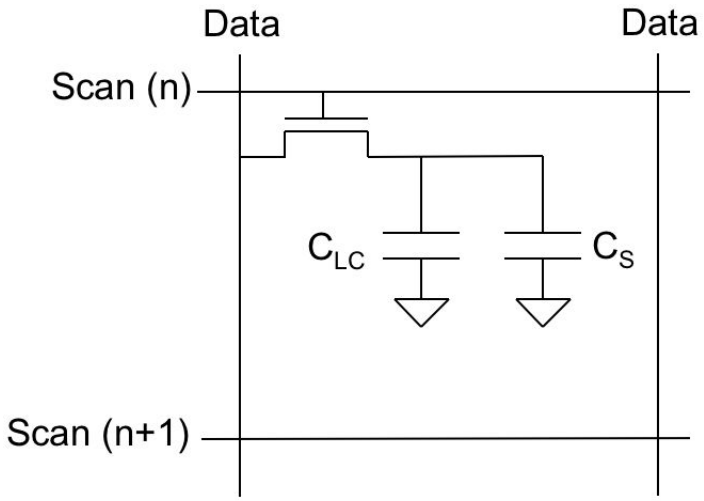

Figure 1.3. Circuit schematic of an LCD active matrix backplane.

Performance requirements for the active-matrix devices in each pixel are very different from the requirements on the data processing devices we hope to add. Active-matrix devices act as pass transistors, may be only of one type (NMOS or PMOS), and have relatively low performance requirements, as the display refresh rate is slow on an electrical time scale. In contrast, data processing applications require complementary devices with fast settling time, to accomplish low-power logical operations at the high data rate coming into the panel. Current AM-LCD panels have highly optimized and well-understood pixel transistors; however, much higher performing devices need to be engineered in order to add logical functionality to the panel.

1.1.3 Thin-Film Transistor Performance Requirements

In order to estimate the relative transistor performance requirements, approximate values of the required mobility can be found for the two types of device, assuming a display format and drive voltage. A color VGA display has 1024 columns $\times$ 3 colors $\times$ 768 rows, or 2,359,296 total pixels. At a 60 Hz refresh rate, the time to refresh a full frame is $\frac{1}{60}$ seconds, or 16.7 ms, and the time to refresh a single line is $\frac{1}{60} \times \frac{1}{768}$ seconds, or 21.7 μs.

Pixel access TFTs are required to settle to their final voltage in the time available for refreshing one line of the display, 21.7 μs. A rough approximation of the settling time is simply the time constant of the RC circuit formed by the liquid crystal capacitance and the TFT, used as a pass transistor. The time constant

$$T_{\mathrm{RC}} = R_{\mathrm{pass}} \cdot (C_{\mathrm{LC}} + C_{\mathrm{S}}), \tag{1.1}$$

with

$$R_{\mathrm{pass}} = \frac{1}{\mu C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{T}})} \tag{1.2}$$

[6]. Using typical values for liquid crystal capacitance

$$C_{\mathrm{LC}} + C_{\mathrm{S}} = 5\,\mathrm{pF}$$

and for transistor and drive parameters

$$t_{ox} = 50\,\mathrm{nm} \quad V_{\mathrm{T}} = 1\,\mathrm{V} \quad V_{\mathrm{GS}} = 5\,\mathrm{V}$$

we find

$$\mu \frac{W}{L} = 0.83\,\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}. \tag{1.3}$$

To get an estimate of the required clock rate for the logic devices, we assume that they are being used in a shift register which has to store an entire frame of data during the time the previous frame of data is sent to the display. Thus, they must be able to shift 2,359,396 times in 16.7 ms, or with a total clock period of 7 ns. The rising and falling edge times should be less than half the clock period, or 3.5 ns. An estimate of the propagation time of a logic gate is

$$T_{\mathrm{P}} = 0.5 \frac{C_{\mathrm{L}} V_{\mathrm{DD}}}{I_{\mathrm{D}}} \tag{1.4}$$

[6]. Assuming the n-type to p-type mobility ratio is 3 and the devices are appropriately sized:

$$\frac{\mu_{\mathrm{N}}}{\mu_{\mathrm{P}}} = \frac{W_{\mathrm{P}}}{W_{\mathrm{N}}} = 3, \tag{1.5}$$

the load capacitance is

$$C_{\mathrm{L}} = 4 W_{\mathrm{N}} L C_{\mathrm{ox}}. \tag{1.6}$$

So, the propagation time is

$$T_{\mathrm{P}} = 0.5 \frac{4L^2}{\mu_{\mathrm{N}}(V_{\mathrm{GS}} - V_{\mathrm{T}} - \frac{V_{\mathrm{DS}}}{2})}. \tag{1.7}$$

Plugging in typical values

$$L = 3\,\mu\mathrm{m} \quad V_{\mathrm{DD}} = 5\,\mathrm{V} \quad V_{\mathrm{T}} = 1\,\mathrm{V}$$

we can find a value for mobility

$$\mu_{\mathrm{N}} = 34.2\,\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}. \tag{1.8}$$

From these estimates, we learn that in order to design conservatively, our pixel TFT should have a mobility on the order of 0.5 $\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$ - 1 $\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$ with a $\frac{W}{L}$ ratio considerably greater than 1, and the logic TFT should have a mobility on the order of 50 $\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$ - 100 $\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$. It is therefore clear that a technology designed to be optimal for the pixel TFTs will not necessarily be usable for the logic TFTs.

1.2 Thin-Film Transistor Fabrication Technologies

Conventional silicon MOSFETs are made from single crystal silicon, engineered to have high purity and very few defects, thereby attaining very high performance. Single crystal devices would easily satisfy the performance requirements for all devices on a AM-LCD panel; however, it is not practical to use them on a display panel. It is not economical to bond a silicon wafer to a panel and etch away the unused areas due to the low density of devices compared with more conventional uses of the silicon wafer. Fabrication of devices at high density on a wafer and transferring them individually to the display panel is also too expensive, due to the number of devices which would need to be placed with high precision over the large panel. The most practical method to build semiconductor devices over the entire area of the panel is to use thin-film deposition methods to coat the panel and then etch away the unused areas. There is no known method to form a thin-film semiconductor on an amorphous substrate with performance comparable to single-crystal material; however, performance can be made acceptable.

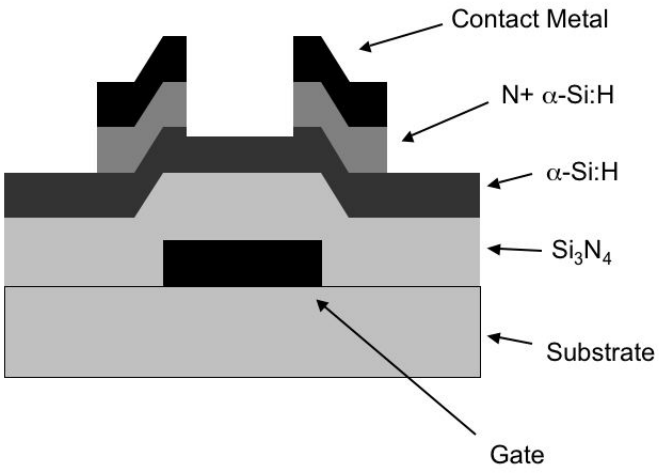

Figure 1.4. Cross-section of a bottom-gated α-Si:H thin-film transistor.

Many different thin film materials systems have been investigated for use in a display backplane. The first attempts commonly used cadmium selenide, due to its ease in forming a good quality semiconducting thin film through vacuum evaporation. Presently, hydrogenated amorphous silicon is used in the vast majority of LCD backplanes, while polycrystalline silicon is used in a smaller number.

1.2.1 Amorphous Silicon

Amorphous silicon has no long-range order, causing many silicon atoms to not be able to form the desired four bonds. When a silicon atom is missing a bond, it appears electrically in the film as a localized trap state, located between the conduction band edge and about 0.2 eV below [7]. Amorphous silicon has a very large number of these defects, and hence is a very poor semiconductor. The electrical effect of these defects can be reduced somewhat by the inclusion of large amounts of hydrogen in the silicon film, typically on the order of 10-15 atomic percent.

The process used to fabricate hydrogenated amorphous silicon (α-Si:H) TFTs for LCD backplanes uses a bottom-gated structure with a metal gate, a silicon nitride gate dielectric,

and an α-Si:H semiconducting layer, as shown in Fig. 1.4. Deposition of the gate dielectric and semiconducting layers is performed by plasma-enhanced chemical vapor deposition (PECVD), typically at 350 °C during dielectric deposition and 250 °C during semiconductor deposition. A higher temperature is desirable for the dielectric deposition in order to encourage growth of stoichiometric Si_3N_4, while a lower temperature is desirable during α-Si:H deposition to control diffusion of hydrogen out of the film as it is forming.

Carrier transport through an amorphous silicon layer is highly inefficient. The primary mode of transport is thermally-assisted hopping between localized trap states [7], leading to a very low mobility as compared with crystalline silicon, typically on the order of 1 $\frac{cm^2}{V \cdot s}$ for well-engineered devices [8]. Performance at this level is acceptable for pixel TFTs, and these devices have a number of other desirable properties. When properly hydrogenated, defect density is low, leading to good turn-on characteristics, with subthreshold slope under 1 V/decade and threshold voltage under 1 V. Good quality large area PECVD tools have been developed to deposit extremely uniform α-Si:H and Si_3N_4 films on the glass substrate, leading to extremely uniform devices [9].

The most significant shortcoming of α-Si:H TFTs, aside from low mobility, is their reliability. The randomly arranged silicon network has many weak Si−Si bonds, which are easly broken under the influence of vertical field. Charge can also easily be trapped at the poor quality α-Si:H$-Si_3N_4$ interface. Both of these lead to shifts in the device threshold voltage over time [10]. Hole mobility in α-Si:H devices is also extremely low, causing PMOS devices to be of too poor quality to be useful and preventing fabrication of CMOS circuits. Overall, the quality of NMOS α-Si:H devices is good enough that they have become ubiquitous as pixel TFTs in AM-LCD displays; however, they are not usable as logic devices, so another solution must be found.

1.2.2 Polycrystalline Silicon

Polycrystalline silicon (poly-Si) is a form of silicon which consists of many small crystalline grains oriented randomly with respect to one another. Within each grain, the

crystalline quality can be high, possessing only a small number of defects. However, there are large concentrations of defects at the boundaries between grains. Depending on the fabrication process, the size of the crystalline grains can be as small as tens of nanometers or as large as several micrometers. Large grains are preferable, as the average trap density is low and the distance between high trap density regions is high. If the grains can be made larger than the transistor channel length, device performance can start to approach that of single crystal silicon.

There are many different methods to fabricate poly-Si. A silicon thin film can be deposited in a polycrystalline state, or it can be deposited as an amorphous film and further treated to transform it into polycrystalline material. The latter tends to be preferable despite the extra process complexity, as larger grain size is typically achieved. Silicon deposition can be performed by low-pressure chemical vapor deposition (LPCVD), PECVD, or sputter deposition, each process operating in a different temperature range. LPCVD is performed in the range of 530 °C - 620 °C, with temperatures above approximately 580 °C producing polycrystalline films, and lower temperature depositions producing amorphous films. PECVD processes are typically run between 250 °C and 400 °C, though they will still function at considerably lower temperatures. Sputter deposition can be run as low as room temperature or as high as is safe for the tool. Quality of sputter deposited silicon films varies with temperature much less than LPCVD or PECVD, as it is a physical deposition process rather than a chemical one. Materials quality only begins to change once the deposition temperature approaches its melting point.

Once a silicon thin film has been deposited, crystallization can be performed either by annealing in a furnace above 600 °C or by laser annealing. Laser annealing can produce large-grained polycrystalline silicon and is compatible with low-temperature substrates, despite raising the temperature of silicon thin film above its melting point of 1414 °C. Excimer laser pulses are extremely short, approximately 30 ns, and the entire heating and cooling cycle associated with one pulse takes under 1 ms [11]. If an appropriate barrier layer

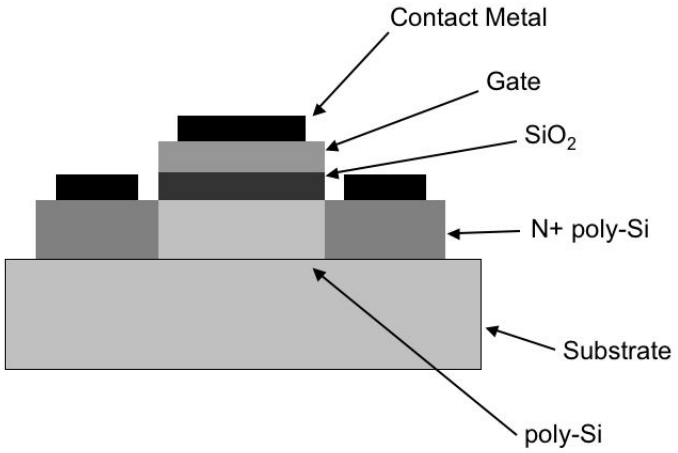

Figure 1.5. Cross-section of a top-gated polycrystalline silicon thin-film transistor.

is used below the silicon film, the molten silicon will cool back to room temperature before enough heat can diffuse into the substrate layer to damage it.

Poly-Si mobility largely depends on the grain size and therefore on the method used for crystallization. Silicon deposited by LPCVD in polycrystalline form can have electron mobility as high as about $10\,\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$, and furnace crystallized poly-Si typically has electron mobility of about $30\,\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$ [12]. Excimer laser crystallized silicon can have much larger grains than furnace crystallized silicon and can typically achieve electron mobility as high as $1\,00 - 200\,\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$ [13]. Using specialized laser annealing techniques such as sequential lateral solidification (SLS) or grain engineering, electron mobility can be raised even as high as $3\,00 - 500\,\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$ [14, 15], approaching that of single-crystal silicon. Electron mobilities this high, combined with a comparable hole mobility in polysilicon, allows fabrication of CMOS circuits capable of high-speed data processing.

After a polycrystalline silicon thin film has been formed, it is typically fabricated into top-gate planar transistors. These devices have a process flow very similar to SOI MOSFETs, and can approach their performance if the silicon thin film is of very high quality. The cross section of a typical poly-Si TFT is shown in Fig. 1.5.

1.3 Challenges for Poly-Si TFTs on Plastic Substrates

As described in section 1.1.1, in order to achieve our ultimate goal of ubiquitous displays, we need high-performance data processing devices produced on inexpensive flexible substrates. The initial goal of demonstrating high-performance devices on a flexible substrate has been accomplished by several research groups [16, 17, 18]. However, challenges still exist that prevent their widespread adoption.

1.3.1 Process Thermal Budget Limitations

The initial challenge that needs to be addressed when designing a thin film transistor process is the thermal budget of the substrate material. Modern AM-LCD panels use a glass substrate that has a strain point of 666 °C [19], and thus can be safely processed up to approximately 600 °C. This limit is entirely compatible with α-Si:H TFTs, which reach a maximum temperature of 450 °C during processing. Higher temperature annealing would be detrimental to device performance, as hydrogen would be driven from the layers, depassivating defects.

Typical processes for poly-Si deposition and crystallization all take place under or at 600 °C, so that they are compatible with glass. Gate oxide formation suffers for the temperature limitation, however. The highest quality $Si-SiO_2$ interface is formed by high-temperature oxidation, the process used in conventional MOSFETs. Thermal growth of SiO_2 is very slow at our limit of 600 °C, so a deposition process must be used, typically LPCVD or PECVD. Device performance suffers as a result of the poorer interface, however, good quality devices can be fabricated.

Moving from a glass substrate to a flexible one lowers the available thermal budget considerably. Many high-temperature flexible plastics have been engineered, but their cost increases commensurately with their temperature compatibility. For instance, polyimide materials, which have a peak processing temperature in the range of 250 °C - 400 °C, have a typical bulk cost of 150 $\frac{\dot{C}}{in^3}$. This is compared with polyethersulfone (PES), which costs

approximately 20 $\frac{¢}{in^3}$, but can only safely reach 200 °C. At the low end of the cost spectrum is polyethylene terepthalate (PET), costing only 4 $\frac{¢}{in^3}$ [20], but with maximum processing temperature limited to only 150 °C. PET is widely used in consumer products, in such applications as soda bottles, textiles (known under the trade name Dacron), and as a thin-film coating (known as Mylar). Its low cost enables it to achieve the kind of ubiquity we are seeking for flexible electronics, so we must develop a device process which is compatible with its thermal limit.

Adapting a process to a lower thermal limit can be a matter of running existing processes at a lower temperature and learning to compensate for the poor quality materials which result, or it can require development of entirely new processes. For instance, PECVD processes will typically deposit material when run anywhere between room temperature and 400 °C. It is therefore possible that adapting an α-Si:H process to a plastic substrate simply consists of lowering the temperature of the reactor and evaluating whether materials performance is sufficient for the application. This work was reported by Sazonov et al. [21], where it was established that functional devices could be fabricated at temperatures as low as 75 °C with only moderate loss in performance compared with conventionally processed α-Si:H TFTs.

Many of the fabrication steps necessary for polycrystalline silicon TFTs can be adapted with little modification from a higher-temperature process. Examining the process options for forming polysilicon described in section 1.2.2, the techniques available below 150 °C include sputter deposition, adaptation of a PECVD process to low temperatures, and laser crystallization. Use of a PECVD process in laser crystallized devices has been demonstrated [17], but adds unnecessary complexity. PECVD silicon films contain large quantities of hydrogen, which will rapidly diffuse out at high temperatures. Laser processing causes the silicon film to rise in temperature so rapidly that severe damage is done as the hydrogen evolves from the film. If a PECVD silicon film is to be used in a laser crystallized polysilicon process, the hydrogen must first be carefully removed through a very low energy laser

treatment [22]. Sputtered silicon contains no hydrogen, thereby avoiding an extra processing step.

Laser crystallized sputtered silicon is usable on a PET substrate without substantial modification, but not all process steps in a polysilicon TFT are so easily adaptable. The gate oxide formation process for conventional MOSFETs was not usable for glass-compatible TFTs and will need to be further modified for plastic compatible TFTs. High-density PECVD has been used to deposit good quality gate oxide at 150 °C [18]. However, high-density PECVD is not easily adaptable to large area substrates, the largest reported deposition system with good uniformity is 30 cm diameter [23]. Additionally, glass-compatible polysilicon TFTs typically use a plasma hydrogenation process to passivate defects after the crystallization process is completed, improving performance in a similar way to the hydrogenation in α-Si:H. This process requires annealing at 350 °C [24], and is not adaptable to plastic-compatible processes.

1.3.2 Device Uniformity

The main performance drawback to the use of polycrystalline silicon (poly-Si), and in particular laser crystallized poly-Si, is the large variation between devices. Whereas amorphous silicon has a uniformly high density of defects throughout, poly-Si has both low defect concentration regions (grains) and high defect concentration regions (grain boundaries). Good quality material will have large grains; only a small number of grain boundaries will appear within each device. Fluctuations in the exact number and location of grain boundaries in a given device will cause large variations in the total number of defects within the device, leading to large performance variations between devices.

Crystallization using a laser adds an additional source of performance variation on top of the variation inherent to polysilicon. Laser annealing of silicon is typically done with a pulsed excimer laser, due to its high power density. Each pulse is only large enough to cover a small fraction of the total area of the panel, hence the laser beam must be scanned

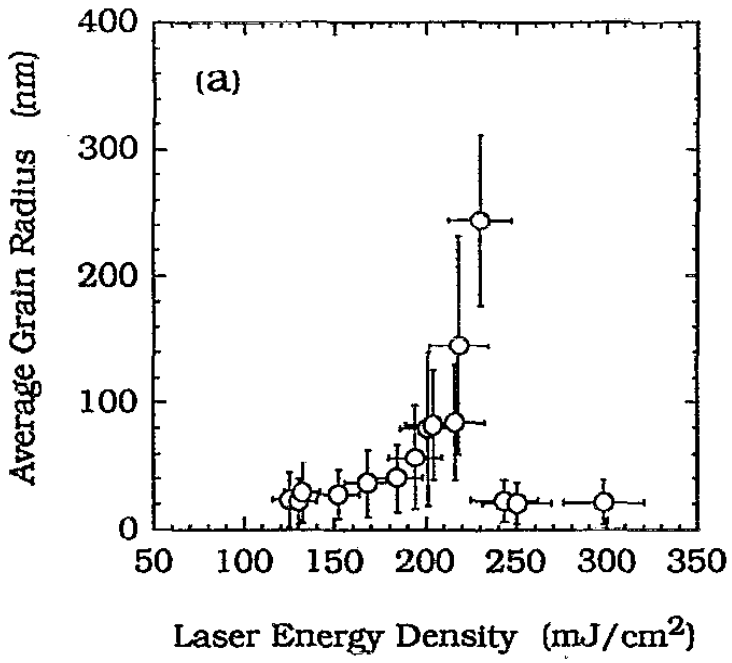

Figure 1.6. Measured polysilicon grain size vs. excimer laser annealing energy [25].

across the panel to anneal the entire film. There are fluctuations in the energy delivered in each pulse, leading to variations in the grain size of the crystallized film.

The problem of pulse energy variation is enhanced by the silicon crystal growth mechanisms during the laser pulse. Looking at Fig. 1.6 [25], it is seen that the peak of grain size vs. laser annealing fluence is steep and narrow. The laser pulse is absorbed into the surface of the silicon film, melting the silicon to a depth determined by the fluence of the pulse. As the molten silicon cools, grains nucleate from the unmelted layer below, yielding a grain size roughly corresponding to the melt depth. The peak grain size arises when nearly all of the film is melted and only a few nucleation sites remain. Once the film is completely melted and no nucleation sites remain, the molten silicon is able to supercool, leading to spontaneous nucleation throughout the film and growth of very small grains. Therefore, when the process is designed to produce films with the largest possible grain size, fluctuations in the laser fluence will lead to the highest degree of grain size nonuniformity [25].

In a higher-temperature polysilicon TFT process, device uniformity can be addressed through the use of hydrogen passivation. Passivation reduces the electrical effect of crystalline defects by completing broken silicon bonds. This has the dual effect of improving performance and uniformity, as defects are responsible for degrading both. It would be highly desirable if a suitable plastic-compatible replacement for hydrogen passivation could be found.

1.3.3 Device Reliability

Good quality high-temperature processed poly-Si often has poor reliability, exhibiting shifts in threshold voltage over time. After fabrication, broken Si bonds are passivated with hydrogen, forming Si−H bonds. These bonds are weak compared with Si−Si bonds, however. When a hydrogenated thin film silicon device is subjected to heat or to electrical stress, Si−H bonds are broken and the defect is depassivated. Devices degrade in this way slowly over time to their original, unpassivated, condition. Performance shift over time is highly undesirable for devices to be used in digital circuits.

Hydrogen passivation is not usable in plastic-compatible devices due to temperature incompatibility, but finding a replacement is essential to the feasibility of flexible electronics. If a passivation technique could be found which has inherently better reliability than hydrogen passivation, it would be very important for the future of plastic-compatible devices.

1.4 Thesis Organization

This dissertation addresses each of these remaining challenges to plastic compatible poly-Si thin-film transistor formation. The focus of the research has been on a passivation technique which is both compatible with low temperature flexible substrates and has better reliability than hydrogen passivation. This is accomplished by implanting a passivating species into the α-Si thin film prior to excimer laser annealing. During laser processing this

impurity reacts with silicon defects, accomplishing the desired effect of electrical passivation. This technique has been demonstrated with N, O, and F impurities, each of which forms a stronger bond to Si than H, thereby improving reliabiity. The theory, experimental design, and measured data for this process is detailed in Chapter 2.

In order to demonstrate the effectiveness of this passivation technique for ultra low temperature devices, a baseline plastic-compatible process needed to be established. Chapter 3 details the fabrication process and development done in order to realize plastic-compatible devices. A reactively sputtered SiO_2 process was used to form a gate dielectric in a process compatible with large-area substrates. The Si thin film was first treated with O_2 under UV light emission to achieve an $Si-SiO_2$ interface with a minimal number of defects. After SiO_2 film deposition, a laser annealing step was used to heat the $Si-SiO_2$ interface, further removing defects. Efficacy of the implant passivation technique was measured in devices fabricated with this process.

Chapter 4 demonstrates laser annealing with a copper vapor laser, as a possible alternative to excimer laser annealing. Copper vapor lasers are widely used in laser machining and have better pulse-pulse nonuniformity and lower cost-of-ownership than excimer lasers. Here the feasibility of their use for formation of polycrystalline silicon is established, and performance and uniformity characteristics are measured.

Chapter 5 summarizes the contributions of this work and provides suggestions for further studies in plastic-compatible device fabrication and defect passivation.

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Chapter 2

Thin Film Transistor Passivation by Ion Implantation and Excimer Laser Annealing

2.1 Introduction

Formation of a silicon film with a minimum of defect states is essential to fabrication of high-performance polycrystalline silicon thin-film transistors. Defects arising from broken bonds at grain boundaries and from lattice imperfections within silicon grains lead to traps within the silicon bandgap, both at deep and shallow levels [1]. Trap states cause an increase in the device threshold voltage, subthreshold slope, and leakage current, and a reduction in mobility [2, 3, 4]. Additionally, nonuniformities in laser processing lead to nonuniformities in trap formation, and thus to an increase in the variation between devices [5].

Two approaches are taken to reduce the number of trap states in the polycrystalline silicon film. The silicon film is first annealed at high temperature, either in a furnace or with a laser, in order to cause large, high-quality grains to form. Extensive studies have been performed to find processes which grow the largest possible grains, and therefore have

the smallest defect density [6, 7]. Once the silicon film has been formed, a treatment is performed in order to render as many as possible of the defect states electrically inactive, called defect passivation. Defects are predominantly silicon atoms with one or more incomplete bonds, and thus can be passivated by adding atoms to complete the broken bonds. After a passivation treatment, lattice defects are electrically neutral and do not affect the electrostatics of the device.

2.2 Thin Film Transistor Passivation Techniques

There are several different techniques which have been attempted for defect passivation, but the one which is by far the most common is hydrogen annealing. Furnace annealing in an atmosphere of hydrogen diluted in an inert gas is a common step in the fabrication of conventional MOSFETs, used to reduce defects at SiO_2−Si and metal−Si interfaces [8]. The density of defects in a polycrystalline silicon thin film is very high compared with that at an interface in a conventional device, so the process has been adapted to use an anneal in hydrogen plasma to increase the rate of defect passivation.

A hydrogen plasma annealing process is performed in a plasma reactor similar to one which could be used for plasma enhanced chemical vapor deposition (PECVD) or plasma etching. A schematic drawing is shown in Fig. 2.1 [9]. The wafer is loaded on a heated chuck and the chamber is filled with hydrogen gas, which is then ionized with RF energy. Ionized hydrogen diffuses into the silicon film and reacts with dangling bonds, accomplishing the desired passivation. The efficacy of the hydrogen plasma annealing process depends on the temperature and time of passivation, as well as the gas mixture and type of plasma reactor used, and has undergone extensive characterization with regard to each of these variables [10, 11, 12, 13, 14].

Data for performance of a hydrogen passivation process vs. processing time and processing temperature are shown in Fig. 2.2 [11] and Fig. 2.3 [10], respectively. Fig. 2.2 shows the evolution of threshold voltage and mobility vs. time, and Fig. 2.3 shows the

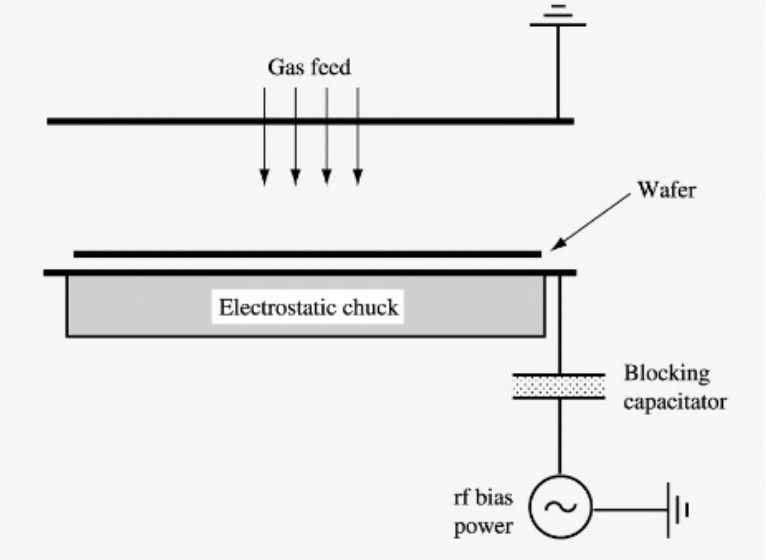

Figure 2.1. Schematic drawing of a parallel-plate plasma reactor [9].

reduction of unpaired spins in Si vs. temperature as measured by electron spin resonance. From these plots we can conclude that hydrogen plasma annealing is very effective for passivation of defects but only when the anneal is performed for many hours at temperatures near 350 °C. This is acceptable for a glass-compatible thin-film transistor process; however, is not usable in a plastic compatible process. Even high-temperature plastics such as polyimide will undergo significant shrinkage after many hours at elevated temperature, and low-cost plastics will burn at temperatures well below what is necessary for hydrogenation.

An initial attempt to lower the time and temperature necessary for adequate passivation was undergone by Sameshima [15], using H_2O vapor annealing. The anneals were conducted at very high pressure, up to 4×10^6 Pa, in order to speed diffusion of reactive species into the silicon film. The use of H_2O additionally enhances passivation by introducing both reactive oxygen atoms and hydrogen atoms to terminate broken silicon bonds. Measured data from Si films treated with the high-pressure H_2O anneal at different temperatures is shown in Fig. 2.4. Defect reduction is measured as the ratio of photocurrent to dark current, as defects prevent low off-current or high on-current. Improvement by five orders of magnitude of on/off ratio is seen after annealing for 1 hour at 190 °C, at approximately 1.5×10^6 Pa. However, this process is still impractical for plastic compatible TFT fabrication. A low-cost

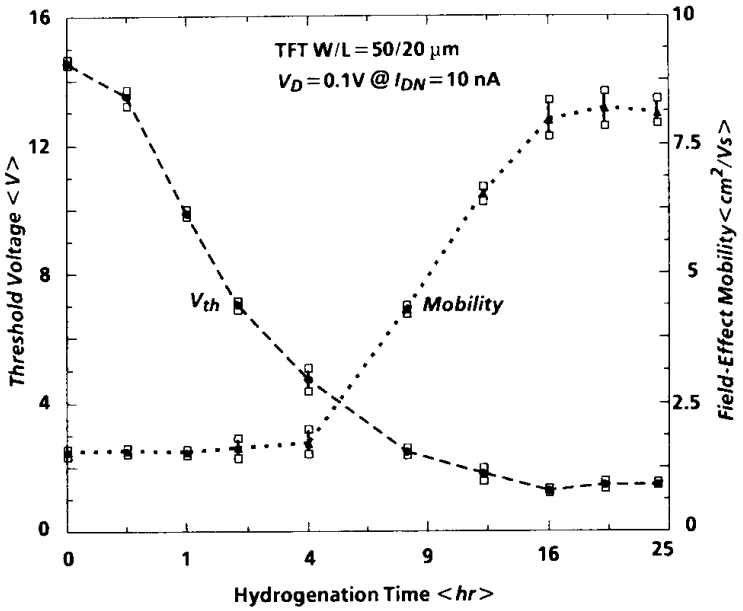

Figure 2.2. Threshold voltage and field-effect mobility as functions of hydrogen plasma annealing time [11].

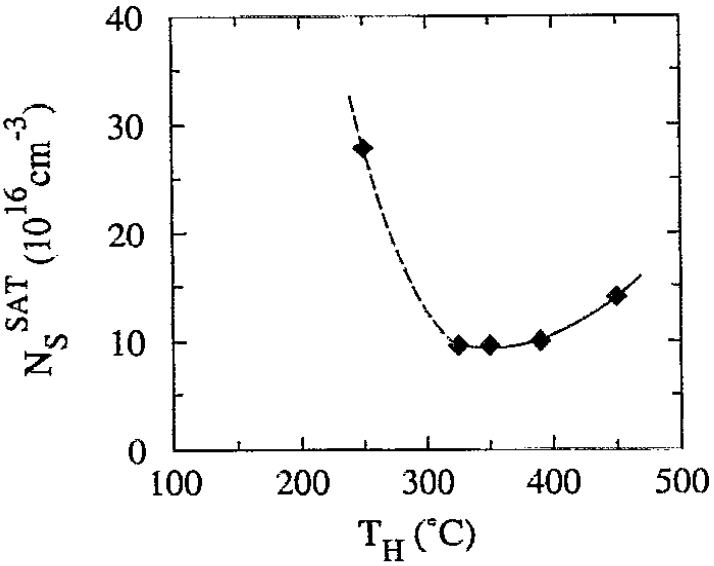

Figure 2.3. Unpaired spins in polycrystalline silicon after hydrogen plasma annealing at different temperatures [10].

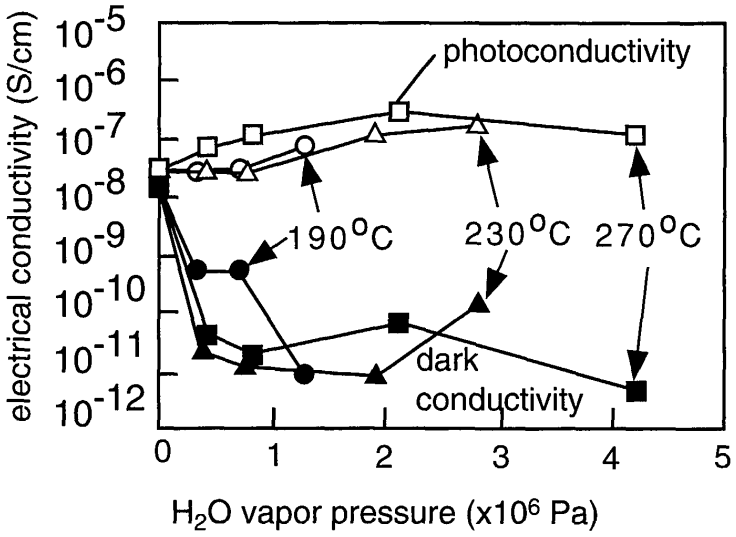

Figure 2.4. Dark conductivity and photoconductivity in polycrystalline silicon films after high-pressure H_2O treatment [15].

plastic substrate will likely undergo severe damage if subjected to the thermal budget and high pressure necessary for this anneal, even though it is considerably lower thermal budget than a conventional plasma hydrogenation.

There has recently been research into defect passivation using fluorine [16, 17, 18, 19]. Fluorine is introduced into silicon either through ion-implantation or by solid-source diffusion from a fluorinated silicon dioxide layer. It cannot be diffused into a silicon film from an ambient gas due to its volatility. The processes used to introduce and activate fluorine in silicon require a high temperature anneal to activate or diffuse the fluorine impurities; passivation with fluorine in a plastic-compatible process has not yet been shown. Fig 2.5 [19] compares device data from thin-film transistors passivated with fluorine and with no passivation. The devices were fabricated in a glass-compatible process, using a long 600 °C anneal to crystallize the silicon and activate the implanted fluorine. Improvement in mobility and subthreshold slope of a factor of 2 is seen in the fluorine implanted devices as compared with the unpassivated devices.

Finally, the use of nitrogen as a passivating species has also been investigated. Performance gains have been seen in passivation processes using a NH_3, N_2O, or N_2 plasma,

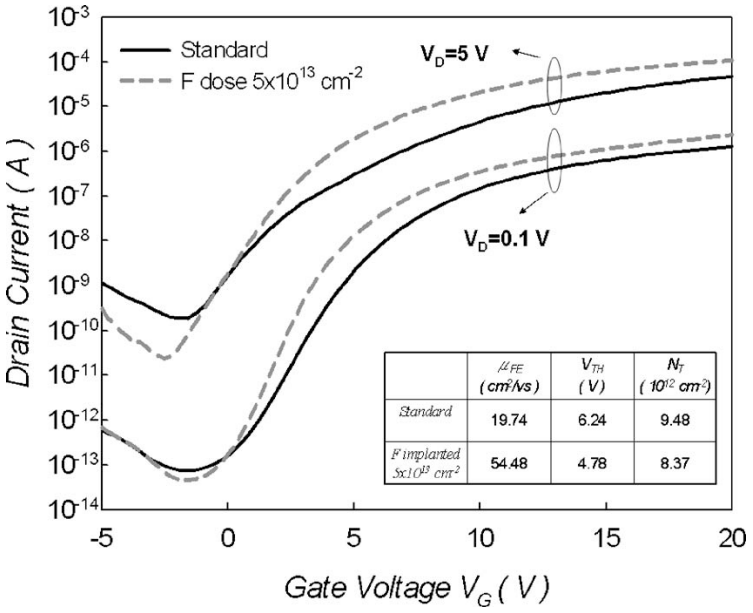

Figure 2.5. Transfer curves and extracted parameters of polysilicon TFTs with and without fluorine passivation [19].

similar to hydrogen plasma annealing. These processes are typically conducted at 250 °C [20] or 300 °C [21], and show comparable performance to hydrogen annealing, in some cases with improved reliability [22]. Implanting nitrogen after furnace crystallization and annealing at 850 °C has also been shown to achieve modest improvements in performance and reliability [23]. These processes are not plastic-compatible, nor in the latter case glass-compatible, but they show feasibility of passivation with nitrogen, and its compatibility in a high-performance polycrystalline silicon TFT.

2.3 Motivation

In order to achieve high performance with good uniformity in a plastic compatible polycrystalline silicon thin film transistor process, a plastic compatible passivation technique must be developed. The difficulty lies in the fact that forming bonds between silicon and a passivating element requires more thermal energy than an inexpensive flexible substrate can withstand. However, silicon crystallization and activation of dopants in the source and

drain regions in a plastic compatible process face the same problem, for which a solution has already been found. Both of these steps are performed using an excimer laser to locally heat a silicon thin-film without damaging the substrate below. If these laser processing techniques can be adapted to activate a passivating impurity, a plastic compatible passivation technique can be found.

Laser processing can take a lot of time, however. Fully melting a silicon thin film with an excimer laser takes an energy density of approximately $400\,\mathrm{mJ/cm^2}$, depending on the thickness and film quality of silicon used and on the wavelength and pulse width of the laser. The maximum pulse energy of a typical state of the art XeCl excimer laser is 1050 mJ, at a pulse repetition rate of 300 Hz [24]. A typical industrial laser crystallization process [25] shapes the beam into an $350\,\mu$m by 75 cm rectangle and scans it in $17.5\,\mu$m steps, resulting in a scan rate of 5.25 mm/s. Modern 8th generation display substrates measure 2.16 m by 2.46 m [26], and could be annealed with this process in three passes, in a total time of 23.42 minutes per panel. This is a long and costly time to spend processing each panel, so adding additional laser steps is highly undesirable. For this reason, rather than adding a step specifically for laser activation of passivating impurities, it is advantageous to attempt to combine passivation either with channel crystallization or source and drain activation. During excimer laser activation of source and drain dopants, laser light is reflected by the gate line, and the channel region under the gate is not heated. Therefore, passivation must be combined with the channel crystallization step. Laser crystallization is typically the first step performed after silicon channel film deposition, so the passivating impurities must either be added in-situ during film deposition, or in a separate step immediately after deposition.

One well-known difficulty with laser processing is its incompatibility with hydrogenated silicon [27]. The diffusivity of hydrogen in silicon at its melting point of 1414 °C is extremely high, approximately $5 \times 10^4\,\mu\mathrm{m^2/s}$ [28]. Even though the Si film is only molten for about 200 ns during a crystallization pulse [29], this leads to a diffusion length of 100 nm, twice the typical film thickness used in a polycrystalline silicon thin-film transistor process. All of the

hydrogen in the silicon film is therefore able to escape during a single laser pulse. Evolution of hydrogen from silicon during laser processing is so rapid that the silicon film is irreversibly damaged [30]. Giust and Sigmon studied TFT performance from laser-annealed sputtered silicon thin films with controlled amounts of hydrogen incorporated during the sputtering process [31]. The laser process was modified to be compatible with hydrogenated silicon films, starting with low-energy pulses and ramping the energy slowly. It was found that the maximum hydrogen content devices had the worst performance, and the minimum hydrogen content devices had the best performance. The predominant effect of adding hydrogen to a silicon film before crystallization is thus seen to be damage during laser processing, rather than any passivating effects.

We seek to passivate polycrystalline silicon TFTs by introducing a passivating impurity into the silicon film prior to laser crystallization. The impurity best known to passivate silicon TFTs, hydrogen, will not work for this process, as it will diffuse out of the silicon film during laser processing, causing damage along the way. Therefore, we have attempted this technique with other elements known to passivate defects in polycrystalline silicon TFTs, namely oxygen, fluorine, and nitrogen. These elements all have a much lower diffusion coefficient in silicon than hydrogen. At the melting point of silicon, nitrogen has a diffusivity of $1.2 \times 10^{-3}\,\mu\mathrm{m}^2/\mathrm{s}$, and oxygen has diffusivity of $3.6 \times 10^{-1}\,\mu\mathrm{m}^2/\mathrm{s}$ [28]. Diffusivity of fluorine in silicon has only been measured up to 700 °C, but extrapolating to 1414 °C for comparison yields a diffusivity of $2.7\,\mu\mathrm{m}^2/\mathrm{s}$ [32]. These are all at least 4 orders of magnitude lower than diffusivity of hydrogen in Si, leading to diffusion lengths below 1 nm. It is therefore reasonable to expect these impurities to stay in the silicon film during the laser annealing process, unlike hydrogen. Additionally, selenium has been shown to passivate surface states in metal−Si contacts, due to its ability to form a surface reconstruction on crystalline silicon with no broken bonds [33]. It is possible that similar effects will be seen on the silicon surfaces at grain boundaries, so passivation using selenium was attempted as well. For simplicity of experimentation and control over dose, the passivating impurities were introduced into the silicon film by ion implantation.

2.4 Process Flow

Self-aligned top-gate TFTs were fabricated on oxidized silicon wafer substrates as follows. A 1 μm thick layer of SiO_2 was deposited by LPCVD onto the Si wafer, followed by a 50 nm layer of Si deposited by DC sputtering at room temperature. Ion implantation of the passivation species (Se, N, O, or F) was then performed through a 45 nm capping SiO_2 layer deposited at 450 °C. The implant energy was chosen so that the projected range is at the interface between the capping oxide layer and the Si layer, and the implantation dose was chosen to place a dose of 1×10^{14} ions/cm^2 into the Si film. This dose corresponds to an impurity density of 2×10^{19} cm^{-3}, chosen to be approximately one order of magnitude higher than a typical density-of-states for fine-grain poly-Si [10], in order to encourage as complete passivation as possible.

After the capping oxide was removed in dilute HF, pulsed XeCl excimer laser annealing (three pulses at a fluence of 275 mJ/cm^2) was performed on the bare Si film, in air. This annealing fluence was chosen to be near the measured full melt threshold of 325 mJ/cm^2 in order to promote growth of large grains, but sufficiently below it to maintain good device to device uniformity. Following the ELA, some samples were given a 600 °C anneal in N_2 for 12 hours. The poly-Si films were patterned and dry etched to form TFT active regions, and a 50 nm gate SiO_2 layer was deposited by LPCVD at 450 °C.

The 80 nm Al gate layer was deposited by DC sputtering at 300 °C, patterned, and wet etched. SiO_2 gate-sidewall spacers 50 nm thick were then formed by LPCVD at 400 °C and anisotropic dry etching. Heavy n-type doping of the source and drain regions was accomplished with phosphorus ion implantation, at a dose of 1×10^{15} ions/cm^2 and energy of 34 keV. The source and drain implant was activated with a second ELA step, using three shots at 175 mJ/cm^2. This annealing fluence was the highest fluence that could be used without damaging the oxide layer covering the source and drain regions. Next, a 130 nm SiO_2 insulation layer was deposited by PECVD, and contact holes were patterned and dry etched. Finally, a 700 nm Al/2% Si layer was deposited by DC sputtering, patterned, and wet etched. The devices were then tested, sintered in N_2 for 2 hours at 350 °C, and retested.

Control devices were fabricated using the same process as described above, but without any passivation species implant. After initial testing, these devices were annealed in hydrogen plasma at 350 °C for 2 hours, in order to compare implant passivation to conventional hydrogen passivation.

2.5 Device Results

Measurements from devices measuring $W/L = 50\,\mu m/5\,\mu m$ are shown in the following figures. I_D vs. V_{GS} transfer characteristics were measured with $V_{DS} = 1\,V$. Table 2.1 shows extracted parameters for the F, O, and N implanted devices and the control devices. Devices labelled -HT received the 12 hour 600 °C anneal, and devices labelled -LT did not. Devices labelled -Ann received 350 °C post-metallization annealing, as described in section 2.4. I_{max} and I_{min} were measured as the maximum and minimum I_{DS} with $V_{DS} = 1\,V$ and $-15\,V \leq V_{GS} \leq 15\,V$. μ_{eff} was measured as the maximum value of $\frac{g_m^2}{2I_D C_{ox} \frac{W}{L}}$ with $V_{DS} = 5\,V$ and $-15\,V \leq V_{GS} \leq 15\,V$. Threshold voltage V_T was extracted as the voltage V_{GS} for which $I_{DS} = 20\,nA/\mu m$ of device width, with $V_{DS} = 1\,V$. The subthreshold slope was computed from the peak value of the slope of $\log I_{DS}$ with $V_{DS} = 1\,V$.

Figs. 2.6 and 2.7 show devices fabricated in the low-temperature process before post-metallization annealing. The devices which were implanted with Se show much worse performance than the unimplanted devices, seen in Fig. 2.6. Their behavior is consistent with the Se impurities sitting substitutionally in the Si lattice and acting as double donors. The heavy n-type doping that results adds a large number of conduction electrons to the silicon film without any gate bias, increasing the off-state current by four orders of magnitude. Doubly ionized Se impurities electronically scatter electrons travelling through the Si channel, lowering the effective device mobility. As the Se implanted devices show severely degraded performance compared with the other implant conditions, they were not further analyzed and are left out of the remaining figures for clarity.

A comparison of the remaining three implant conditions with the unimplanted devices

Table 2.1. Performance of 450 °C Processed Devices and 600 °C Processed Devices Before and After 350 °C Annealing

Device	I_{min} pA	I_{max} mA	μ_{eff} $cm^2/V{\cdot}s$	V_T V	S V/dec	ΔV_T V
N-LT	6.15	0.610	82.6	-1.367	0.616	
O-LT	23.1	0.443	55.1	-0.820	0.734	
F-LT	24.2	0.535	68.2	-1.566	0.657	
control-LT	26.1	0.317	33.3	0.104	1.120	
N-HT	6.08	0.644	72.7	-2.538	0.480	
O-HT	19.7	0.499	63.3	-1.857	0.561	
F-HT	36.2	0.452	54.9	-1.122	0.659	
control-HT	7.91	0.409	45.8	-1.396	0.720	
N-LT-Ann	2.56	0.607	113.9	-1.641	0.459	0.729
O-LT-Ann	3.11	0.450	77.1	-1.610	0.551	0.520
F-LT-Ann	6.63	0.530	89.3	-2.442	0.604	0.500
H-LT-Ann	15.0	0.448	54.6	-3.103	0.662	0.428
N-HT-Ann	1.67	0.646	116.9	-2.428	0.344	0.133
O-HT-Ann	1.11	0.518	98.0	-2.786	0.355	0.393
F-HT-Ann	1.23	0.468	85.2	-2.274	0.365	0.370
H-HT-Ann	0.835	0.421	70.5	-1.635	0.379	0.212

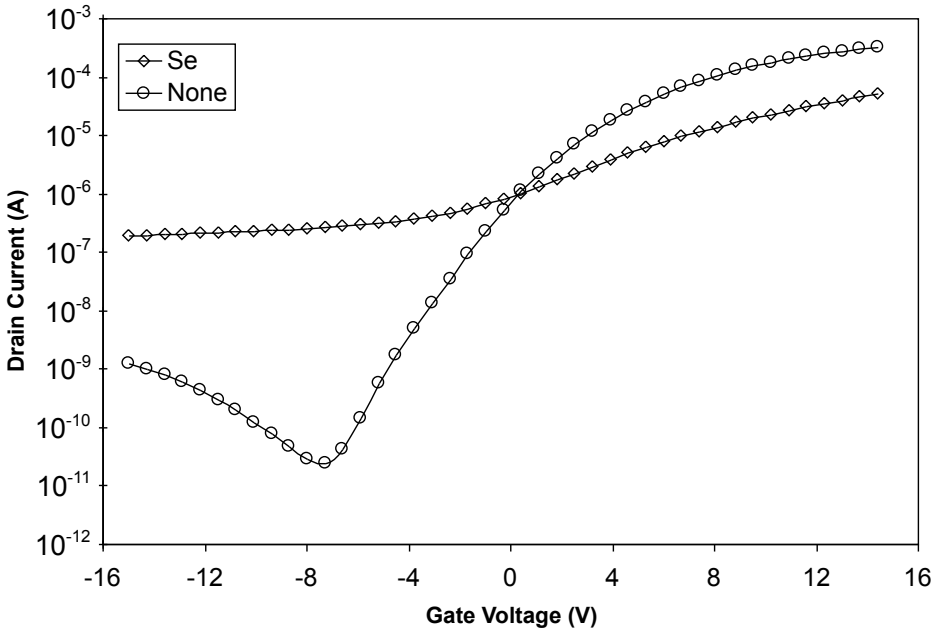

Figure 2.6. I_D vs. V_{GS} transfer curves for unimplanted TFTs vs. TFTs implanted with Se.

is seen in Fig. 2.7. It is seen that passivation has been successful for each of the three passivation species F, O, and N. Each shows significantly improved subthreshold slope and mobility compared with the unimplanted devices. Threshold voltages appear to have shifted in the negative direction, typically a sign of defect reduction; however, comparison of threshold voltages is difficult due to the large differences in subthreshold slope. Additionally, all devices measured show significantly negative threshold voltages. A likely explanation is gate dielectric contamination with positive charge from dirty processing equipment, shifting the flatband voltage in the negative direction.

Devices passivated with N are seen to have the highest mobility and steepest subthreshold slope, followed by F passivation and then O passivation. It is likely that the passivation reaction is limited by kinetics, as the silicon film cools within $1\,\mu$s after the excimer laser pulse [29]. The efficacy of passivation correlates well with the bonding enthalpies between Si and the passivation species: Si−N has the lowest enthalpy (437 kJ/mol), so that Si−N bonds are formed most easily, followed by Si−F (576 kJ/mol) and then Si−O (800 kJ/mol) [34].

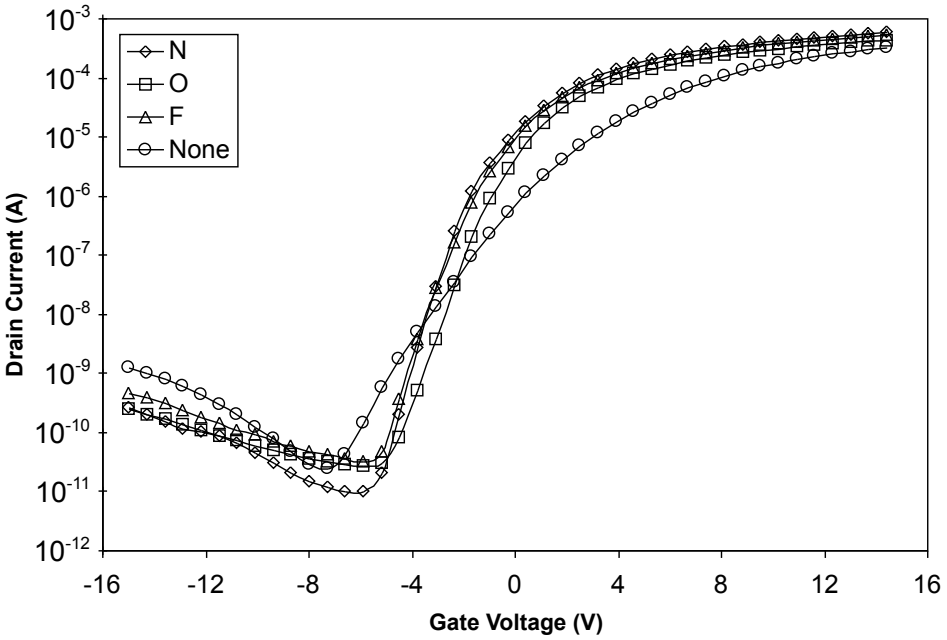

Figure 2.7. I_D vs. V_{GS} transfer curves for unimplanted TFTs vs. TFTs implanted with F, O, and N.

Transfer curves for devices after post-metallization annealing are shown in Fig. 2.8 and Fig. 2.9. Fig. 2.8 shows devices passivated in hydrogen plasma at 350 °C for 2 hours compared with implant passivated devices that have received a 350 °C 2 hour anneal in N_2. Transfer curves for the hydrogen passivated devices and the implant passivated devices are seen to be very similar, indicating that the different passivation techniques are acting with a similar mechanism. Implant passivated devices are still seen to have higher mobility and steeper subthreshold slope than the hydrogen passivated devices, though, looking at Fig. 2.2, further hydrogen annealing will likely continue to improve performance of the hydrogen passivated devices. The hydrogen passivated devices are seen to have lower reverse leakage current than implant passivated devices, possibly due to better passivation of intra-grain defects and defects at the interface between the channel silicon and the underlying oxide layer. The implant passivation technique will likely do a poor job of passivating these defects, as the passivating impurities are pushed out of the grains as they grow laterally and from the bottom to the top of the film. During hydrogen passivation the hydrogen ions

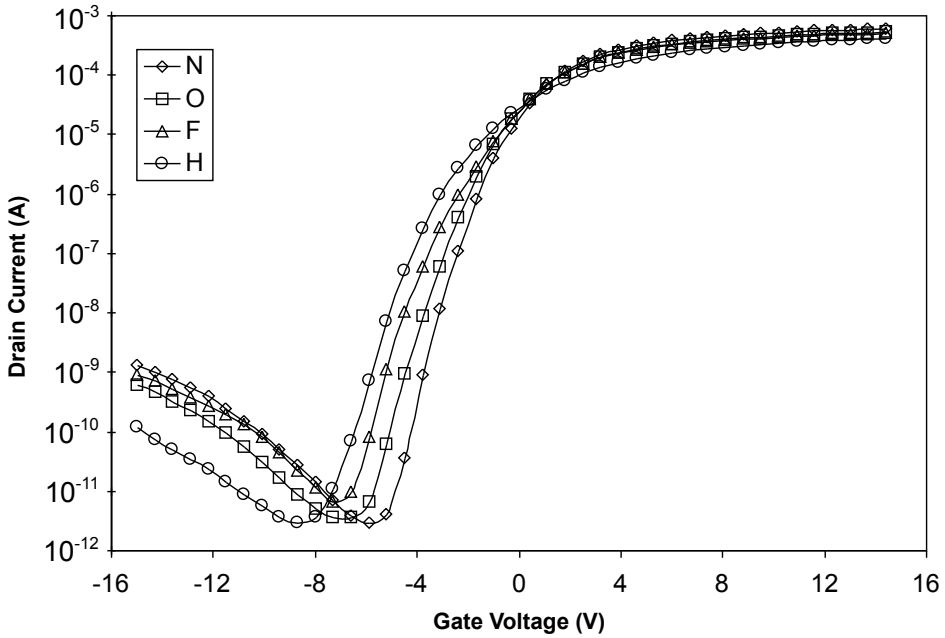

Figure 2.8. I_D vs. V_{GS} transfer curves for hydrogen plasma passivated TFTs vs. TFTs implanted with F, O, and N.

have a long time to diffuse throughout the silicon film and thus will passivate all kinds of defects.

Fig. 2.9 shows transfer curves after post-metallization annealing for devices which received a 600 °C anneal after laser crystallization. Similar trends are seen as for the low-temperature processed devices, where the devices passivated with nitrogen have the highest mobility and steepest slope, and the hydrogen passivated devices have the lowest reverse leakage current. However, the curves are much closer together, and the differences in performance are much smaller than in the case of the low-temperature processed devices. This indicates that the devices are much closer to the limit of the performance increase possible through defect passivation, and thus initially have a much smaller number of defects.

A comparison of unpassivated devices with and without the 600 °C anneal is shown in Fig. 2.10. This confirms the observation that the 12 hour 600 °C anneal serves to reduce the trap state density in the polycrystalline silicon channel, as the annealed devices show higher mobility, steeper subthreshold slope, and lower off-state current. This is not a difference in defect passivation, as neither device has any passivating impurities added. It is unlikely

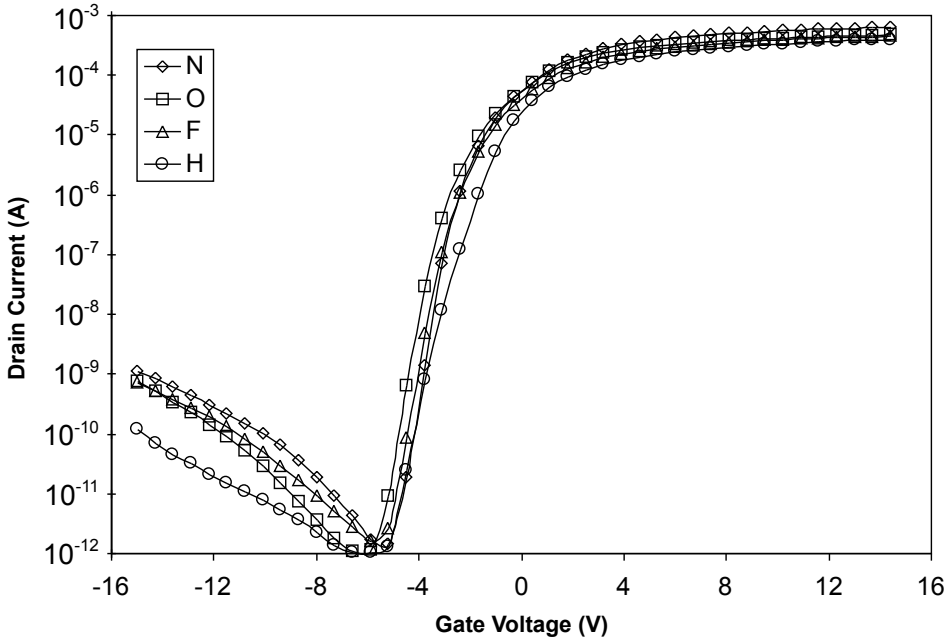

Figure 2.9. I_D vs. V_{GS} transfer curves for 600 °C annealed TFTs passivated by hydrogen plasma and by F, O, and N implant.

that significant grain enlargement occured during the anneal, as the grains formed during a typical ELA process are considerably larger than grains grown by solid phase crystallization at 600 °C. Therefore the most likely explanation of the performance improvement after the 600 °C anneal is healing of intra-grain defects and grain boundary defects as Si atoms are allowed to find their lowest energy state.

Shift in threshold voltage under dc bias stress was measured for devices after 350 °C annealing, and is shown in Fig. 2.11. It was found that stress under high gate bias quickly damaged the low-quality deposited gate oxide, causing negative threshold voltage shifts and confounding measurement of defect generation in the Si channel film. To avoid this effect, stress measurements were conducted under a low gate bias, $V_{GS} = 1\,V$. A high drain bias, $V_{DS} = 15\,V$, was used in order to ensure the devices were turned on sufficiently. The N-passivated device exhibits the greatest V_T shift with stress, followed by the O-passivated and F-passivated devices. The poorer reliability of the N-passivated device could possibly be explained by the low Si−N bond enthalpy. However, the H-passivated device shows the best reliability even though the Si-H bond is weaker than the Si−N bond, having an

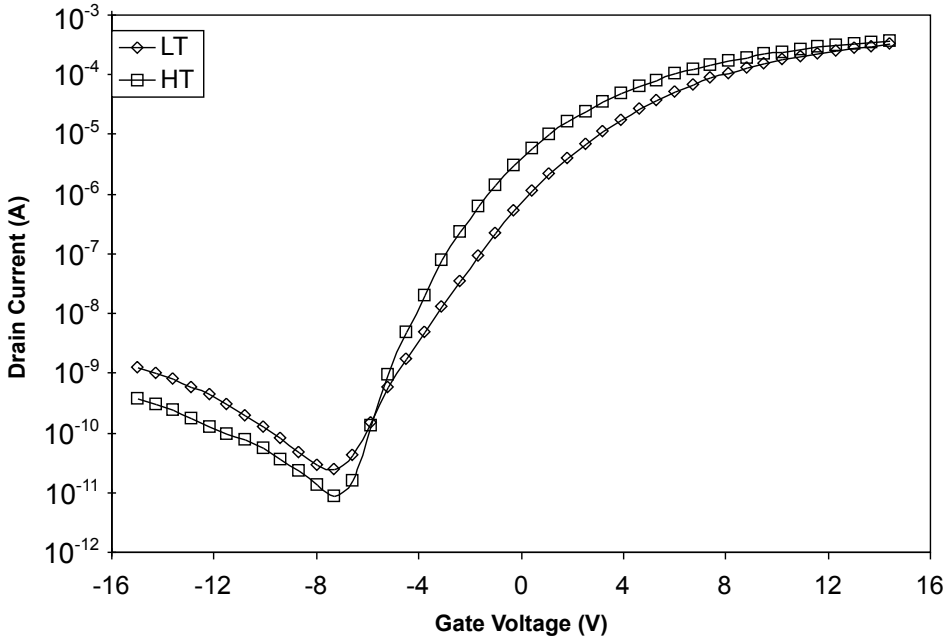

Figure 2.10. Unpassivated TFTs with and without 600 °C annealing after excimer laser crystallization

enthalpy of 300 kJ/mol [34]. This indicates that the implanted species were only able to form weak bonds with Si to passivate the defects, likely due to the extremely short amount of time available for the reaction to proceed.

Measurements of threshold voltage shift in devices which received 600 °C annealing after excimer laser crystallization are shown in Fig. 2.12. A moderate reliability improvement is seen in the H-, O-, and F-passivated devices, but a drastic improvement is seen in the N-passivated devices, such that they exhibit the smallest V_T shift. This may be attributed to the ability of N to bond to three Si atoms if given sufficient thermal energy, so that considerably more energy is required to remove the N atom from the defect site. Devices passivated with O and F show only slightly improved reliability after the long anneal because O and F are able to diffuse out of the film during the anneal, while the diffusion coefficient of N in Si is low enough at 600 °C to make out-diffusion of N negligible.

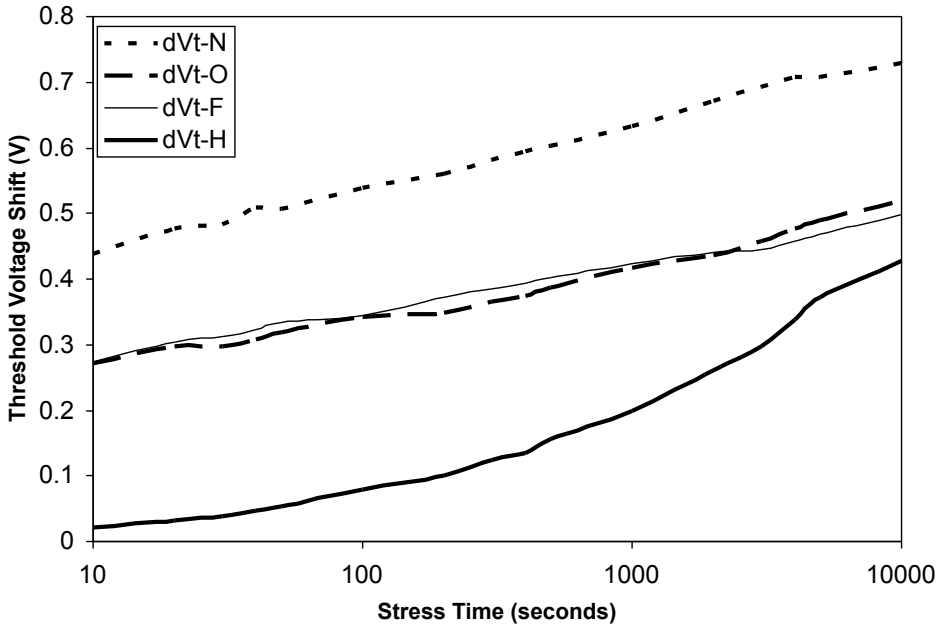

Figure 2.11. Threshold voltage shift vs. stress time for low temperature processed devices.

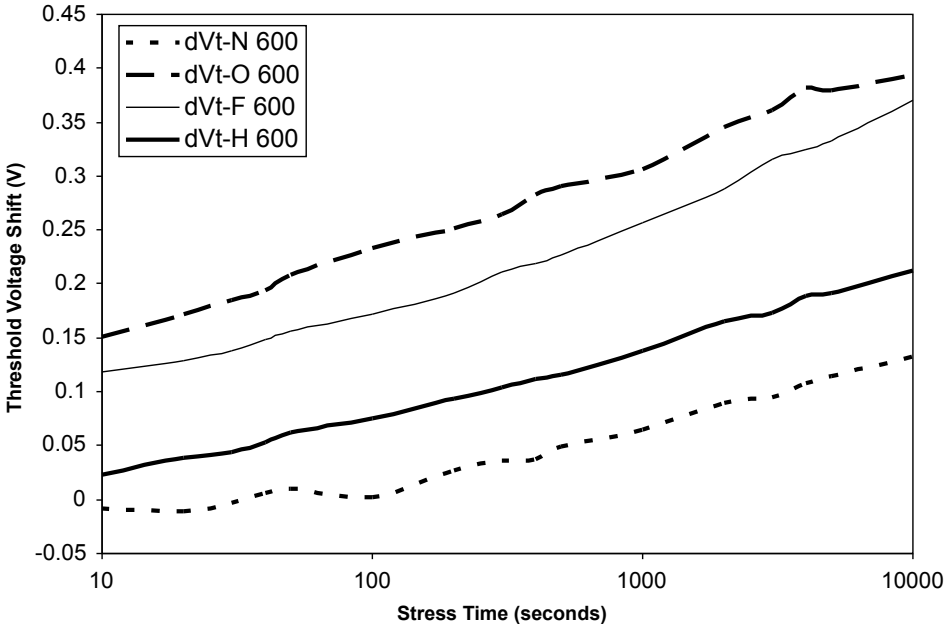

Figure 2.12. Threshold voltage shift vs. stress time for devices which received 600 °C annealing after laser crystallization.

2.6 Summary

In this chapter, defect passivation by ion implantation and pulsed laser annealing is introduced and demonstrated in a glass compatible thin-film transistor process with a maximum temperature of 450 °C. Improved performance in seen in devices with an N, O, or F implant, and improved reliability is seen in N passivated devices with an additional 600 °C anneal. This is the lowest thermal budget demonstration of passivation with nitrogen or fluorine published to date, and suggests that this technique can be succesfully adapted to a plastic-compatible process. Nitrogen may also be used in this way in a more conventional glass compatible process to improve device reliability and to reduce the necessary plasma hydrogenation time to form high-performance devices. Adaptation of this technique to a plastic compatible process is discussed in Chapter 3.

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Chapter 3

Ultra-Low Temperature Poly-Si Thin Film Transistor Fabrication and Defect Passivation

3.1 Ultra-Low Temperature Process Challenges

We seek to demonstrate the compatibility of passivation by ion-implantation and pulsed-laser annealing with an ultra-low temperature poly-Si thin-film transistor process. High-performance plastic-compatible poly-Si thin film transistors are no longer novel, and have been demonstrated by several research groups in recent years. Most notably, they were reported by Tung et al. [1], Gosain et al. [2], and Han et al. [3]. The processes used by these different groups are fairly similar, converging to a set of well-known process steps due to the tight temperature constraints. Each process uses a laser annealed silicon thin film, a high-density plasma gate oxide, pulsed-laser activated source and drain regions, and Al gate and contact layers.

The highest performing devices fabricated on plastic to date were reported in Gosain et al. [2]. In addition to the use of a high-quality gate dielectric, these devices use an

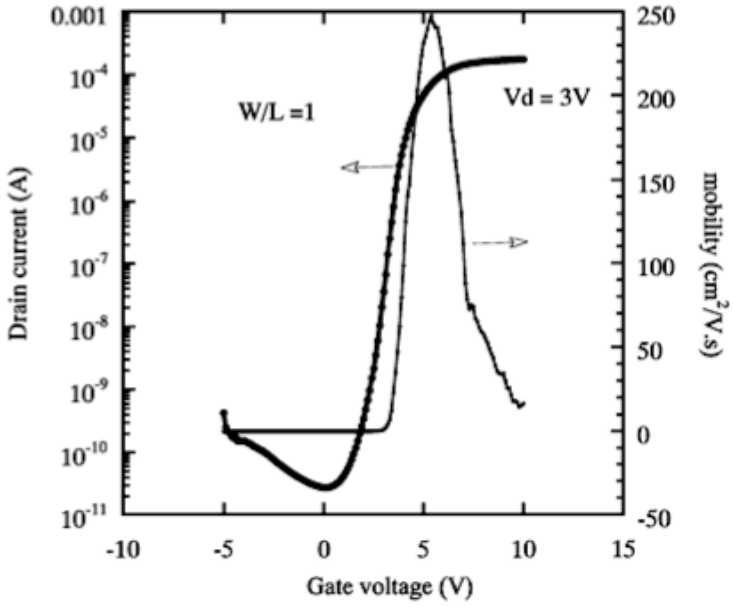

Figure 3.1. 150 °C processed TFTs fabricated by Gosain et al. [2]

excimer laser annealing process with 50 pulses at the optimal annealing energy. Transfer characteristics of a representative device are shown in Fig. 3.1. The devices have a measured mobility of approximately 250 $\frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ and subthreshold slope of 0.16 V/dec. Mobility this high is unusual for a pulsed-laser annealing process, even with such a high number of laser pulses. It is believed that the high mobility is due to the low thermal conductivity of the plastic substrates used, causing the silicon film to cool slowly during the laser annealing process. The authors state that the grain size of the annealed silicon film on a plastic substrate is approximately three times that of a film on a quartz substrate having undergone the same process. Device performance this high shows that there is a promising future for laser annealed poly-Si TFTs on plastic substrates.

However, there is still room for improvement to the plastic-compatible poly-Si TFT process. In particular, the high-density plasma process used for gate oxide deposition is not a manufacturable technique for devices on large-area substrates. Both high-density plasma techniques, inductively coupled plasmas and electron cyclotron resonance plasmas, use a circularly symmetric electromagnetic field to excite the plasma, resulting in a

large ionization density. Circular symmetry is desirable for wafer level processing, but these techniques do not scale well to large rectangular substrates. Uniformity across a display panel is therefore very poor. The gate oxide layer is one of the most critical to device performance, where nonuniformities in thickness will be directly reflected in device performance. Therefore, it is essential to develop a gate oxide process scalable to large area substrates with good uniformity.

Finally, none of the processes referenced above uses any passivation treatment, despite the benefits described in Chapter 2, because none is available in a plastic-compatible process. This work will demonstrate the feasibility of passivation in a plastic-compatible process using ion-implantation and pulsed laser annealing.

3.2 Deposition of a SiO_2 Gate Dielectric Layer by Reactive Sputtering of Si

3.2.1 Sputter Deposition Background

Sputtering has become a very widely used technique for thin-film deposition, commonly used to deposit the metal layers in integrated circuit processes. In flat panel display electronics, it is used for deposition of silicon thin films containing very little hydrogen. Sputtering is a highly manufacturable technique that can deposit a film of high purity over a large area without loss of uniformity. If the process could be used for deposition of a SiO_2 gate dielectric, it would be a highly preferable technique to high-density PECVD.

Sputtering is a physical vapor deposition process rather than a chemical vapor deposition process like LPCVD or PECVD. It operates by physical transport of the material to be deposited from a source to a deposition substrate. A diagram of a typical sputter deposition chamber is shown in Fig. 3.2 with the source of material to be deposited labeled as the target.

The target and substrate are loaded facing one another in the deposition chamber. In the diagram and in the system used in this work, the substrate is face up at the bottom

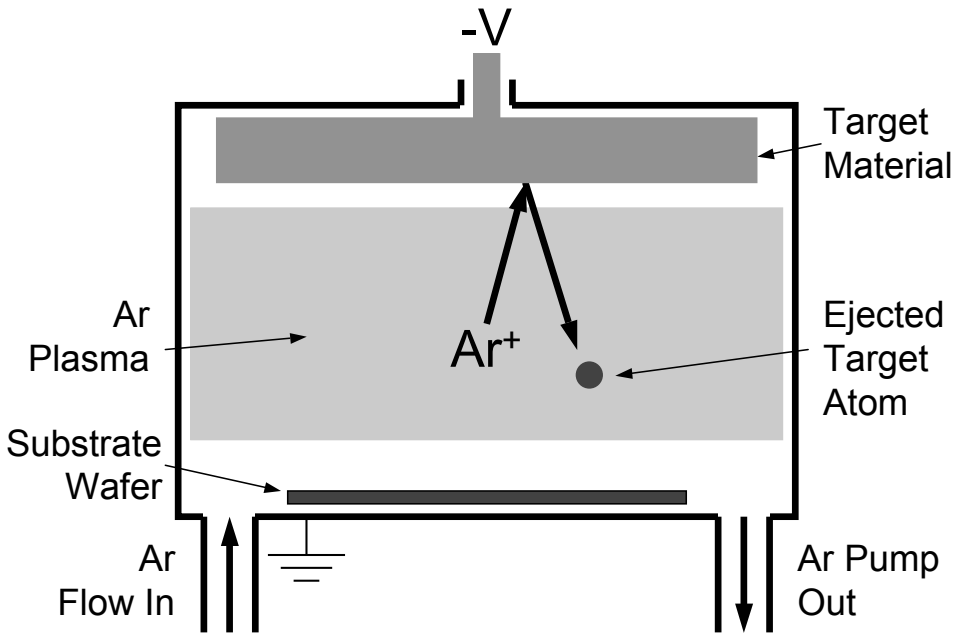

Figure 3.2. A typical dc sputter chamber.

of the chamber, with the target facing down at the top of the chamber. The system is pumped to a low base pressure to remove atmospheric contaminants and refilled with Ar to a pressure of $1 - 10$ mTorr. A high negative dc voltage is placed on the target with respect to the chamber, causing the Ar to ionize to Ar^+. The electric field accelerates the ionized Ar^+ toward the target, causing ions to collide with the target and dislodge material. The material leaves the target in a random direction, travels across the chamber, and deposits on the substrate or the chamber walls. Each point on the target looks like a single point source of material, generating deposition with radial nonuniformity centered on that point. Across the area of the target, the point sources average, creating a large area of uniform deposition, approximately the same size as the target. The target is designed to be larger than the deposition substrate, ensuring uniformity across the entire substrate. When sputtering onto large area rectangular panels, the target can be designed to create uniform deposition in an area longer than the short dimension of the panel. The panel can then be driven slowly through the region of uniform deposition, ensuring a uniform coating across the panel.

A disadvantage to sputter deposition as described is that there is a constant flow of

positive ions colliding with the target. The target must be able to conduct the charge from the ions back to the power supply; otherwise it will build up on the surface, increasing the target voltage and eventually causing an arc back to ground. Therefore, only conductive materials can be sputtered in this way. However, there are two well-known techniques that can be used to deposit dielectric materials by sputtering. The first is to drive the target with high frequency alternating current, rather than with dc. This causes charge to collect on the surface for half of the cycle, and to be removed for half of the cycle, preventing an overall buildup. The power efficiency of an RF sputtering process is poor, however, as only a fraction of the energy put into the plasma goes into dislodging material from the target.

The other commonly used dielectric sputtering method is reactive sputtering. A conductive target is used and driven with dc, as in conventional sputtering; however, the chamber is filled with both Ar and a reactive gas. The Ar ionizes and sputters the target, while at the same time the reactive gas ionizes and reacts with the target material. The reaction occurs either before or after the material has travelled from the target to the substrate, depending on the materials system and process conditions used. This process allows high deposition rate formation of dielectric films, and is commonly used for oxides and nitrides. The major difficulty with reactive sputtering is control over film stoichiometry, as the reaction rate must compete with the deposition rate of the unreacted material, forming partially unreacted films if the deposition conditions are chosen improperly.

Here we attempt to form a SiO_2 gate dielectric layer by reactive sputtering at 150 °C. Since the sputtering process physically moves material from target to substrate, the low temperature will not prevent deposition from occuring, as it might in a chemical vapor deposition process. However, film quality may be poor. Low surface diffusivity at 150 °C can prevent the oxide film from becoming fully dense, as SiO_2 molecules land in a random arrangement on the substrate surface. Fixed charge can develop in the oxide layer as a result of incomplete oxidation of deposited Si, ionization of Si atoms as they are ejected from the target, or incorporation of ionized Ar^+ into the film. The interface quality may also be poor due to the slow rate of reaction at 150 °C between the deposited SiO_2 and the

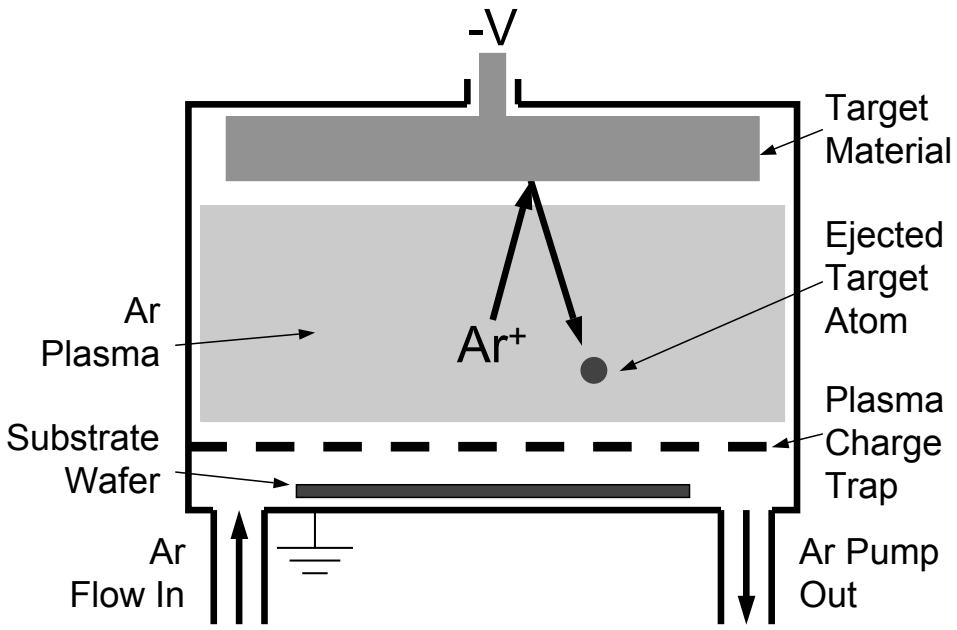

Figure 3.3. A dc sputter chamber with plasma charge trap.

Si substrate surface. In order to form a good quality gate dielectric, steps have been taken to minimize each of these types of defects.

3.2.2 Damage Reduction By Plasma Charge Trap

Development of fixed charge in the oxide layer by incorporation of ionized species has been reduced through the use of a plasma charge trap (PCT) [4]. The PCT is a perforated stainless steel sheet, inserted into the sputter chamber between the high-energy Ar^+ plasma and the substrate. The PCT is inserted 30 mm from the deposition substrate and has 3.32 mm diameter holes with 40.3 % aperture ratio. The deposition rate will therefore be sharply reduced, but as long as the mean free path of the deposition species is significantly shorter than the distance from the PCT to the substrate, uniformity will still be acceptable. The PCT is grounded, causing high-energy ionized species to be collected in the trap rather than allowed to land on the substrate, where they would cause damage and add charge to the surface. A diagram of the sputter chamber with the PCT installed is shown in Fig. 3.3.

Takeuchi et al. [4] investigated effects of the PCT on a sputtered Mo gate layer over a

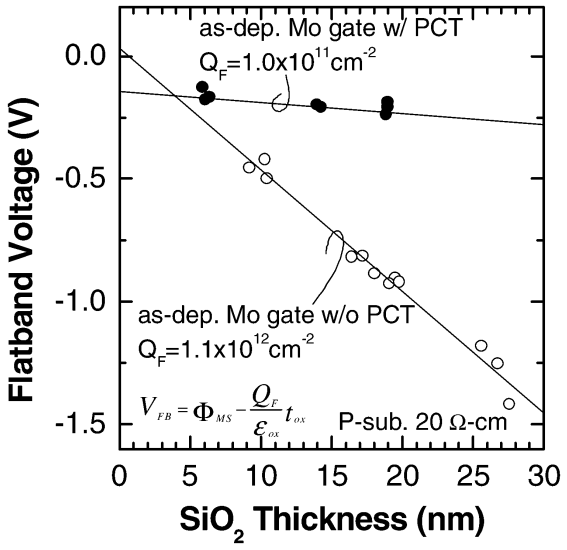

Figure 3.4. Reduction of charge incorporated into a sputtered Mo thin film by plasma charge trap [4].

thin SiO_2 gate oxide, in order to demonstrate the improvement in charge incorporation. A 500 nm Mo gate layer was sputtered at 200 °C onto SiO_2 layers varying in thickness between 5 nm and 25 nm. Flatband voltage of fabricated capacitors was measured and plotted, shown in Fig. 3.4. A reduction in oxide fixed charge by a factor of 10 is seen in devices processed with the PCT, indicating that it has the desired effect of blocking high-energy ionized species. A potential caveat to the use of the PCT in a SiO_2 sputtering process is that it will become coated with insulating SiO_2 as the process proceeds, reducing its effectiveness. Even if this happens, the beginning of the process is when it is most important to prevent damage to the substrate, and this is when the PCT will still be conductive. Between SiO_2 depositions, the PCT was coated with Si to ensure it is conductive at the beginning of the process.

3.2.3 Reactive Sputtering Process Development

To ensure that the SiO_2 film is as dense and as completely oxidized as possible, the process was engineered to have a low deposition rate with a large oxygen partial pressure in the process chamber. Using a partial pressure of 3 mTorr O_2 mixed with 3 mTorr Ar,

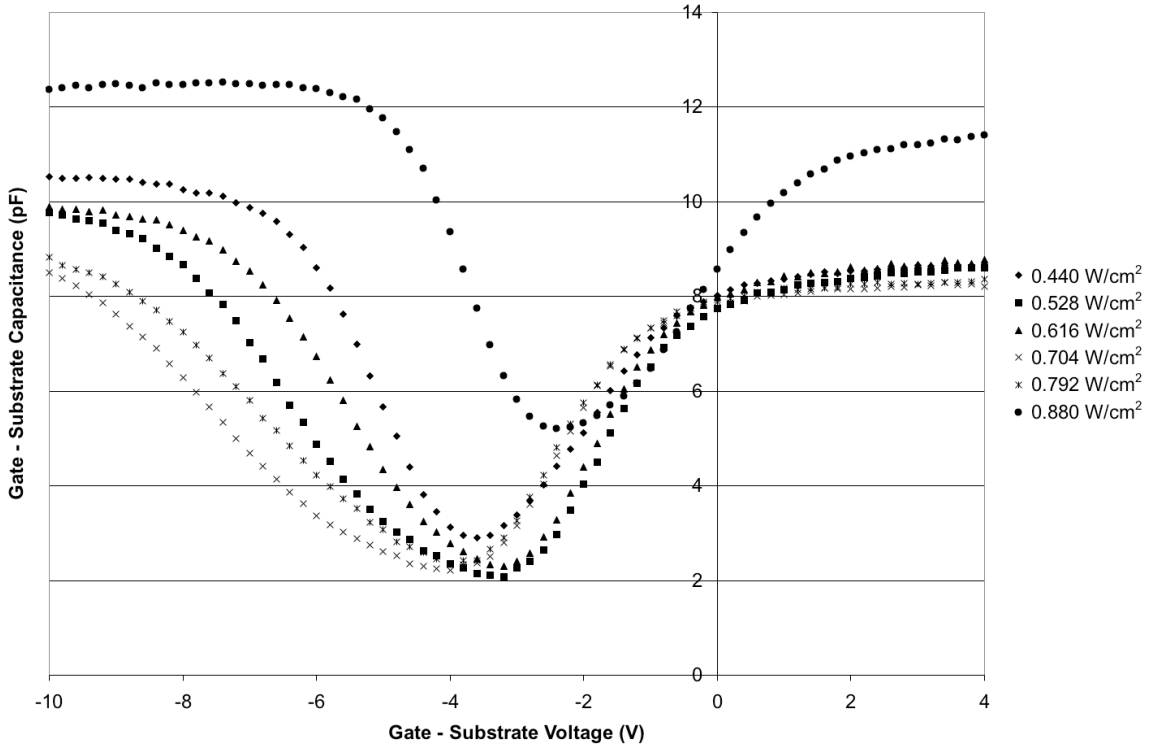

Figure 3.5. Capacitance - Voltage curves for reactively sputtered gate SiO_2 layers varying deposition power density from $0.44\,W/cm^2$ to $0.88\,W/cm^2$.

a study was conducted to find the optimal deposition power. Initially, it was found that using a deposition power above $0.88\,\mathrm{W/cm^2}$ yielded an unstable plasma and films with stoichiometry and thickness varying across the wafer. The oxygen flow inlet is located on the right side of the wafer, and it was found that the oxygen introduced into the chamber was completely consumed before it was able to reach the left side of the wafer, due to the large amount of silicon sputtered for it to react with.

Given the constraint of $0.88\,\mathrm{W/cm^2}$ maximum deposition power density, films were deposited in the range of $0.44\,\mathrm{W/cm^2}$ to $0.88\,\mathrm{W/cm^2}$ in $0.088\,\mathrm{W/cm^2}$ increments. In order to compare the films with capacitance-voltage (CV) measurements, it is desirable to have all experimental films the same thickness. Deposition rate in a sputtering process typically scales linearly with deposition power, so the deposition time for the films was scaled to have a constant (deposition power) $\times$ (deposition time), with a nominal film thickness target of 40 nm. After the SiO_2 deposition onto p-type Si substrates, 200 nm of Al was deposited by sputtering at 100 °C to form a gate layer. The Al was then patterned and wet etched. Quasistatic MOS CV curves were measured with a low-frequency LRC meter, and are shown in Fig. 3.5. The higher capacitances seen in the $0.88\,\mathrm{W/cm^2}$ curve indicate that the deposited Si is not completely oxidized under that deposition condition, causing the film to have a higher than expected dielectric constant. The $0.528\,\mathrm{W/cm^2}$ curve has the steepest slope on the inversion side; so that was selected as the optimal deposition power density.

During the reactive sputtering process development, and later during the use of the process to fabricate TFTs, it is important to ensure that the sputtering target and chamber are in the same initial state for every process run. An oxide layer will build up on the target during processing, and if it is not cleaned off between runs, the process may change from run to run as the layer grows thicker. However, if there is no oxide layer on the target at the beginning of the reactive sputtering process, the process will be unstable as the oxide begins to form. Therefore, a two step cleaning process was run in-between every deposition process. The chamber was first run (with a dummy wafer loaded in the chamber) with

3 mT Ar and no oxygen while monitoring the plasma voltage. Once the voltage stabilized, indicating that target was fully cleaned, the process was stopped, and the chamber gas was changed to the conditions used for processing, 3 mT Ar and 3 mT O_2. The process was then restarted. Once the plasma voltage stabilized again, indicating the initial oxide layer was formed, the process was stopped, and the chamber was ready for the next deposition.

3.2.4 UV Photo-oxidation Pretreatment

In order to improve the interface between the sputtered SiO_2 layer and the underlying poly-Si film, the Si film was first treated with an oxidation process at 150 °C. Thermal oxidation at 150 °C is not an option, as the growth rate is so slow as to be negligible. However, ionized oxygen will react with the silicon substrate, forming a thin SiO_2 layer. Diffusion of ionized oxygen through SiO_2 is still extremely slow at 150 °C, so this process will only form a very thin layer, but the interface formed will potentially be of higher quality than that of a deposited oxide.

Ionized oxygen can be produced through the use of a plasma, and this technique has been used to oxidize silicon for this purpose [5]. However, the oxygen ions in the plasma will be of very high energy and can damage the surface. We attempt to use ultraviolet light to ionize oxygen gas and grow a thin SiO_2 layer on silicon at 150 °C. Examining the ultraviolet absorption cross-section of oxygen, seen in Fig. 3.6, the wavelength where absorption is at its peak is approximately 150 nm, and absorption falls off sharply by 200 nm. High power xenon dielectric barrier discharge lamps are readily available, providing illumination at the xenon excimer wavelength, 172 nm (7.2 eV). This falls in the region of strong oxygen absorption, though not at the peak absorption. Photo-oxidation of silicon with the assistance of a Xe excimer lamp at 250 °C was shown previously by Zhang and Boyd [6].

The photo-oxidation process was first characterized to find the optimal temperature and pressure [9]. Films were grown under a wide range of conditions and characterized for fixed charge and interface trap density. Data for performance vs. oxygen pressure is shown in Fig. 3.7, and for performance vs. temperature in Fig. 3.8. In the low pressure range

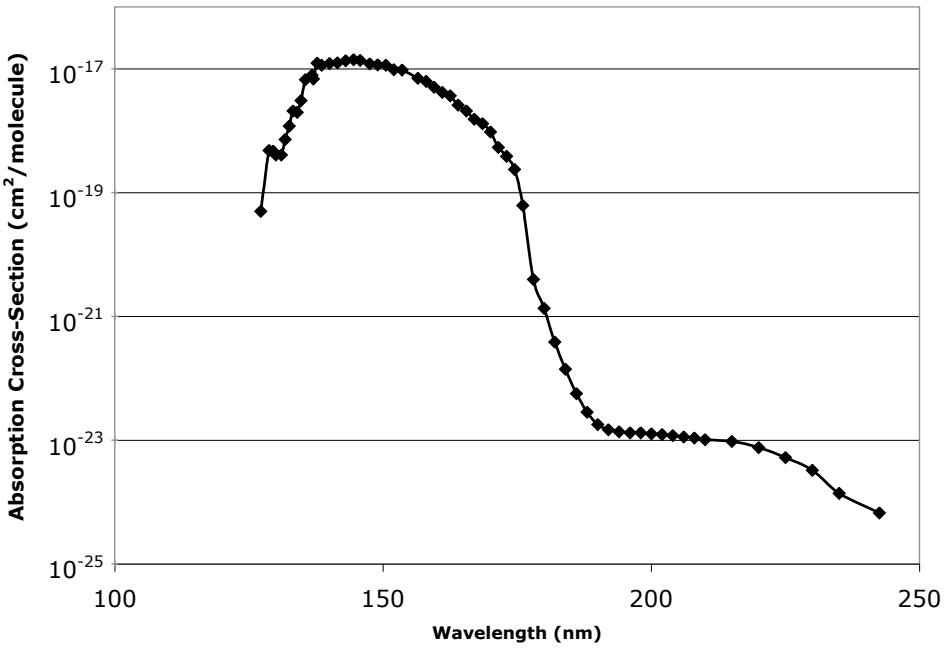

Figure 3.6. Oxygen absorption of light in the range 125 nm - 250 nm. Data from Goldstein et al. [7] and Frederick et al. [8].

of 1×10^{-4} Torr - 1×10^{-3} Torr, process pressure is achieved with a turbomolecular pump, and in the higher pressure range a mechanical pump is used. It is seen that the best quality films are grown at 150 °C, in 5×10^{-4} Torr of oxygen.

Once the optimal photo-oxidation process parameters were established, MOS capacitors were made from reactively sputtered SiO_2 on p-type Si wafers, with and without a photo-oxidation pretreatment. Photo-oxidation is performed in a modified degas station in the sputter deposition cluster tool, allowing wafers to be moved from the photo-oxidation process station to the reactive sputtering process station without exposure to atmosphere. After the photo-oxidation process was performed, 50 nm of SiO_2 was deposited, using the reactive sputtering process parameters determined above. 200 nm of Al was then deposited at 150 °C to form a gate layer. Photolithography and wet etching were then performed to pattern the gate electrodes. MOS CV measurements are shown in Fig. 3.9 with and without UV photo-oxidation. Inversion slope of the device with photo-oxidation pretreatment is considerably steeper, indicating a lower interface trap density, as expected. However, the

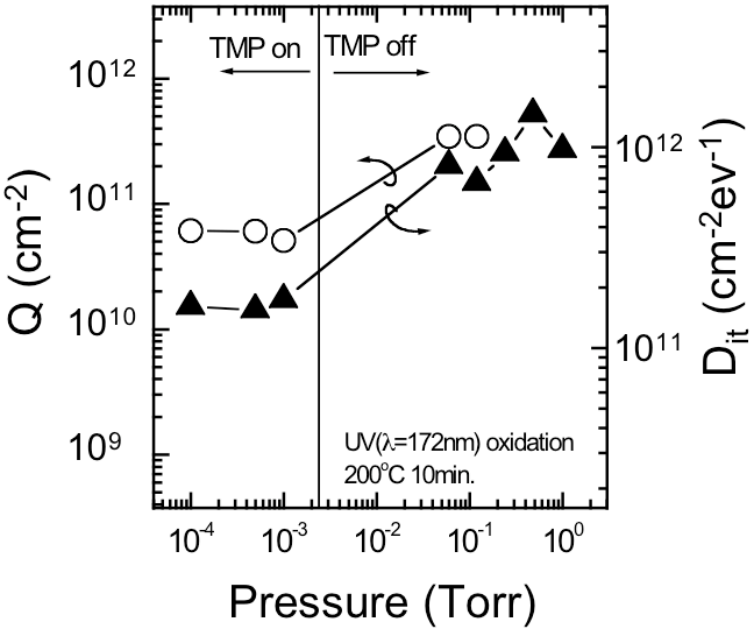

Figure 3.7. Fixed charge and interface trap density of thin SiO_2 films grown by UV photooxidation, varying pressure between 1×10^{-4} Torr and 1 Torr [9]. The films grown at 5×10^{-4} Torr are seen to have the best performance.

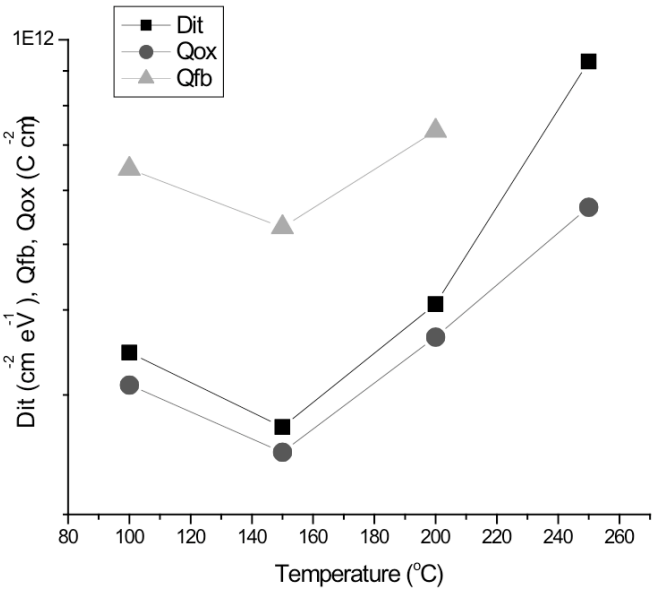

Figure 3.8. Fixed charge, charge at flatband, and interface trap density of thin SiO_2 films grown by UV photooxidation, varying temperature between 100 °C and 250 °C [9]. The films grown at 150 °C are seen to have the best performance.

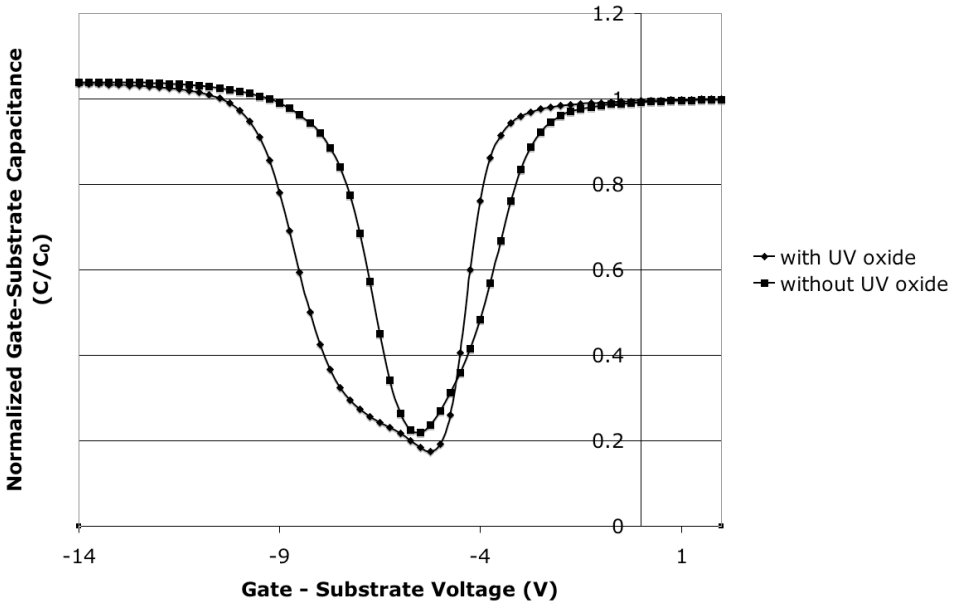

Figure 3.9. Capacitance - Voltage plots for capacitors made with reactively sputtered SiO_2 with and without photooxidation pretreatment. The pretreatment is seen to improve inversion slope but add fixed charge to the device.

flatband voltage is also pushed in the negative direction, indicating the the photo-oxidation process has increased the total oxide fixed charge density.

3.2.5 Laser Oxide Annealing

As a final step to improve the gate oxide quality, a second laser annealing step was performed after oxide deposition, using the same laser apparatus as for silicon crystallization. SiO_2 is transparent to the laser light at 308 nm (4.02 eV), so the light passes through the SiO_2 layer and is absorbed by the underlying Si layer. The transient temperature increase in the Si layer is expected to have an annealing effect on the $Si-SiO_2$ interface, reducing defects. This process has been demonstrated by Han et al. [3] to reduce the flatband voltage of a low-temperature deposited oxide. CV measurements of MOS capcitors made with a low temperature ICP-CVD SiO_2 layer before and after excimer laser annealing are shown in Fig. 3.10. Investigation of the effect of laser annealing on the reactively sputtered gate oxide was left to TFT fabrication, as its performance depends on the interaction between the gate oxide and the underlying thin film. The scanning nature

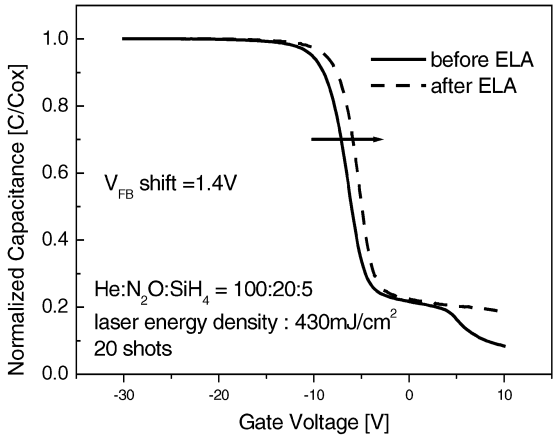

Figure 3.10. Capacitance - Voltage plots for capacitors made with ICP-CVD at 150 °C before and after excimer laser annealing [3].

of the laser treatment allows the laser oxide annealing process to be conducted on only part of the wafer, and device results with and without this treatment can be compared.

3.3 Ultra-Low Temperature Thin Film Transistor Process

Self-aligned top-gate TFTs were fabricated using a process similar to the 450 °C process described in section 2.4, modified to keep all TFT processing steps at or below 150 °C. Silicon wafers with 1 μm of wet thermal oxide were used as starting substrates. A 50 nm silicon channel film was deposited by room temperature sputtering. 55 nm of SiO_2 was then deposited by conventional PECVD at 150 °C as a screen for the passivation implant. A slightly thicker screen oxide layer was used as compared with the 450 °C process due to the low density of the PECVD oxide. Passivation species (N, O, and F) ion implantation was performed using conditions chosen similarly to the higher temperature process, putting the peak impurity concentration at the interface between the Si film and the screen oxide, with a total concentration of 1×10^{14} ions/cm^2 in the Si layer. The screen oxide was then removed in dilute HF.

A two-step excimer laser annealing process was then performed. First, the Si film was crystallized with 3 laser pulses at a fluence of approximately 300 mJ/cm^2. The

crystallization fluence was chosen to be just below the full melt threshold, observed by optical inspection of surface roughness. A second laser annealing step followed crystallization, in an attempt to replicate the post-ELA high-temperature anneal used in section 2.4. The laser anneal was performed with a fluence of approximately 170 $\mathrm{mJ/cm^2}$, for 0, 10, 30, and 100 pulses in separate regions on each wafer, arranged in horizontal stripes. The annealing fluence was chosen to be just below the minimum energy necessary to melt the silicon film, in order to heat the film without melting.

After ELA, the poly-Si films were patterned and dry etched to form TFT active regions. Resist softbake and post-exposure bake were at 90 °C, and the post-develop hard bake was done under UV light at 140 °C. After etching, resist strip was done in oxygen plasma at 150 °C. These resist processing steps were used in the lithography process for each patterned layer.

Following active layer etching, 50 nm of reactively sputtered $\mathrm{SiO_2}$ with a photo-oxidation pretreatment was deposited according to the process described in section 3.2. A laser annealing treatment was then performed on the gate oxide layer. The annealing process was performed with 10 laser pulses at a fluence of approximately 130 $\mathrm{mJ/cm^2}$, covering the right half of each wafer. In this way, half of each of the horizontal stripes with different numbers of pulses in the second laser annealing step received the gate oxide anneal. The fluence of 130 $\mathrm{mJ/cm^2}$ was chosen as the highest laser fluence that could be used without any visible damage to the gate oxide layer.

A 150 nm Al gate layer was deposited by dc sputtering at 150 °C, patterned, and wet etched. $\mathrm{SiO_2}$ gate-sidewall spacers 50 nm thick were then formed by PECVD at 150 °C and anisotropic dry etching. Heavy n-type doping of the source and drain regions was accomplished with phosphorus ion implantation, at a dose of 1×10^{15} $\mathrm{ions/cm^2}$ and energy of 34 keV. The source and drain implant was activated with a final ELA step, using three shots at 110 $\mathrm{mJ/cm^2}$. A lower fluence activation step compared with section 2.4 was necessary, as the gate oxide layer damaged easily under laser irradiation.

A 200 nm $\mathrm{SiO_2}$ insulation layer was deposited by PECVD at 150 °C, and contact holes

Table 3.1. Performance of 150 °C Processed Devices without Gate Oxide Annealing

Device	I_{min} pA	I_{max} nA	μ_{eff} $cm^2/V{\cdot}s$	V_T V	S V/dec
control - 0 shots	3.22	54.0	0.41	3.30	1.04
control - 10 shots	2.11	57.1	0.47	3.12	1.01
control - 30 shots	1.87	64.8	0.53	3.04	0.96
control - 100 shots	1.28	51.3	0.38	3.13	0.97
F - 0 shots	4.54	65.5	0.57	2.74	1.04
F - 10 shots	3.28	59.2	0.51	2.65	1.01
F - 30 shots	2.34	67.1	0.55	2.77	0.96
F - 100 shots	2.68	56.9	0.47	2.62	1.01
O - 0 shots	3.65	71.5	0.59	2.89	1.03
O - 10 shots	3.31	51.9	0.42	2.77	1.01
O - 30 shots	2.30	62.8	0.48	2.75	0.98
O - 100 shots	2.41	59.6	0.46	2.66	0.97
N - 0 shots	9.90	47.5	0.70	1.98	1.28
N - 10 shots	9.46	57.1	0.69	1.92	1.25
N - 30 shots	7.57	60.0	0.83	1.75	1.26
N - 100 shots	7.05	56.9	0.76	1.68	1.26

were patterned and dry etched. Finally, a 500 nm Al/2% Si layer was deposited by dc sputtering, patterned, and wet etched. A sputter cleaning process was used to remove native oxide from the source and drain regions of the devices immediately before contact Al/Si deposition, in order to encourage formation of low resistance ohmic contacts.

3.4 Device Performance

3.4.1 Nominal Device Performance

Transfer characteristics of a W/L = 50 μm/5 μm TFT are shown in Fig. 3.11. This device has no passivation implant, 0 shots in the non-melt laser annealing step, and no gate oxide annealing. Performance is much poorer than the devices seen in Chapter 2.

Table 3.2. Performance of 150 °C Processed Devices with Gate Oxide Annealing

Device	I_{min} pA	I_{max} nA	μ_{eff} $cm^2/V{\cdot}s$	V_T V	S V/dec
control - 0 shots	1.59	119	1.61	3.24	0.82
control - 10 shots	1.73	74.3	1.48	3.24	0.85
control - 30 shots	0.98	63.5	0.70	3.24	0.81
F - 0 shots	2.10	91.4	0.58	2.68	0.72
F - 10 shots	2.24	72.6	0.93	2.10	0.75
F - 30 shots	2.59	77.9	1.07	1.93	0.77
O - 0 shots	1.34	108	0.69	2.65	0.65
O - 10 shots	2.74	51.1	0.39	2.36	0.84
O - 30 shots	2.95	68.2	0.47	2.15	0.79
N - 0 shots	5.19	36.2	0.23	2.34	1.18
N - 10 shots	6.09	40.0	0.18	2.36	1.31
N - 30 shots	5.23	29.7	0.23	1.97	1.17

The subthreshold slope is approximately 1.0 V/decade and threshold voltage approximately 3.3 V, which are reasonable values, however, the output current is very low. Measured mobility is approximately 0.4 $\frac{cm^2}{V{\cdot}s}$, and peak output current is only 3 μA with $V_{GS} = 10$ V and $V_{DS} = 5$ V, leading to an on/off ratio of approximately 4 orders of magnitude. The only major difference between the 450 °C process and the ultra-low temperature process is the gate oxide deposition step; so it is likely that a poor quality $Si{-}SiO_2$ interface is responsible for the low current. Despite the efforts taken to avoid damage to the interface, sputter deposition will produce an interface which is far rougher than a CVD process, resulting in acceptable CV curves and TFT turn-on behavior but low mobility.

Even though device performance is poor, the TFTs are functional devices, and performance is good enough to examine the effects of the various experimental splits. Data from devices processed with different passivation and laser annealing conditions are shown in the following sections, and a summary of the performance of $W/L = 50\,\mu m/5\,\mu m$ devices is shown in Table 3.1 and Table 3.2. The number of shots indicated refers to the number of non-melt excimer laser shots performed after laser crystallization.

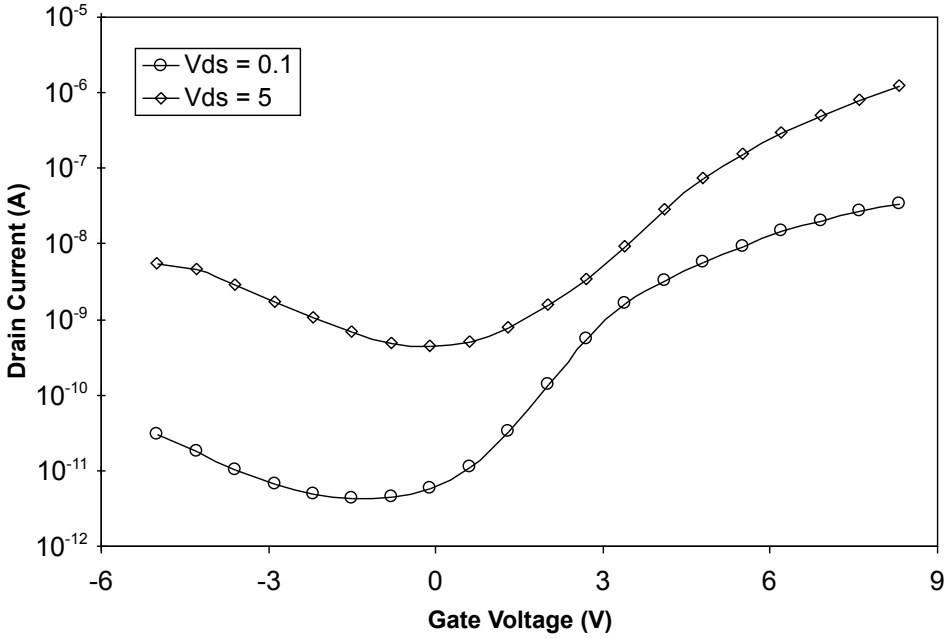

Figure 3.11. Transfer characteristics of a TFT fabricated at 150 °C with reactively sputtered gate oxide. Device dimensions are W/L = 50 μm/5 μm.

3.4.2 Effects of Passivation Implant

Fig. 3.12 shows transfer characteristics from devices with F, O, and N passivation implants, and from a device with no passivation. The devices are W/L = 50 μm/5 μm, with V_{DS} = 0.1 V. Unlike in the 450 °C process, passivation with nitrogen is seen to degrade performance, increasing the subthreshold slope from 1.0 V/decade for the control device to 1.3 V/decade. The threshold voltage is greatly reduced, however, decreasing to 2 V. This behavior is consistent with nitrogen becoming active in the Si film as a deep level trap. Nitrogen is a group V impurity and would be expected to dope Si in a similar way to phosphorous or arsenic. However, due to the large discrepancy in atomic radius between N and Si, the N impurity sits slightly off of the lattice site in the $\langle 111 \rangle$ direction [10]. This pushes the donor level down into the bandgap, approximately at $E_c - 0.4$ eV [11]. The asymmetry of the lowest energy configuration for N substitutional in Si causes activation to be poor, with only a few percent becoming substitutionally active under optimal processing conditions. A low concentration of n-type deep level traps would have the observed effects of

lowering the threshold voltage, raising the off-state current, and degrading the subthreshold slope.

Instability of the nitrogen substitutional defect additionally causes it to be easily deactivated. Brower [10] found that the substitutional nitrogen defect disappears upon annealing above 400 °C, shown in Fig. 3.13. Deactivation in this way explains why deep-level traps are seen in the ultra-low temperature processed devices but not in the devices fabricated with a 450 °C gate oxide. Unfortunately, this indicates that nitrogen is not an appropriate passivation species for a plastic-compatible process when used in this way.

In devices passivated with oxygen and with fluorine, a reduction in threshold voltage of approximately 0.5 V is seen; however, the subthreshold slope is unchanged. It is possible that the implanted oxygen and fluorine are passivating defects in the silicon film, leading to the threshold voltage improvement, but the subthreshold slope is limited by the large number of defects at the oxide interface, which is not affected by the implant. It is unlikely that the threshold voltage shift comes from any interaction between the implanted material and the gate oxide, as there is very little thermal energy added to these samples after the gate oxide deposition. Additionally, it is unlikely that the threshold voltage shift comes from a doping effect, as it would have been seen in the 450 °C processed devices as well.

3.4.3 Effects of Non-Melt Laser Annealing

Non-melt laser annealing shots after excimer laser crystallization are seen to have a moderate beneficial effect on performance for both the unpassivated devices (shown in Fig. 3.14) and the implant passivated devices. For each implant condition, the non-melt laser annealing improves the subthreshold slope and lowers the off-current, as the thermal energy allows some of the defects in the Si film to heal. Improvement in the F and O implanted devices is comparable to the improvement in the control devices, suggesting that the annealing is not facilitating any further passivating effects. A small performance increase is seen in the N implanted devices, but not enough to suggest that the laser annealing treatment has a depassivating effect on the nitrogen deep level traps.

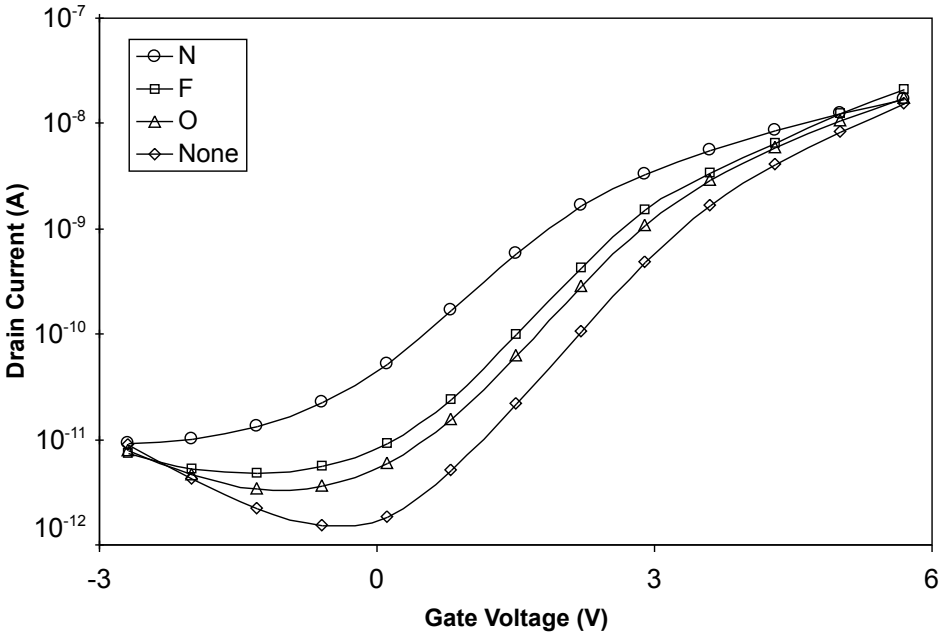

Figure 3.12. Transfer characteristics of TFTs processed at 150 °C with N, O, and F passivation implants, and control devices. Device dimensions are W/L = 50 μm/5 μm, and V_{DS} = 0.1 V.

3.4.4 Effects of Gate Oxide Laser Annealing

Transfer characteristics of devices which received gate oxide annealing and 30 non-melt laser annealing shots are shown in Fig. 3.15. Unpassivated devices show an improvement in subthreshold slope from 1.0 V/decade to 0.8 V/decade, indicating the gate oxide anneal has reduced the total number of interface defects. Fluorine and oxygen implanted devices show an improvement in subthreshold slope beyond what is seen in the unpassivated devices. This indicates that the heat treatment is serving both to heal interface defects and to allow the implanted fluorine and oxygen to passivate interface defects.

During the laser crystallization process, the implanted impurities diffuse out of the crystal as it grows laterally and from bottom to top of the film, piling up at grain boundaries and at the surface of the film. The high concentration of impurities at the $Si-SiO_2$ interface then is available to passivate interface defects if thermal energy is provided, as with the laser oxide annealing.

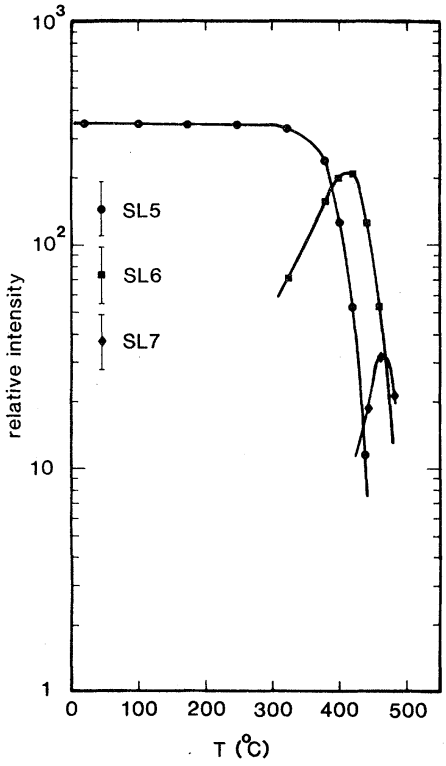

Figure 3.13. Electron paramagnetic resonance measurements of nitrogen doped silicon after 20 minutes annealing at varying temperatures [10]. SL5 indicates the nitrogen substitutional defect.

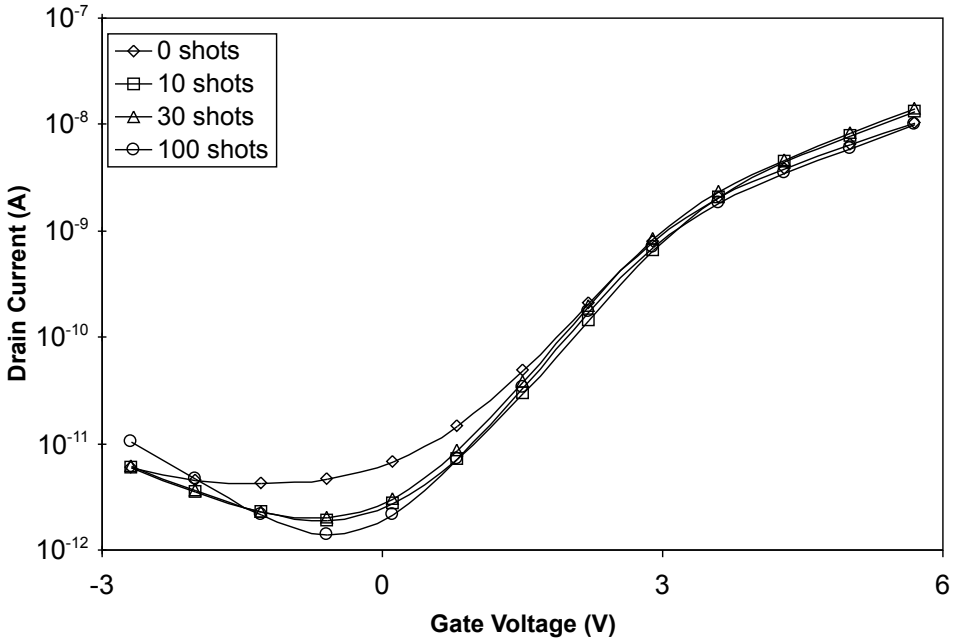

Figure 3.14. Transfer characteristics of 150 °C processed, unpassivated devices with 0 - 100 pulses of non-melt laser annealing after crystallization. Device dimensions are W/L = 50 μm/5 μm, and V_{DS} = 0.1 V.

Data are not shown for devices with 100 pulses of non-melt excimer laser annealing and gate oxide annealing as yield for those devices was extremely low, breaking down at very low voltage on the gate or drain. The silicon region annealed which received 100 ELA pulses after crystallization is visibly much rougher than the other silicon areas. The very rough interface may cause formation of additional defects during gate oxide annealing.

No significant shifts in mobility were seen across all passivation and laser annealing conditions. Mobility is strongly affected by surface roughness, even in the absence of electronically active states. The effects that have been seen from the passivation and laser annealing treatments are from the creation and removal of electronic states within the layers and at the interface and are largely not related to the physical morphology of the interface.

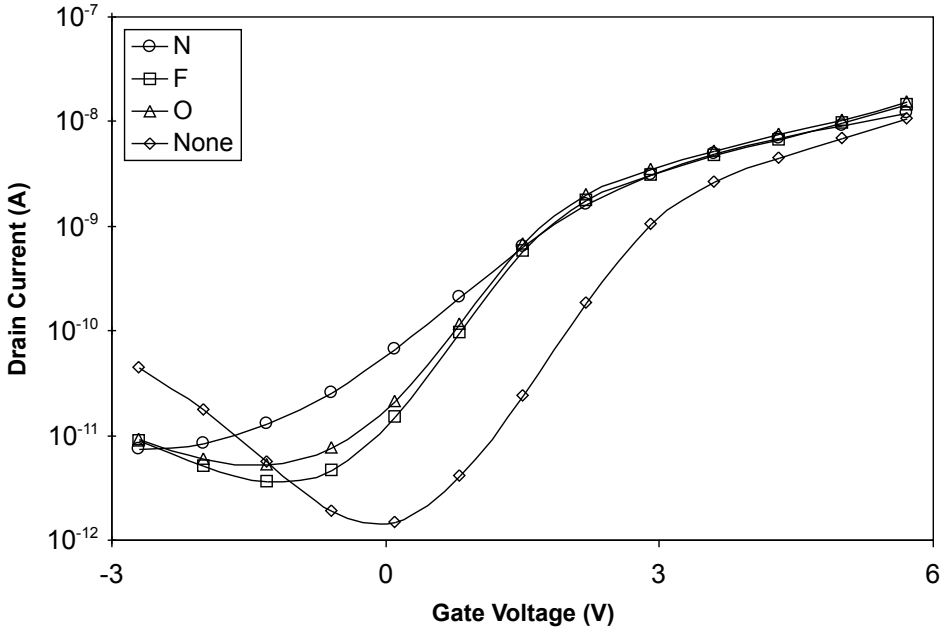

Figure 3.15. Transfer characteristics of TFTs processed at 150 °C with N, O, and F passivation implants, and control devices. Devices received laser annealing after gate oxide deposition. Device dimensions are W/L = 50 μm/5 μm, and V_{DS} = 0.1 V.

3.5 Device Reliability

Threshold voltage shift under dc bias stress was measured, as in Chapter 2. Devices were found to break down quickly under high gate or drain bias, due to the poor-quality gate oxide interface. In order to get a good measurement of breakdown over time, low gate and drain bias stress voltages were used, V_{GS} = 1 V, and V_{DS} = 3 V. Threshold voltage was measured by the constant-current method, as before. However, it was necessary to compare threshold shift of devices with very different nominal threshold voltage and subthreshold slope. In order to ensure that different devices are in the same region of operation at their measured threshold voltage, the current at which the threshold voltage is measured is defined as the current flowing through the device at its peak subthreshold slope, in the t_{stress} = 0 s curve.

3.5.1 Effects of Passivation Implant

Threshold shift of devices processed with different passivation conditions, with no non-melt laser annealing pulses and no gate oxide annealing, are shown in Fig. 3.16. Unpassivated devices are seen to have the steepest threshold voltage increase with stress time, significantly higher than any of the implant passivated devices. This is in contrast to the devices processed at 450 °C, shown in Fig. 2.11, where implant passivated devices had more threshold voltage shift than the the control device. The 450 °C gate oxide deposition had the side effect of removing some strained or weak bonds at silicon grain boundaries, improving the reliability of the unpassivated devices shown in Fig 2.11. Even at low temperature, the passivation implant serves to reduce the density of easily-broken bonds, improving the overall reliability.

Similarly to Fig. 2.11, devices passivated with nitrogen shown in Fig. 3.16 have the largest threshold shift after a short stress time. However, the nitrogen passivated devices shown in Fig. 3.16 have a very shallow slope of threshold shift compared with devices for the other passivation conditions. The primary electrical effect of nitrogen in the ultra-low temperature processed devices is to act as a deep-level trap, giving the devices a significant negative threshold shift. This defect is much more difficult to remove with electrical stress than the nitrogen impurities serving to passivate defects at silicon grain boundaries, thereby reducing the rate of threshold shift with stress. Impurities passivating defects at grain boundaries are deactivated quickly, leading to the large initial threshold shift in the nitrogen passivated devices.

3.5.2 Effects of Non-Melt Laser Annealing

Reliability of nitrogen passivated devices was found in Chapter 2 to be significantly improved by a 600 °C anneal. A similar effect was seen in the nitrogen passivated devices processed at 150 °C, with the addition of non-melt laser annealing pulses after laser crystallization. Threshold shift of devices processed with different passivation conditions,

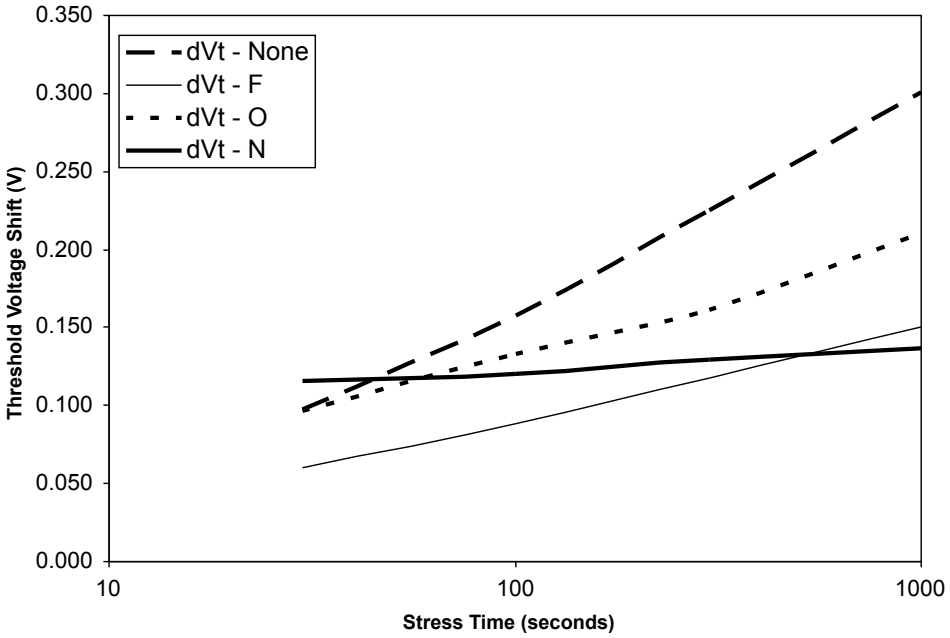

Figure 3.16. Threshold voltage shift with electrical stressing time of devices with N, O, and F implant, and control devices. Bias stress voltages used are $V_{GS} = 1\,V$ and $V_{DS} = 3\,V$. Device dimensions are $W/L = 50\,\mu m/3\,\mu m$.

with 30 non-melt laser annealing pulses and no gate oxide annealing, are shown in Fig. 3.17. Total threshold shift after 1000 s for all passivation conditions is seen to reduce by approximately 30%, but the nitrogen-passivated device has gone from having the most threshold shift after a short time to having the least, indicating that the non-melt laser annealing pulses were successful in replicating the effects of 600 °C annealing.

Threshold shift of fluorine-implanted devices with different numbers of non-melt laser annealing pulses and no gate oxide annealing is shown in Fig. 3.18. The trend seen here is representative of the other implant conditions as well. A large improvement is seen from devices with no non-melt laser annealing to devices with 10 pulses, and devices with 30 pulses are comparable to those with 10 pulses. Devices with 100 non-melt laser annealing pulses are seen to have a considerably larger threshold shift than any of the other conditions. The silicon regions which have received 100 laser pulses are visibly rougher than regions processed with fewer non-melt laser pulses. The roughness increases the number of weak bonds at the gate oxide interface, leading to increased threshold shifts under electrical stress.

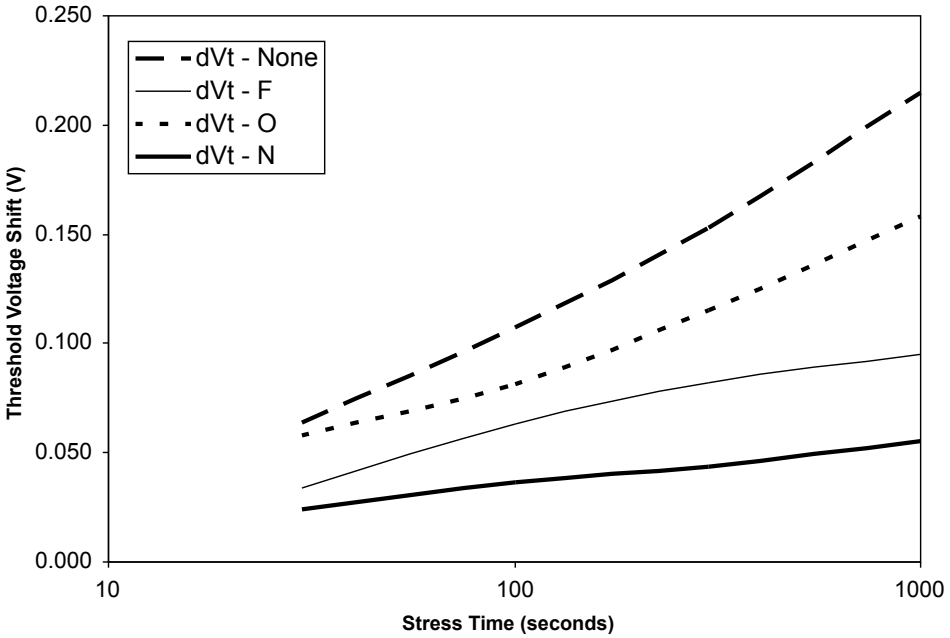

Figure 3.17. Threshold voltage shift with electrical stressing time of devices with N, O, and F implant, and control devices. Devices received 30 pulses of non-melt laser annealing after crystallization. Bias stress voltages used are $V_{GS} = 1\,V$ and $V_{DS} = 3\,V$. Device dimensions are $W/L = 50\,\mu m/3\,\mu m$.

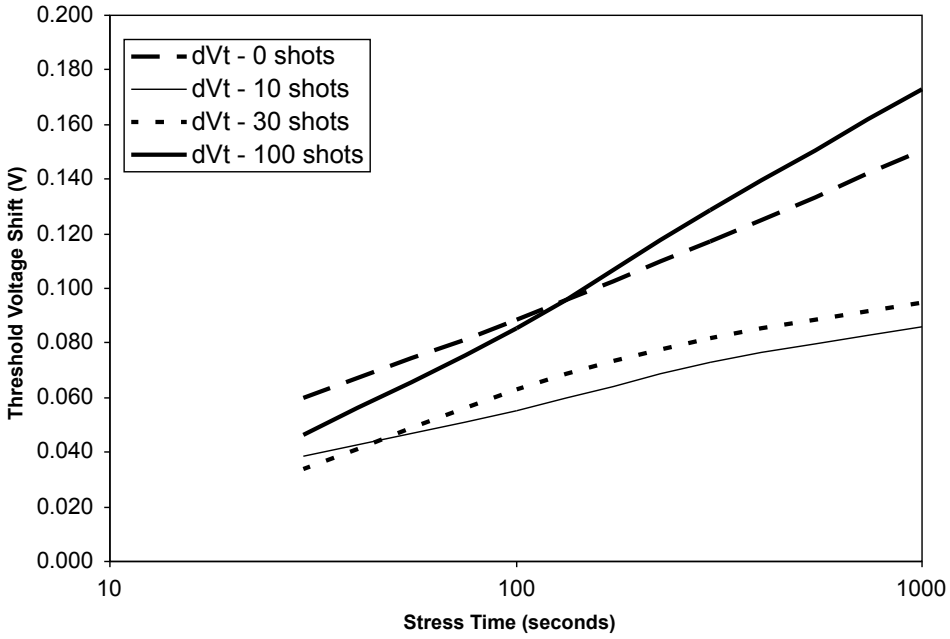

Figure 3.18. Threshold voltage shift with electrical stressing time of devices with F implant. Devices received 0 - 100 pulses of non-melt laser annealing after crystallization. Bias stress voltages used are $V_{GS} = 1\,V$ and $V_{DS} = 3\,V$. Device dimensions are $W/L = 50\,\mu m/3\,\mu m$.

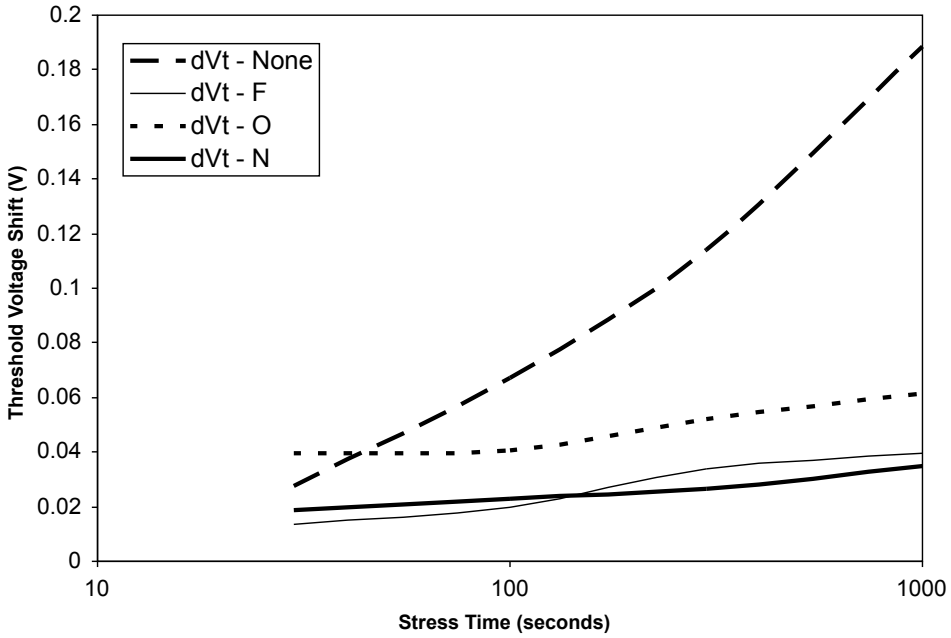

Figure 3.19. Threshold voltage shift with electrical stressing time of devices with N, O, and F implant, and control devices. Devices received 30 pulses of non-melt laser annealing after crystallization and laser annealing after gate oxide deposition. Bias stress voltages used are $V_{GS} = 1\,V$ and $V_{DS} = 3\,V$. Device dimensions are $W/L = 50\,\mu m/3\,\mu m$.

3.5.3 Effects of Gate Oxide Laser Annealing

Threshold shift of devices processed with different passivation conditions with 30 non-melt laser annealing pulses and 10 gate oxide laser annealing pulses are shown in Fig. 3.19. A similar trend is seen to Fig. 3.17 for devices processed under the same conditions but without the gate oxide anneal, and the threshold shift for the unpassivated device is nearly unchanged. However, all of the implant passivated devices show a large reduction in threshold shift with stress time. Combined with the measurements of transfer curves showing an improvement in threshold voltage with gate oxide laser annealing, this data strongly suggests that the implanted impurities are becoming activated to passivate defects at the $Si-SiO_2$ interface during the gate oxide laser annealing process.

Threshold shift of fluorine-implanted devices with different numbers of non-melt laser annealing pulses and 10 gate oxide laser annealing pulses is shown in Fig. 3.20. As shown in Fig. 3.19, threshold shift of devices processed with gate oxide laser annealing pulses

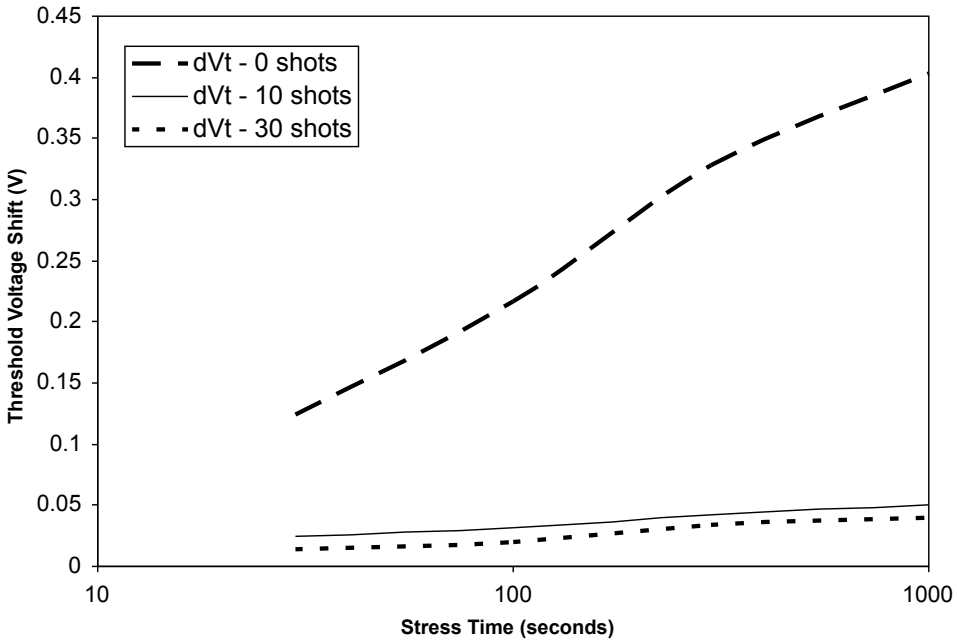

Figure 3.20. Threshold voltage shift with electrical stressing time of devices with F implant. Devices received 0 - 30 pulses of non-melt laser annealing after crystallization and laser annealing after gate oxide deposition. Bias stress voltages used are $V_{GS} = 1\,V$ and $V_{DS} = 3\,V$. Device dimensions are $W/L = 50\,\mu m/3\,\mu m$.

and non-melt laser annealing pulses is improved considerably over devices with non-melt laser annealing pulses and no gate oxide laser annealing pulses. However, threshold voltage shift of devices with gate oxide annealing but no non-melt laser annealing is seen to be increased considerably for all passivation conditions. This effect is likely caused by poor film morphology, rather than creation of defects, as it happens equally to the passivated films and unpassivated films. It is possible that a small number of non-melt laser annealing shots smoothes the surface of the poly-Si film, allowing the gate oxide laser annealing to heat the film without damage.

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Chapter 4

Silicon Crystallization by Copper Vapor Laser Annealing

4.1 Laser Properties

Excimer laser crystallization of silicon has become a standard and well-understood process in the fabrication of poly-Si thin film transistors. It enables the formation of high quality poly-Si films while meeting restrictions on substrate thermal budget. The high output power and high available pulse rate of excimer lasers allows for relatively high throughput systems. Silicon has a high absorption at the UV wavelengths of light produced by common excimer laser systems, causing efficient energy conversion from laser light into heat in the thin film. A plot of the optical absorption of amorphous silicon is shown in Fig. 4.1 [1]. At typical excimer wavelengths (248 nm $\Rightarrow$ 5.0 eV, 308 nm $\Rightarrow$ 4.0 eV), absorption is approximately $1 \times 10^6\,\mathrm{cm}^{-1}$, yielding a penetration depth of 10 nm. Typical silicon TFTs have a 50 nm thick silicon film, which will easily absorb the entire pulse energy. This is particularly important for laser processing of silicon on a low-cost glass or plastic substrate, as the substrate materials will absorb light at excimer wavelengths, causing damage if any of the laser energy was transmitted through the silicon film.

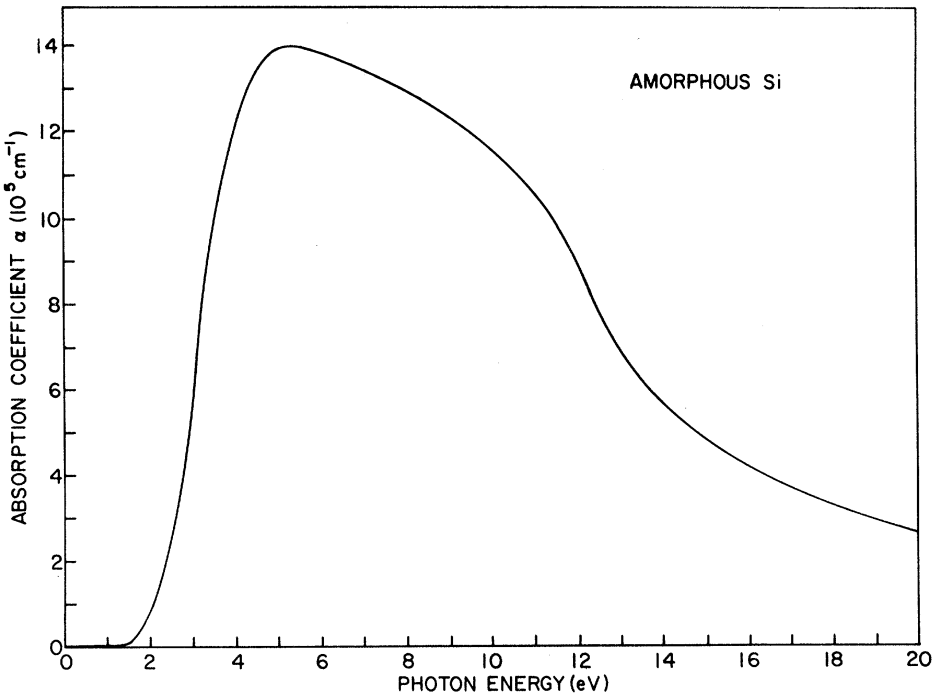

Figure 4.1. Optical absorption coefficient for amorphous silicon [1].

There are disadvantages to excimer laser processing that warrant investigation into other methods of silicon crystallization. The most important is the pulse energy variation of excimer systems. Typical excimer systems have a pulse energy σ of 2% [2], leading to a total 3σ pulse energy variation of ± 6 %. This is a modest variation, but the laser annealing process is very sensitive to pulse energy stability. Seen in Fig. 1.6, the variation of poly-Si grain size with pulse energy is very strong, particularly near the grain size peak. The sharp drop-off in grain size seen with the transition above full-melt necessitates the process be designed to use an energy below the full-melt threshold by an amount related to the pulse energy fluctuation, to ensure that pulse energy never passes the threshold. Thus the maximum performance which can be achieved in a laser annealing process is related to the total pulse energy variation. Any efforts to reduce this variation will contribute directly to forming higher performance silicon films and devices.

A second reason to look into a replacement for excimer laser systems is the complexity and cost of maintaining one. Excimer lasers require a halogen gas supply, typically either

chorine or fluorine. These gases are highly corrosive, requiring expensive plumbing and careful handling. Over time they degrade the laser parts, requiring regular maintenance to keep the laser functioning optimally. The concentration of active gas species in the chamber decays as the laser is run, causing the pulse energy to change over time and requiring frequent fills of fresh gas.

A promising solution to both of these problems is the use of a copper vapor laser to replace the excimer laser. Copper vapor lasers use a tube filled with an inert carrier gas, typically neon, and a solid source of copper. The copper is heated and vaporizes to provide the active species for the laser discharge. Partial pressure of active species is determined by the vapor pressure of copper at the heater temperature, for typical tools this temperature is approximately 1500 °C. Concentration of species in the chamber can therefore be maintained simply by keeping the heater temperature constant. The only gas which needs to be supplied to the tool is the inert carrier gas, and the copper source only needs to be changed when the entire solid source has been vaporized.

There are several well known techniques to engineer a consistent and stable electron density in a copper vapor laser tube during operation [3, 4]. By utilizing these techniques in combination with novel discharge circuit design [5, 6], lasers with extremely good pulse energy stability can be produced. The copper vapor laser used in this work has a total pulse energy fluctuation of ±0.8 % [7]. Its extremely small energy fluctuation should enable the design of a very high performance laser annealing process with good device to device uniformity.

Copper vapor lasers emit light in the visible range, at 510 nm ($\Rightarrow$ 2.44 eV) and 578 nm ($\Rightarrow$ 2.15 eV), in an approximate ratio of 2:1. According to Fig. 4.1, the absorption coefficient of amorphous silicon in this range is $1 \times 10^5\,\mathrm{cm}^{-1}$, leading to a penetration depth of 100 nm. This is in contrast with crystalline silicon, which has an absorption coefficient at 2 eV of $1 \times 10^4\,\mathrm{cm}^{-1}$, indicating it absorbs the laser light considerably less efficiently. A penetration depth of 100 nm is twice the typical TFT film thickness of 50 nm; so approximately half of the laser energy will be absorbed into the silicon film, while half will pass through to the

substrate. Typical low-cost substrate materials are transparent to visible wavelengths, so damage from the transmitted laser light will not be a concern [8].

There has been a small amount of research demonstrating the feasibility of crystallization of amorphous silicon with a copper vapor laser [9], primarily for thin-film photovoltaic applications. This work seeks to demonstrate comparable electronic properties of copper vapor laser annealed silicon and excimer laser annealed silicon by fabrication of thin-film transistors.

4.2 Process Flow

In order to best measure the electrical properties of the laser annealed silicon films, a high-performance glass-compatible poly-Si TFT process was designed. Unlike the processes used in Chapter 2 and Chapter 3, there were no laser annealing steps used other than the crystallization step. This necessitates the use of a 600 °C furnace activation step, and therefore use of a higher temperature compatible gate material than the Al used previously. An annealed LPCVD gate SiO_2 layer was used in order to ensure that device performance was not limited by interface defects.

Self-aligned top-gate TFTs were fabricated on oxidized silicon wafer substrates as follows. A 1 μm thick layer of SiO_2 was deposited by LPCVD onto the Si wafer, followed by a 50 nm layer of Si deposited by DC sputtering at room temperature. Laser annealing was performed with an XeCl excimer laser on one wafer and with a copper vapor laser on a separate wafer. Excimer laser annealing was performed with three pulses at 300 mJ/cm^2, 320 mJ/cm^2, 340 mJ/cm^2, and 360 mJ/cm^2, in separate regions on the wafer, to investigate the performance variation around the measured full melt threshold of 340 mJ/cm^2. Copper vapor laser annealing was performed with three pulses at different fluences in separate regions on the wafer, as described in Table 4.1. The regions are referred to by the maximum pulse fluence used, as that pulse will have the most impact on the grain structure of the

Table 4.1. Copper Vapor Laser Annealing Schedule

Region	Shot 1 mJ/cm^2	Shot 2 mJ/cm^2	Shot 3 mJ/cm^2
350	300	350	350
400	300	400	400
450	300	450	400
500	300	500	400

film. Higher fluences were used in the copper vapor laser annealing process to account for the lower absorption at the longer wavelength.

The annealed poly-Si films were patterned and dry etched to form TFT active regions, and a 50 nm gate SiO_2 layer was deposited by LPCVD at 450 °C. The wafers were then annealed for 4 hours at 600 °C to densify the SiO_2 layer and improve the interface quality. A Mo gate layer was deposited by DC sputtering at 300 °C, patterned, and dry etched. SiO_2 gate-sidewall spacers 50 nm thick were then formed by LPCVD at 400 °C and anisotropic dry etching. Heavy n-type doping of the source and drain regions was accomplished with phosphorus ion implantation at a dose of 1×10^{15} ions/cm^2 and energy of 30 keV.

Next, a 150 nm SiO_2 insulation layer was deposited by LPCVD at 400 °C. A second 4 hour 600 °C annealing step was performed to densify the insulation oxide layer and to activate the n-type source and drain implant. It is essential that the implant activation anneal occur after the insulation layer deposition in order to protect the highly brittle Mo gate layer from cracking and flaking off of the wafer during the high temperature step. To complete the device fabrication, contact holes were patterned and dry etched, and a 700 nm Al/2% Si layer was deposited by DC sputtering, patterned, and wet etched. An anneal was then performed at 450 °C in N_2 / 10 % H_2 to ensure formation of low-resistance contacts to source and drain.

After testing, a 2 hour, 350 °C plasma hydrogenation step was performed, in order to investigate the relative performance of devices after a defect reduction process.

Table 4.2. Measured Performance for Unpassivated Excimer Laser Annealed and Copper Vapor Laser Annealed Devices.

Device	I_{min} pA	I_{max} μA	μ_{eff} cm^2/V·s	V_T V	S V/dec
ELA - 300 mJ/cm^2	14.3	393	72.0	1.094	0.331
ELA - 320 mJ/cm^2	5.21	507	89.1	0.569	0.261
ELA - 340 mJ/cm^2	5.00	244	39.7	4.005	0.776
ELA - 360 mJ/cm^2	3.39	196	31.6	5.007	0.747
CVLA - 350 mJ/cm^2	3.57	102	33.7	2.50	0.528
CVLA - 400 mJ/cm^2	3.39	547	86.7	1.722	0.417
CVLA - 450 mJ/cm^2	3.28	306	52.8	2.412	0.490
CVLA - 500 mJ/cm^2	5.75	303	47.4	2.577	0.522

4.3 Device Results

In order to gain a feeling for the sensitivity of the excimer laser annealing and copper vapor laser annealing processes to variations in laser annealing fluence, it is instructive to examine both the variation within a given laser condition and the variation between the different annealing conditions. Data for the different laser conditions before and after hydrogen plasma annealing is presented below.

4.3.1 Unpassivated Devices

Transfer curves for typical excimer laser annealed devices from each of the four annealing conditions are shown in Fig. 4.2. Extracted parameters for devices processed under the different conditions before passivation are shown in Table 4.2, taken as the average measured value for 5 devices processed under the same conditions. All devices shown in this chapter are W/L = 50 μm/5 μm, and measurements were taken with V_{DS} = 5 V. Parameters were extracted as described in section 2.5. The excimer laser annealed devices show a wide variation between the different laser conditions, despite the small fluence step size of 20 mJ/cm^2 and total difference in fluence of 60 mJ/cm^2. In particular, examining the average threshold voltage of measured devices in each laser condition, the 300 mJ/cm^2 and

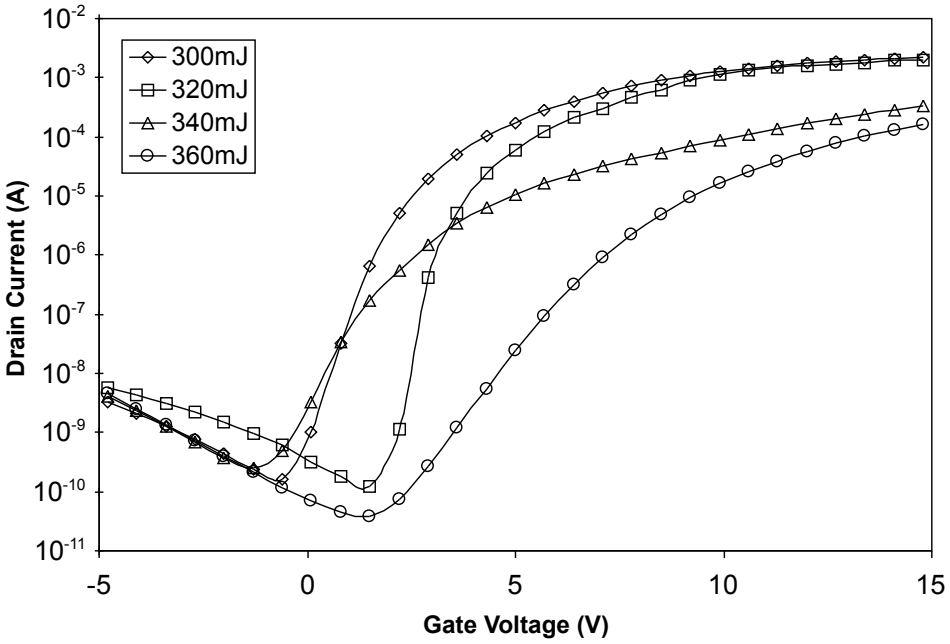

Figure 4.2. Typical TFT performance for silicon films crystallized by excimer laser annealing at 300 mJ/cm^2 to 360 mJ/cm^2, before hydrogen plasma passivation.

320 mJ/cm^2 have average V_T of 1.1 V and 0.57 V, respectively, while the devices annealed at 340 mJ/cm^2 and 360 mJ/cm^2 have average V_T of 4.0 V and 5.0 V. Average measured mobility is nearly factor of 2 higher in devices annealed at the lower two laser fluences compared with the higher two. The reason for this large variation is that the laser fluences used were chosen to be at the steepest part of the curve of grain size vs. fluence [10], in the range from immediately below the full melt threshold to immediately above the full melt threshold.

Variation within a given laser condition for the excimer laser annealed devices was also seen to be very large. Transfer curves for four typical devices annealed at 300 mJ/cm^2 are seen in Fig. 4.3, devices were chosen to show the entire range of variation observed. The total measured variation in threshold voltage in each of the four regions is greater than 5 volts, and the 360 mJ/cm^2 annealed devices are seen to have mobility as high as 91 $\frac{\text{cm}^2}{\text{V·s}}$ and as low as 8 $\frac{\text{cm}^2}{\text{V·s}}$. Only the devices annealed at 300 mJ/cm^2 have consistent device performance, with device mobility measured in the range of 45 $\frac{\text{cm}^2}{\text{V·s}}$ to 87 $\frac{\text{cm}^2}{\text{V·s}}$, though, the large variation in threshold would still present a challenge to the utilization of these devices

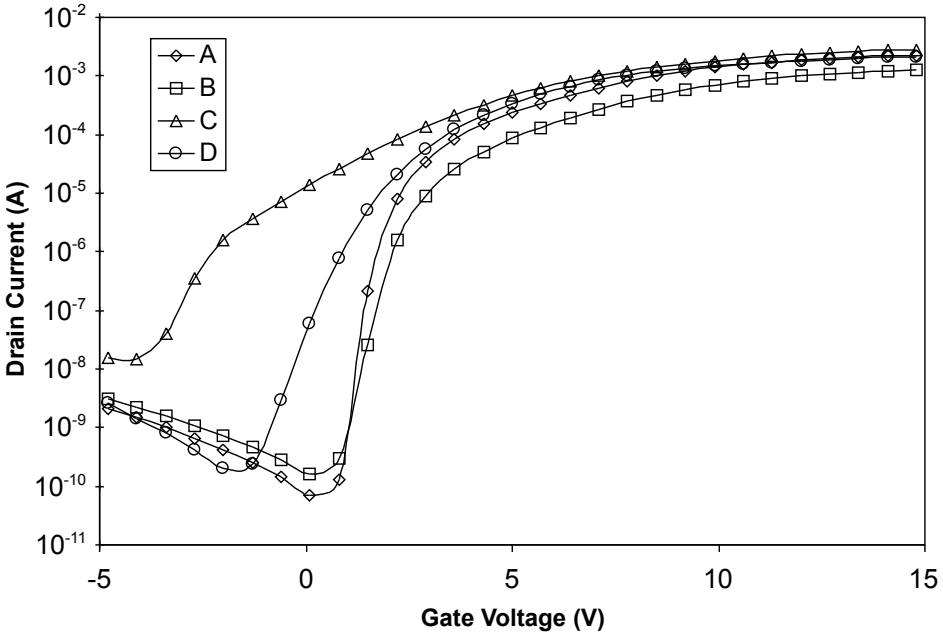

Figure 4.3. TFT performance for four devices crystallized by excimer laser annealing at $300\,\mathrm{mJ/cm^2}$, before hydrogen plasma passivation. Curves were chosen to represent the entire range of variation seen.

in a display. This minimal level of consistency between devices is only achieved by reducing the nominal laser annealing fluence away from the full melt threshold, reducing the peak device performance.

Transfer curves for typical devices annealed with a copper vapor laser are shown in Fig. 4.4. Mobility variation between the four laser annealing conditions is seen to be comparable to the excimer laser annealed devices, indicating that the relationship between laser fluence and grain size in the range of laser fluences used is similar for the two processes. However, the different conditions are much more consistent in threshold voltage and subthreshold slope. The variation in average V_T is only $0.6\,\mathrm{V}$ between the different laser conditions, and the average subthreshold slope varies by only $0.06\,\mathrm{V/decade}$. In contrast, the excimer laser annealed devices have a V_T variation of $5.5\,\mathrm{V}$ and a subthreshold slope variation of $0.44\,\mathrm{V/decade}$ across the different laser annealing conditions. The strong similarity between the devices annealed at different copper vapor laser fluences indicates

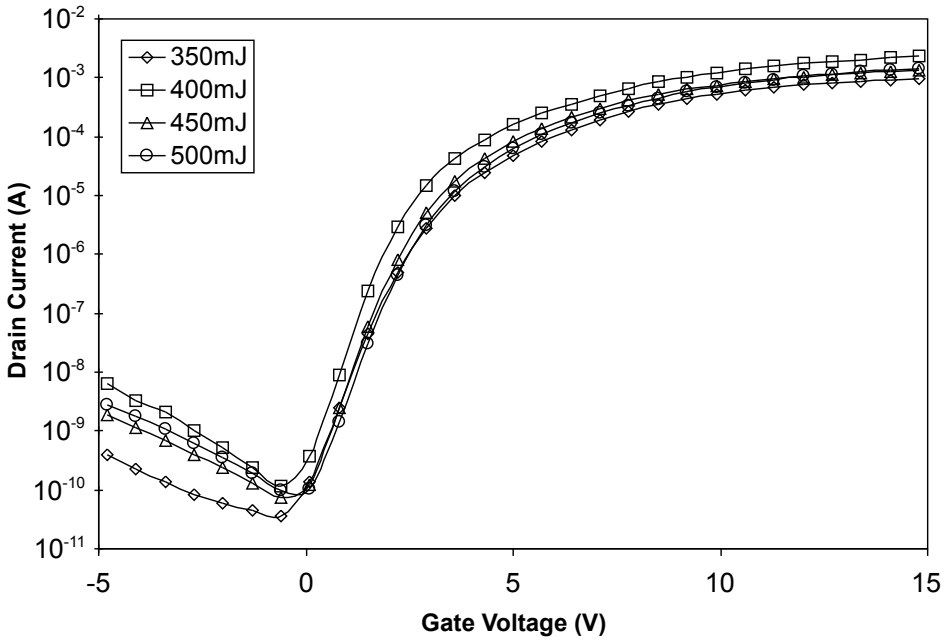

Figure 4.4. Typical TFT performance for silicon films crystallized by copper vapor laser annealing at 350 mJ/cm^2 to 500 mJ/cm^2, before hydrogen plasma passivation.

that process uniformity for a copper vapor laser process should be much better than for an excimer laser process, even given lasers of comparable pulse energy uniformity.

Examining multiple devices annealed under the same conditions reveals that uniformity is much improved over the excimer laser annealed devices. Transfer curves for devices annealed at 400 mJ/cm^2 are shown in Fig. 4.5. Mobility variation within a given region is approximately a factor of 2 between the lowest and the highest, again similar to the excimer laser annealed devices. However, total variation of threshold voltage is only approximately 0.2 V within each region, and subthreshold slope varies by only 0.1 V/decade.

Given the similarities in mobility between the excimer laser annealed devices and the copper vapor laser annealed devices, it is likely that the poly-Si grain size and variation are comparable between the two processes. However, threshold voltage and subthreshold slope are much more uniform in the copper vapor laser annealed devices than the excimer laser annealed devices, indicating that formation of dangling bond related midgap states is much more uniform in the copper vapor laser annealing process. Relative performance

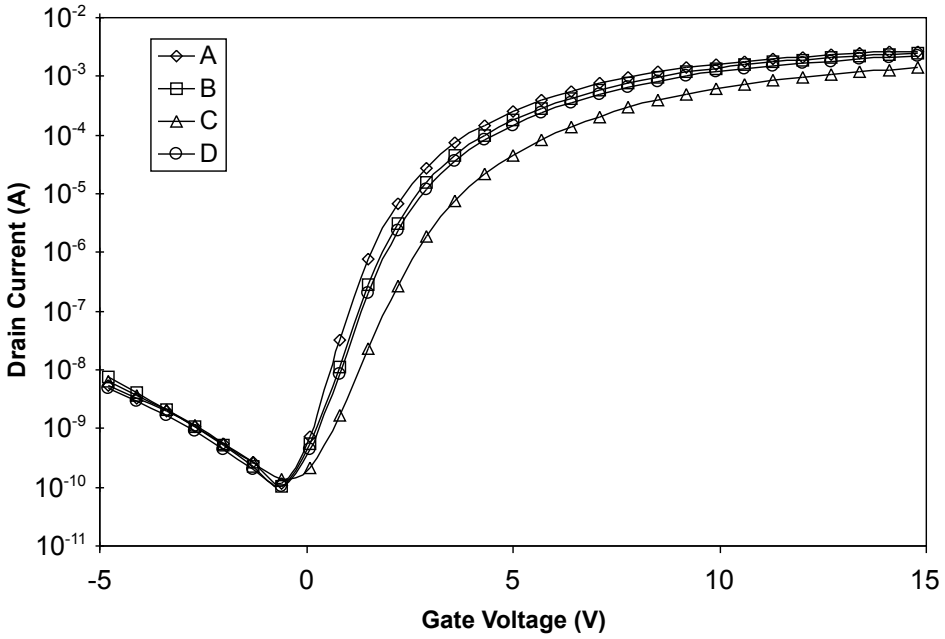

Figure 4.5. TFT performance for four devices crystallized by copper vapor laser annealing at 400 mJ/cm^2, before hydrogen plasma passivation. Curves were chosen to represent the entire range of variation seen.

after these defects have been made electrically inactive can be evaluated by performing a hydrogen plasma annealing process on the devices.

4.3.2 Passivated Devices

A hydrogen plasma passivation process was performed in a parallel-plate plasma reactor at 350 °C in 50% H_2 and 50% Ar at a power density of 0.2 W/cm^2. Transfer curves for passivated devices annealed by excimer laser are shown in Fig. 4.6 and for passivated devices annealed by copper vapor laser in Fig. 4.7. Device extracted parameters after passivation are shown in Table 4.3. As expected, turn-on characteristics have greatly improved and the different laser annealing conditions have become much more similar, as a large fraction of the dangling bond defects have been made electrically neutral.

Mobility of all devices has improved somewhat, but there is still wide spread in mobility between the different laser conditions. Defect reduction improves mobility due to the removal of strain-bond shallow states [11]; however, physical scattering at grain boundaries

Table 4.3. Measured Performance for Passivated Excimer Laser Annealed and Copper Vapor Laser Annealed Devices.

Device	I_{min}	I_{max}	μ_{eff}	V_T	S
	pA	μA	$cm^2/V{\cdot}s$	V	V/dec
ELA - 300 mJ/cm^2	11.7	565	133.6	0.774	0.156
ELA - 320 mJ/cm^2	11.3	544	105.5	1.057	0.150
ELA - 340 mJ/cm^2	12.8	493	81.2	1.291	0.191
ELA - 360 mJ/cm^2	14.8	123	10.7	2.111	0.274
CVLA - 350 mJ/cm^2	7.18	103	36.5	0.985	0.264
CVLA - 400 mJ/cm^2	2.30	667	110.5	0.704	0.230
CVLA - 450 mJ/cm^2	3.28	306	52.8	2.412	0.490
CVLA - 500 mJ/cm^2	5.75	303	47.44	2.577	0.522

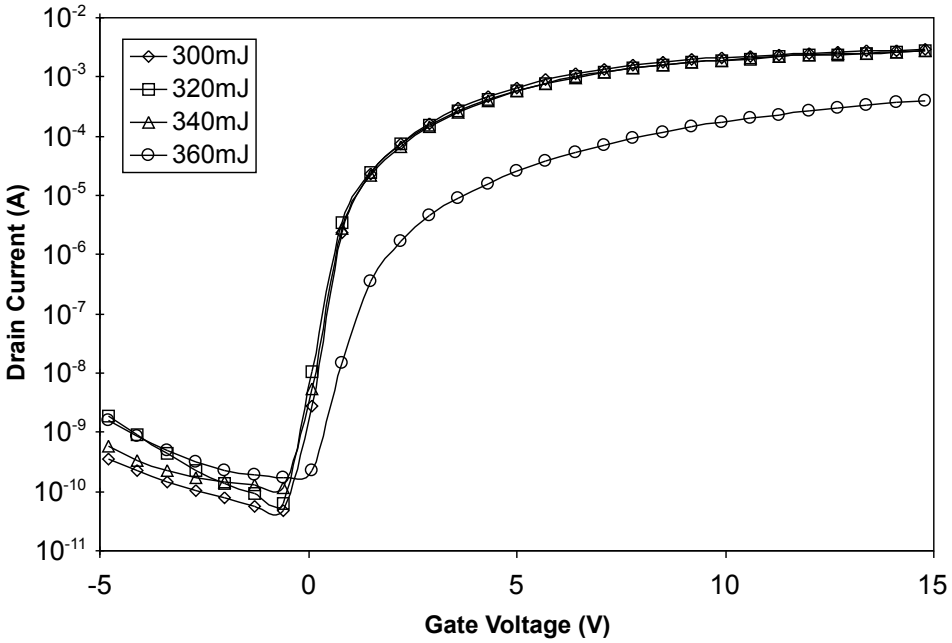

Figure 4.6. Typical TFT performance for silicon films crystallized by excimer laser annealing at 300 mJ/cm^2 to 360 mJ/cm^2, after hydrogen plasma passivation.

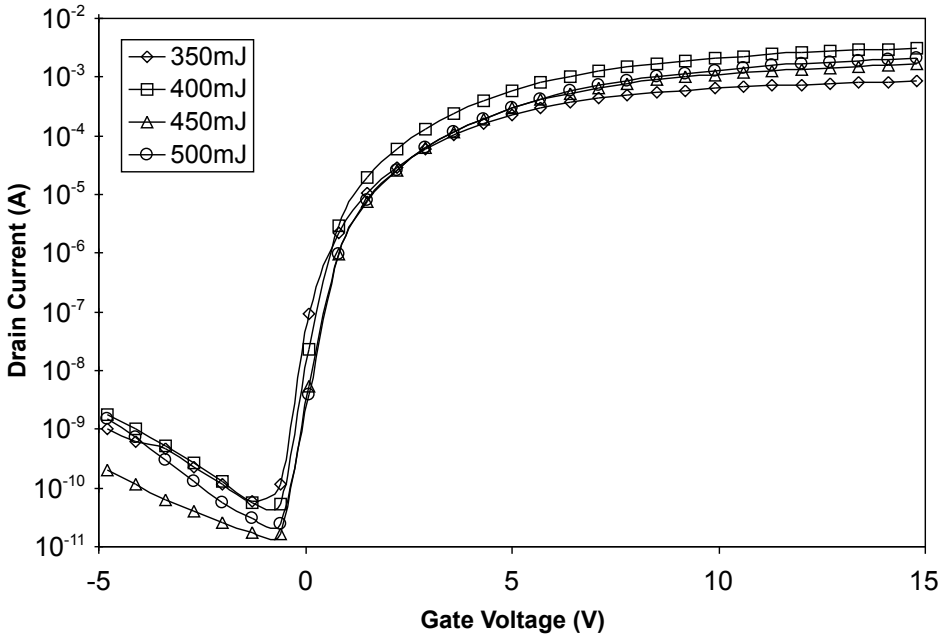

Figure 4.7. Typical TFT performance for silicon films crystallized by copper vapor laser annealing at 350 mJ/cm^2 to 500 mJ/cm^2, after hydrogen plasma passivation.

will cause a reduction in mobility even if all electrical defects are removed. Thus, evaluating variation in mobility in passivated devices can yield information about uniformity of poly-Si grain-growth independent of the density of dangling bonds formed during the laser annealing process.

Transfer curves for typical passivated devices annealed by excimer laser at 300 mJ/cm^2 are shown in Fig. 4.8 and for typical passivated devices annealed by copper vapor laser at 400 mJ/cm^2 in Fig. 4.9. These laser annealing conditions had the highest average performance and smallest variation between devices, and the device curves shown were chosen to represent the full range of device performance observed. Both sets of device results show good uniformity in the passivated devices, with similar spread of measured mobility. Observed spread in turn-on characteristics appears similar between the two sets of devices, though the overall shape of the transfer curves of the copper vapor laser annealed devices is more consistent than that for the excimer laser annealed devices. To gain a more quantitative measurement of the performance variation in these two groups of devices, 15 devices from each group were measured and statistics calculated. Average value

Table 4.4. Statistics before and after hydrogen plasma passivation for 15 devices annealed by excimer laser at $300\,\mathrm{mJ/cm^2}$ and for 15 devices annealed by copper vapor laser at $400\,\mathrm{mJ/cm^2}$.

Device	I_{min} pA	I_{max} μA	μ_{eff} $cm^2/V{\cdot}s$	V_T V	S V/dec
ELA - unpass - $\bar{x}$	14.3	393	72.0	1.094	0.331
ELA - unpass - σ	29.1	88.2	11.0	1.606	0.106
CVLA - unpass - $\bar{x}$	4.50	486	75.7	1.982	0.469
CVLA - unpass - σ	1.44	74.8	13.4	0.322	0.058
ELA - pass - $\bar{x}$	5.12	470	104.2	0.545	0.159
ELA - pass - σ	1.81	79.3	14.5	0.233	0.007
CVLA - pass - $\bar{x}$	2.54	622	102.0	0.717	0.219
CVLA - pass - σ	0.780	82.7	16.4	0.152	0.020

and standard deviation of extracted parameters for devices annealed by excimer laser at $300\,\mathrm{mJ/cm^2}$ and annealed by copper vapor laser at $400\,\mathrm{mJ/cm^2}$ before and after passivation are shown in Table 4.4.

Before hydrogenation, average turn-on characteristics of the excimer laser annealed devices were better than the copper vapor annealed devices, despite having a much larger spread. This indicates that, on average, there are a smaller number of dangling bond defects in the excimer laser annealed devices. Turn-on characteristics of passivated devices remain better for the excimer annealed devices; and in addition, since there were a smaller number of defects to passivate, the variation between passivated excimer laser annealed devices is smaller than the variation between passivated copper vapor laser annealed devices, as the devices are all closer to completely passivated. Mobility and variation in mobility are nearly identical for the two laser annealing processes, indicating that the physical grain structure is very similar.

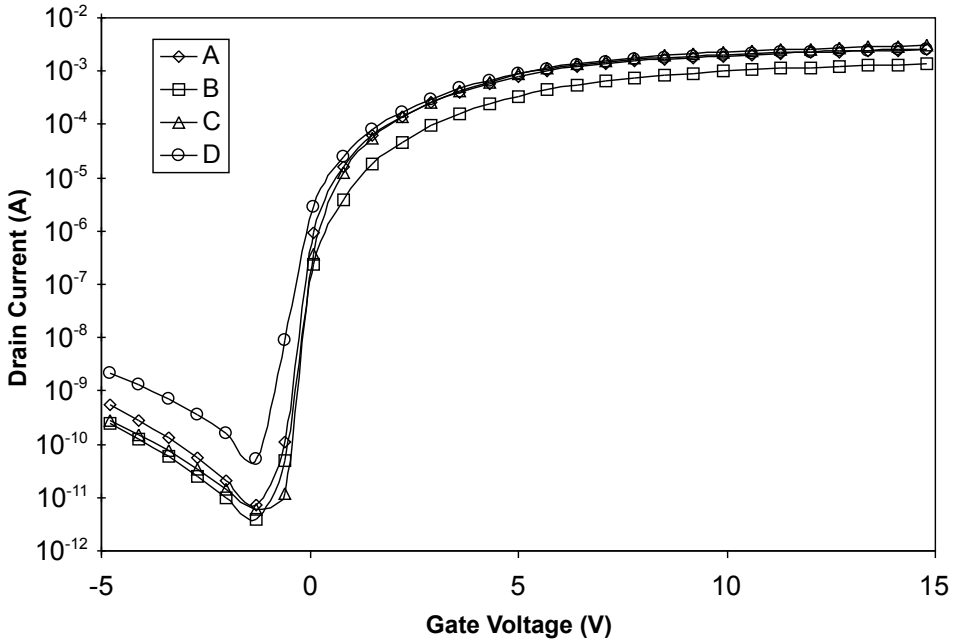

Figure 4.8. TFT performance for four devices crystallized by excimer laser annealing at $300\,\mathrm{mJ/cm^2}$, after hydrogen plasma passivation. Curves were chosen to represent the entire range of variation seen.

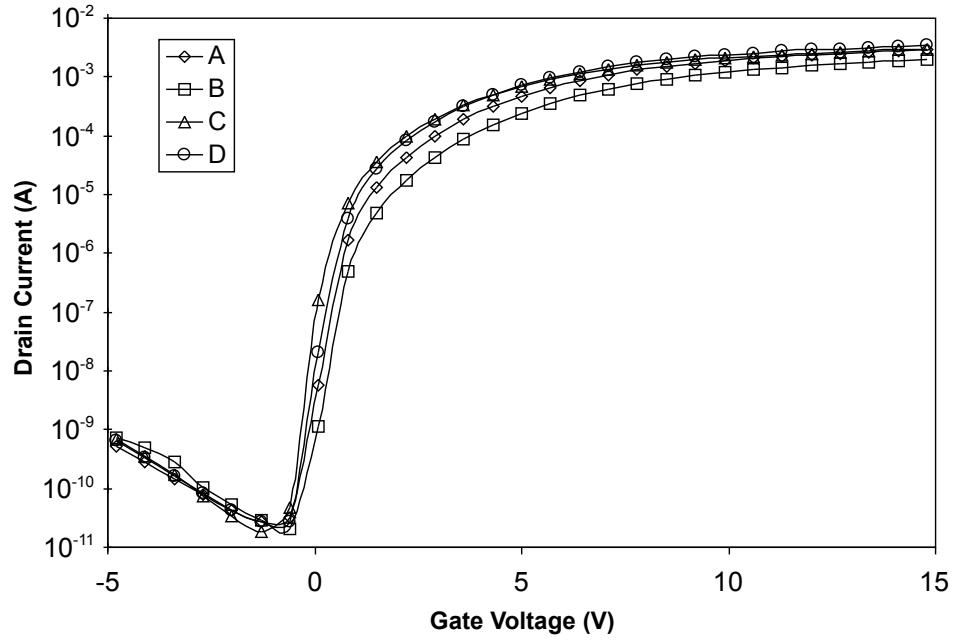

Figure 4.9. TFT performance for four devices crystallized by copper vapor laser annealing at $400\,\mathrm{mJ/cm^2}$, after hydrogen plasma passivation. Curves were chosen to represent the entire range of variation seen.

4.4 Summary

Formation of poly-Si films for thin film transistors by copper vapor annealing has been shown. Absorption of light emitted by copper vapor laser is good, despite its relatively long wavelength, due to the higher absorption of amorphous silicon at low photon energies compared with crystalline silicon. High performance devices were formed, with similar grain structure to devices crystallized by conventional excimer laser annealing. Before a hydrogen plasma passivation treatment, device uniformity was seen to far exceed that of excimer laser. This has potential applications to plastic-compatible devices, where improving uniformity through a passivation treatment is very difficult.

After a hydrogen plasma passivation treatment, device performance and uniformity of excimer laser annealed devices was slightly superior to that of the copper vapor laser annealed devices, though both were very good. The data suggest that annealing with copper vapor laser forms silicon films with slightly higher average defect density, but much lower defect density variation. Measured TFT mobility of devices formed by the two processes were very similar, suggesting formation of films with similar grain structure.

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Chapter 5

Conclusions

5.1 Summary

Flat panel display technology has been advancing very rapidly in recent years. Liquid crystal displays have the advantage over other currently established display technologies of leveraging semiconductor manufacturing technology and its rapid exponential growth. As display manufacturing becomes cheaper, new applications open up, putting displays in more and more places. Flexible flat panel technology will drive costs down further yet, as manufacturing on plates transitions to manufacturing on rolls. At the same time, it will enable an entire new set of applications that demand flexible or robust displays. In order for flexible flat panel display technology to become a reality, novel processes need to be established to bring devices compatible with inexpensive flexible substrates to the level of performance, uniformity, and reliability which is necessary for a usable product.

Plastic compatible processes to fabricate high performance thin-film transistors are well-established, largely thanks to the success of excimer laser annealing and high-density plasma chemical vapor deposition. These techniques share the idea of selectively adding energy to a deposited film, allowing it to proceed towards thermodynamic equilibrium without raising the substrate temperature above acceptable limits. Utilization of novel techniques like

these is necessary to form devices made from high-quality deposited films on a low-cost, low thermal budget substrate.

Low temperature processing typically forms silicon films containing a large number of easily-broken bonds, contributing to poor reliability of the devices with electrical stress. Reliability is typically improved by high-temperature annealing, not available in a plastic-compatible process. Even when formed in a higher temperature glass-compatible process, poly-Si films have a large number of defects, hurting performance and device to device uniformity. The established process for defect passivation is hydrogen plasma annealing, which is also not available in a plastic compatible process. This dissertation investigated several novel techniques to improve uniformity and reliability of plastic compatible thin film transistors, seeking alternatives to hydrogen plasma annealing, high-density plasma chemical vapor deposition, and excimer laser annealing. A summary of these techniques and their results is presented in the next section.

5.2 Contributions

The first technique investigated was defect passivation by ion implantation and pulsed laser annealing. Selective heating by excimer laser annealing was utilized to activate an implanted impurity species to passivate dangling bond defects at grain boundaries. This process occurs during crystallization of the amorphous silicon film, avoiding the need for any extra annealing steps. Defect passivation comparable to conventional hydrogen plasma annealing was observed with nitrogen, oxygen, or fluorine in a 450 °C maximum temperature process, with the N implant having the best performance.

When the technique was incorporated into a plastic compatible process, defect passivation was observed with oxygen or fluorine. Combined with a second laser annealing step after gate oxide deposition, it was additionally shown to reduce defects at the $Si-SiO_2$ interface. Device reliability to electrical stress was shown to be improved over control devices in the plastic compatible process and further improved with a non-melt laser annealing step

after crystallization. The best performance and reliability in the experiment was seen with the F implanted devices. Devices implanted with N were seen to have degraded performance, unlike in the earlier higher temperature experiment, due to its formation of a deep-level trap state, which is deactivated at 400 °C or above.

A 150 °C reactively sputtered SiO_2 process was established. A gate oxide layer fabricated with this process shows acceptable MOS C-V characteristics but was found to severely limit mobility of devices formed. Device performance was sufficient for demonstration of defect passivation in a plastic compatible process but would not be usable for high performance logic. The sputtering process incorporated two techniques for damage reduction at the $Si-SiO_2$ interface, the use of a photooxidation process to form a good quality interfacial SiO_2 layer and the use of a plasma charge trap to avoid damage caused by high energy plasma species during sputtering. This was a novel method for gate oxide deposition and is worthy of further investigation towards the formation of a high quality interface.

Copper vapor laser annealing was established as an alternative to excimer laser annealing for the formation of high-quality poly-Si films. This technique holds promise due to the high pulse energy uniformity possible with a copper vapor laser. High quality devices were formed, with mobility comparable to devices formed with films crystallized by excimer laser, showing that the longer wavelength light is acceptable for silicon crystallization. Device uniformity without any defect reduction process was seen to be far superior for copper vapor laser crystallized devices compared to ones crystallized by excimer laser. The high uniformity of defects formed in films crystallized by copper vapor laser annealing makes this laser annealing process attractive for plastic compatible devices where device uniformity is necessary but defect reduction is very difficult.

Finally, several different thin-film transistor processes have been established and characterized in the UC Berkeley Microlab. A high-performance process has been documented, utilizing several 600 °C annealing steps to reduce defects while maintaining compatibility with conventional display glass. This process used a LPCVD gate oxide layer and furnace annealed source and drain regions. The defect reduction effect of a

long 600 °C anneal after silicon crystallization has been shown. A 450 °C process with very good performance has been shown by removing all 600 °C steps from the previous process and using laser annealing to activate source and drain dopants. A 150 °C plastic compatible process has additionally been shown, replacing LPCVD gate oxide deposition with the reactively sputtered gate oxide. This process could easily be adapted to use an ECR PECVD gate oxide to form high-performance devices [1]

5.3 Recommendations for Future Work

Several novel thin-film transistor processes have been demonstrated in this dissertation, and there exist many opportunities for further development of these processes. Each process needs further investigation of interactions between the process parameters and the fabricated material properties. Learning more about these interactions will allow process optimization and formation of the best quality films. Additionally, further work is necessary to simplify integration of these novel processes into a standard thin film transistor process.

5.3.1 Defect Passivation by Ion Implantation and Pulsed-Laser Annealing

Due to the large number of experimental splits in this investigation, it was not possible to investigate the effect of implant dose on defect passivation and reliability of fabricated devices. This investigation will be necessary for the fabrication of high-performance devices and will also yield useful information about the mechanics of the passivation process and defect density in the film.

Materials characterization of implanted and annealed films will complete the picture of the defect passivation process. SIMS measurements can tell us about impurity redistribution in the film during laser annealing, to establish how much of the impurity is pushed out to the grain boundaries during formation and how much is left in the grains for possible passivation of intra-grain defects. Measurements of grain size versus implant dose and laser annealing energy can provide insight into how grain growth is affected by impurity

concentration, perhaps enabling growth of larger grains in addition to defect passivation. For instance, it has been suggested that presence of oxygen impurities silicon films during laser crystallization can slow cooling and enhance grain formation [2].

This passivation process makes only a small modification of the conventional excimer laser annealed thin-film transistor process, the addition of an ion implantation step. However, it would be worthwhile to investigate if the ion implantation step could be removed as well. It is possible to incorporate the passivation impurities in-situ during silicon sputter deposition either by adding the impurity to the sputtering gas or to the sputter target. Addition of the impurity into the sputter gas has the advantage of allowing different experimental process conditions to achieve different concentrations in the sputtered film. However, the final incorporated concentration will not be known until characterization is performed, and there may be problems with uniformity of impurity concentration across the wafer, as was seen in the SiO_2 reactive sputtering process at low oxygen partial pressure. Addition of impurities to the target solves both of those problems, as the incorporated impurity concentration and uniformity should be the same in the film and in the target. This method requires that the impurity concentration be decided upon in advance and is not modifiable once the target is formed; so it would be more applicable to a manufacturing process.

Finally, it would be worthwhile to investigate if passivation of interface defects through gate oxide annealing could be achieved without adding an extra annealing step to the standard process. This could be achieved by combining the anneal with the source and drain activation anneal. In the standard process, the implant and anneal are masked by the aluminum gate line. The channel region must still be masked from the heavy implant, but then exposed to the laser light. A simple way to accomplish this would be masking the implant with photoresist, then removing it and performing laser annealing. This process adds an extra mask and causes the gate line to no longer be self-aligned to the source and drain regions. A second way is by using a gate material which will absorb the implant but is transparent to laser light. Common transparent conductive oxides such as indium tin

oxide or zinc tin oxide have moderate absorption of light at excimer wavelengths but are transparent to visible light [3]. In a process with a transparent conducting oxide gate line, the copper vapor laser could be used for source and drain activation and oxide annealing in a single laser step.

5.3.2 Reactive Sputtering of Silicon Dioxide

More research is needed to determine if there is a set of processing conditions for the reactively sputtered gate dielectric process which will produce a high quality interface. Good quality sputtered dielectric layers have been formed by RF sputtering of silicon dioxide, so it is likely that it is possible by reactive sputtering as well. Since it has been observed that acceptable CV characteristics do not necessarily lead to good interface performance, it will be necessary to perform process qualification runs with a complete TFT process rather than by simply fabricating MOS capacitors on bare silicon wafers. It is possible that a longer UV photooxidation treatment, lower power silicon sputtering, or higher oxygen partial pressure could yield a better quality interface.

Additionally, enhancement of performance and reliability have been shown by incorporation of fluorine into the gate dielectric layer [4]. This is likely the same effect which was observed in this work in devices which had implant passivation and laser oxide annealing. Better fluorine incorporation may be possible if the oxide were doped in-situ during deposition, by one of the methods described in section 5.3.1.

5.3.3 Silicon Crystallization by Copper Vapor Laser Annealing

Silicon films crystallized by copper vapor laser annealing were seen to have similar grain structure and TFT mobility to films crystallized by excimer laser annealing. However, it is not clear if the melting and crystal growth processes are the same as those which occur during excimer laser annealing. Most useful to the development of a high-performance copper vapor laser annealing process would be the construction a curve of the form of

Fig. 1.6, showing average poly-Si grain size versus laser annealing fluence. From the data seen in Chapter 4 we would expect it to have a shallow slope and smoother fall-off after the full melt threshold is crossed. If this is indeed the case, the process could be designed to anneal films at the laser fluence yielding the peak grain size, without the wide performance variation seen in a similarly designed excimer laser annealing process.

5.4 References

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