Evolutionary MOSFET Structure and Channel Design for Nanoscale CMOS Technology

by

Byron Ho

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Committee in charge:

Professor Tsu-Jae King Liu, Chair
Professor Oscar Dubon
Professor Vivek Subramanian
Professor Ming Wu

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Abstract

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The constant pace of CMOS technology scaling has enabled continuous improvement in integrated-circuit cost and functionality, generating a new paradigm shift towards mobile computing. However, as the MOSFET dimensions are scaled below 30nm, electrostatic integrity and device variability become harder to control, degrading circuit performance. In order to overcome these issues, device engineers have started transitioning from the conventional planar bulk MOSFET toward *revolutionary* thin-body transistor structures such as the FinFET or fully-depleted silicon-on-insulator (FDSOI) MOSFET. While these alternatives appear to be elegant solutions, they require increased process complexity and/or more expensive starting substrates, making development and manufacturing costs a concern.

For certain applications (such as mobile electronics), cost is still an important factor, inhibiting the quick adoption of the FinFET and FDSOI MOSFET structures while providing an opportunity to extend the competitiveness of planar bulk-silicon CMOS. A segmented-channel MOSFET (SegFET) design, which combines the benefits of both planar bulk MOSFETs (*i.e.* lower process complexity and/or cost) and thin-body transistor structures (*i.e.* improved electrostatic integrity), can provide an *evolutionary* pathway to enable the continued scaling of planar bulk technology below 20nm. In this work, experimental results comparing SegFETs and planar MOSFETs show suppressed short-channel effects and comparable on-state current (despite halving the effective device width). In addition, three-dimensional device simulations were used to optimize and benchmark the bulk SegFET and FinFET designs. Compared to the FinFET design, the results indicate that the SegFET can achieve similar on-state current performance and intrinsic delay (for the same channel stripe pitch) at a lower height/width aspect ratio and less aggressive retrograde channel doping gradient for improved manufacturability, making it a promising candidate for continued bulk-silicon CMOS transistor scaling.

High-mobility channels are also investigated in this work for their potential to improve MOSFET performance, but issues with physical material parameters (electrostatic control, strain

effects, etc.) and process integration necessitate careful design when implementing these materials in the MOSFET channel regions. Because germanium (Ge) and silicon-germanium ($Si_{1-x}Ge_x$) alloys are Group IV materials like silicon (Si), and since these materials are already extensively used in mainstream volume integrated-circuit manufacturing, they represent the most straightforward path to integrating high-mobility channels on silicon. Device simulations are used to optimize $Si_{1-x}Ge_x$ channel thickness and Ge concentration for $Si_{1-x}Ge_x$/Si heterostructure p-channel MOSFETs; it is found that a thin (< 5 nm) channel with moderate (20% - 40%) Ge concentration is optimal for device performance and manufacturability. $Si_{1-x}Ge_x$/Si heterostructure channels were also experimentally integrated in SegFETs and show 30% higher on-state current (for an off-state current of 10 nA/μm) and reduced layout-width dependencies as compared to the planar MOSFET counterpart. Finally, Monte Carlo simulations were used to compare the scalability and performance of pure Ge and Si double-gate structures at short gate lengths (< 20 nm). Due to the higher dielectric constant and low transport mass (which becomes lighter with added strain), pure Ge channels may not be attractive for ultra-short gate lengths (8 nm) because of reduced electrostatic control and increased direct source-to-drain tunneling. However, if gate length scaling slows dramatically or channel strain decreases with shrinking device pitch, then Ge channels can be a viable alternative to Si for high-performance applications.

To my family, for their limitless support

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Acknowledgements

The body of work that comprises a Ph.D is never completed in isolation. This work is no different, and I owe many thanks to many people.

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Chapter 1

Introduction

1.1 A Short Historical Perspective of Transistor Development

The development of modern electronics, which began with the invention of the solid-state transistor in 1947, is an excellent example of human ingenuity, motivation, and perseverance. The pace of transistor improvement has been astounding; for instance, the cost of one transistor has decreased from the order of one dollar in 1978 to the order of a tens of nanodollars today (Fig. 1.1) [1] while its size has steadily shrunk to the point where more than 300 million transistors can fit on the head of a pin (pin radius = 1mm, transistor length = width = 100nm).

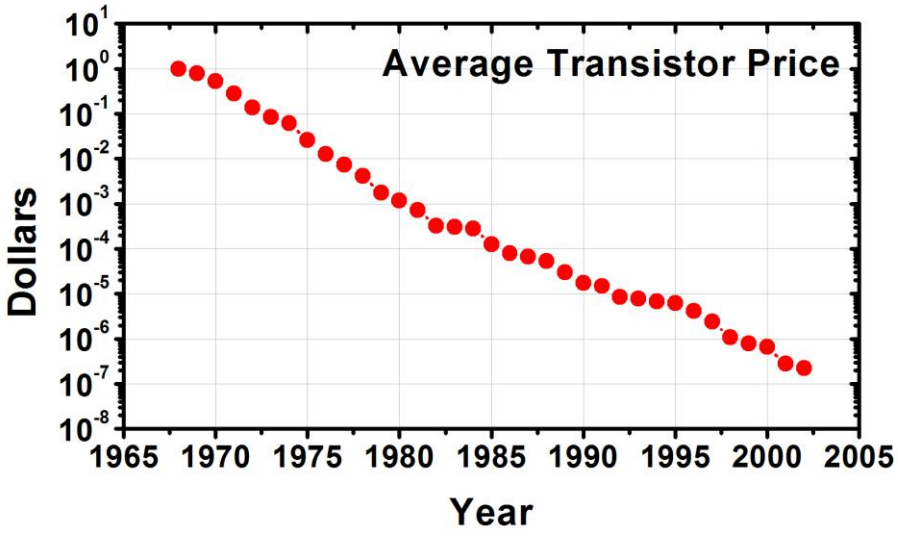

Fig. 1.1. Average transistor price from 1968 to 2002. Adapted from [1].

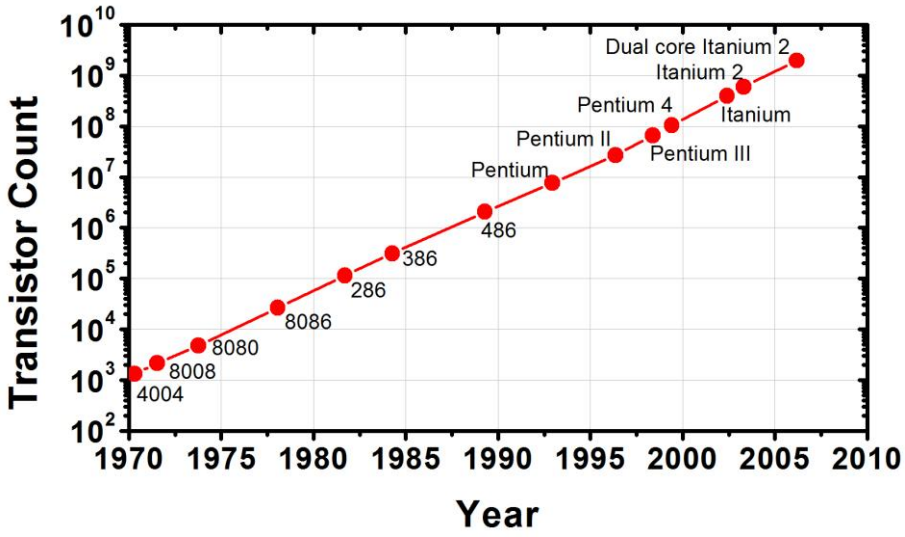

Fig. 1.2. Number of transistors on Intel microprocessors from 1970 to 2006. Adapted from [3].

Several key developments in the semiconductor industry helped enable this historical engineering feat: the development of the silicon (Si) metal-oxide-semiconductor field-effect-transistor (MOSFET), integrated circuits (IC), and complementary MOSFET (CMOS) circuits. The ability to easily grow a stable, high-quality silicon dioxide (SiO_2) insulating film on Si as well as relatively straightforward scaling of transistor dimensions allowed the Si MOSFET to supersede bipolar junction transistor (BJT) technology. By integrating these transistors along with resistors, capacitors, diodes, and wires all on the same chip, power, size, and cost could be reduced drastically compared to circuits made up of discrete components. Finally, the minimal standby leakage power in CMOS (*i.e.* when the circuit is not switching logic states), enabled MOSFET scaling to sustain improvements in circuit density and speed. In addition to these key developments, credit must also be given to breakthroughs in semiconductor processing technology. Without high-purity, large semiconductor crystal growth, photolithography, thin-film growth and deposition (epitaxy and chemical vapor deposition), dry reactive ion etching (RIE), and ion implantation, the success of modern IC technology could not have been achievable.

The rate of transistor development was highlighted by Gordon Moore in 1968, where he observed that the number of transistors per IC chip doubled every two years [2]. Though Moore only expected this trend to last a decade, breakthroughs in semiconductor processing has allowed "Moore's Law" to hold true to this day, with modern IC chips now containing more than a billion transistors (Fig. 1.2) [3]. By incorporating more components within the same chip area and leveraging the parallel nature of planar processing, the cost per transistor has been reduced in each successive generation of IC technology, yielding higher circuit functionality for the same price or providing the same circuit functionality at a lower price. In addition to reduced cost, scaling the transistor size also leads to improvements in energy efficiency and operating speed; if the device dimensions are scaled by a factor $1/\kappa$ (where $\kappa > 1$), then the circuit delay reduces by a factor of κ, circuit density increases by κ^2, and switching power density remains constant [4].

These benefits that come with scaling allow lower power per IC function or more circuits for the same chip area and power dissipation.

With the requisite technology and infrastructure in place, IC technology entered a "golden age," where relatively straightforward scaling of the two-dimensional (2-D) planar bulk Si MOSFET enabled exponential increases in computing power and reductions in cost, unimaginable only several decades before. The main parameter to improving MOSFET performance – scaling of the SiO_2 gate oxide thickness – allows better coupling of the gate electrode to the channel and increases the inversion charge carrier density to increase drive current. Eventually, the oxide thickness was scaled so thin that excessive tunneling current from the gate to the channel was having deleterious effects on device performance and reliability. Insulators with high dielectric constants (high-*k*) as well as metal gate technology resolved this problem by increasing the physical oxide thickness (T_{OX}) but reducing the electrical oxide thickness (EOT) [5]. This high-*k*/metal gate (HKMG) technology was a fundamental shift in Si CMOS since it was the relatively pristine SiO_2 gate oxide interface that initially made Si CMOS more attractive than other transistor technologies.

As Si CMOS scaling continues, HKMG development only represents one example of incorporating new materials into the Si MOSFET. Although HKMG mitigates the gate leakage and reduced EOT, it also results in lower channel mobility compared to SiO_2/polysilicon gate stacks due to remote coulomb scattering [6]. To continue improving performance (*i.e.* drive current), strain technology such as contact-etch stop layers (CESL) [7], stress memorization technique (SMT) [8], and embedded source/drain stressors [9] are routinely used today to further boost performance by improving channel mobility. In fact, the performance gains of modern MOSFETs can be mostly attributed to these various strain technologies (Fig. 1.3) [10].

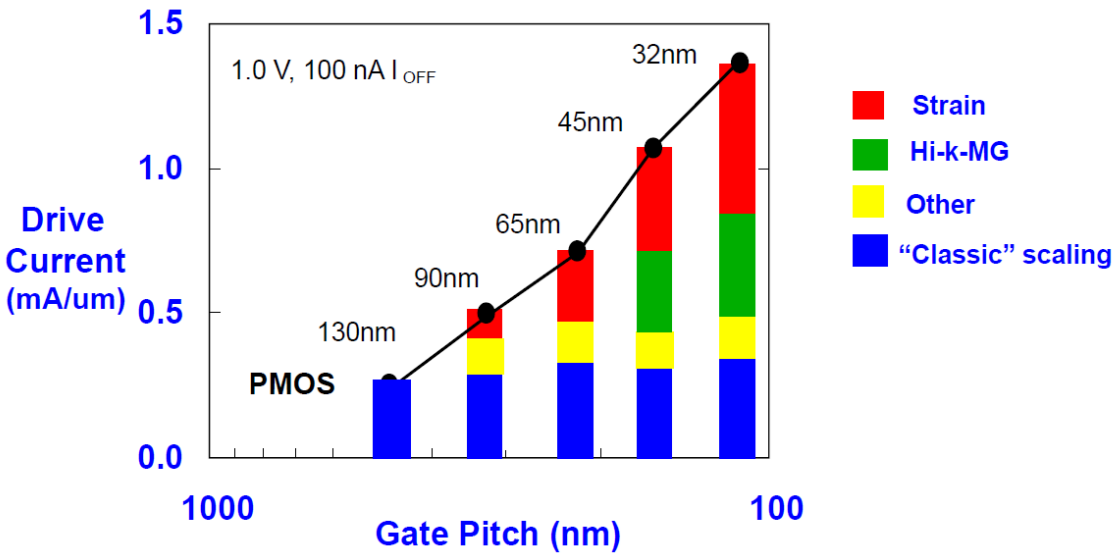

Fig. 1.3. Breakdown of p-channel MOSFET performance enhancement components. Adapted from [10].

Although the recent developments of HKMG and strain techniques have altered the appearance of the conventional MOSFET (Fig. 1.4), the overall geometry of the device has remained relatively unchanged, *i.e.* the MOSFET is still built on a planar (2-D) bulk Si substrate. However, with continued transistor scaling (physical L_G < 30nm), the distance between the source and drain junctions are now so close that the gate has difficulty in maintaining electrostatic control over the channel. This results in degradation of short-channel effects: subthreshold swing S (the gate voltage needed to increase subthreshold current by one order of magnitude) increases and results in higher off-state leakage, the threshold voltage V_T decreases for shorter L_G, and the reduction of V_T with increasing drain voltage due to the lowering of the source-channel potential barrier as the drain potential increases (known as drain-induced barrier lowering, DIBL). In order to attain a high on-state drive current, these degraded short-channel effects result in unacceptably high leakage currents when the device is in the off-state. Conversely, to maintain a low off-state current specification, the device cannot achieve high drive current when biased in the on-state.

In order to continue improving performance with transistor scaling without incurring unacceptably high off-state leakage currents, the planar bulk MOSFET structure can be altered to provide better electrostatic integrity and suppressed short-channel effects (SCE). This reduces the S so that it takes less application of gate voltage to reach the on-state, allowing the device to have both a low off-state leakage current and high on-state current. In addition, to further boost drive current, materials with higher mobility than Si can be utilized. As shown in Fig. 1.5 (adapted from the International Roadmap of Semiconductors (ITRS)), new MOSFET structures and high-mobility materials are two large unknowns facing the industry. In the next two sections, these two unknowns – advanced alternative MOSFET structures and high-mobility channel materials – will be discussed in greater detail.

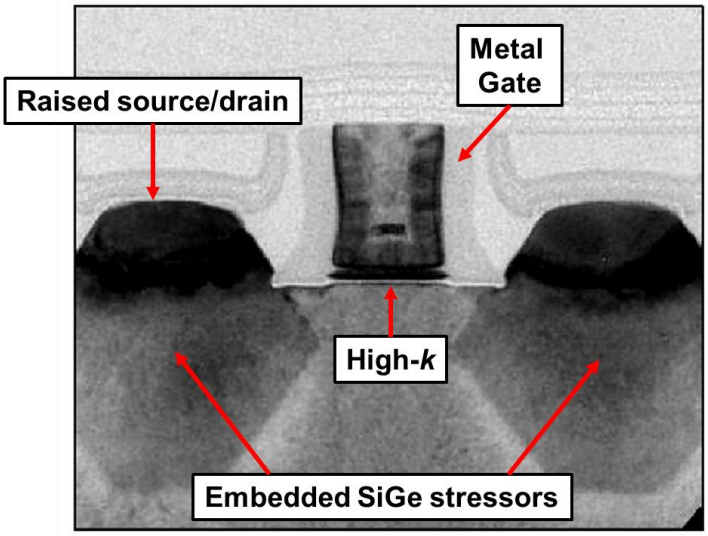

Fig. 1.4. Cross-sectional transmission electron micrograph of Intel's 32nm node p-channel MOSFET. Adapted from [5].

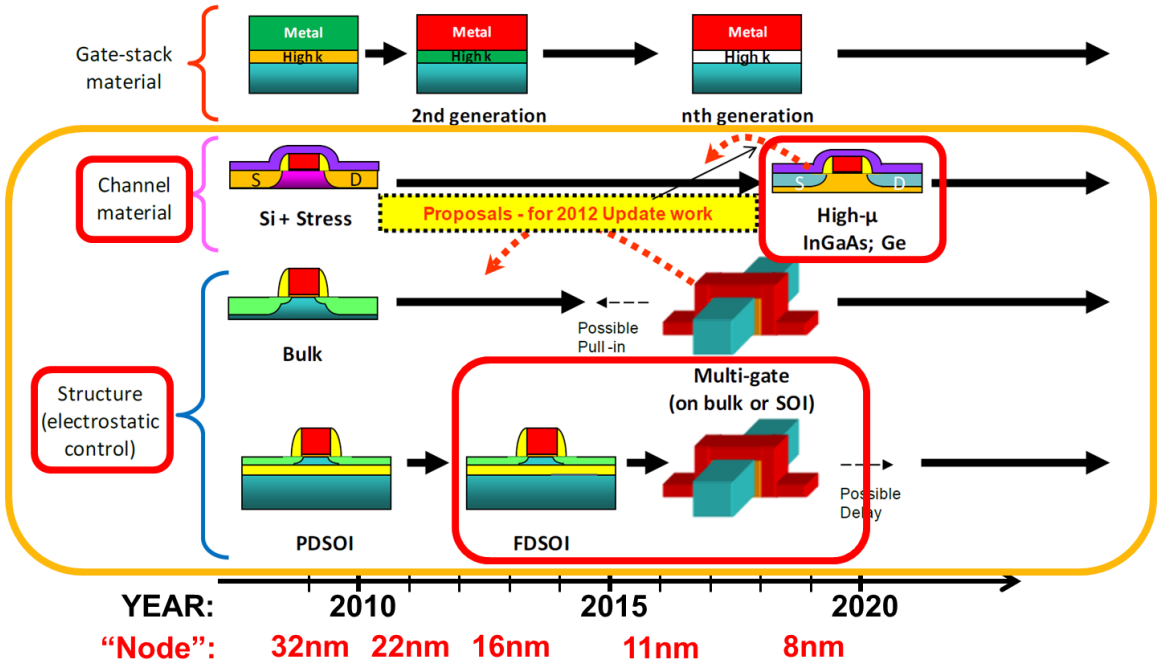

Fig. 1.5. Schematic diagram of ITRS roadmap. Adapted from [11].

1.2 Advanced MOSFET Structures – An Evolution or Revolution of the Planar Bulk Design?

To prevent excessive SCE in the planar bulk MOSFET (in essence, reducing the capacitive coupling from the drain to the source), the source/drain junction depth X_J, channel depletion depth X_{DEP}, and the EOT should be minimized to improve gate control over the channel. Quantitatively, these parameters are used to determine the scale length of the planar bulk MOSFET [12], λ_{BULK}, which is an indication of the minimum achievable L_G before SCE are too severe, and is given in (1):

$$\lambda_{BULK} = 0.1\left(T_{OX}X_J X_{DEP}^2\right)^{\frac{1}{3}}. \qquad (1)$$

With transistor dimensions shrinking, scaling of X_J, X_{DEP}, and T_{OX} (or equivalently, EOT) are becoming unsustainable with conventional ion implantation technologies. The two main advanced MOSFET structure candidates – fully-depleted silicon-on-insulator (FDSOI) and double gate (DG) MOSFETs – avoid using ion implantation to define X_J and X_{DEP} and instead rely on geometrically confining the channel to an ultra-thin body (UTB) of Si. X_J and X_{DEP} are then defined by the thickness of the Si body.

FDSOI MOSFETs are built on a silicon-on-insulator (SOI) substrate, where a thin film of Si (< 10 nm thick) rests upon an insulating buried-oxide (BOX) layer (Fig. 1.6) [13]. By limiting

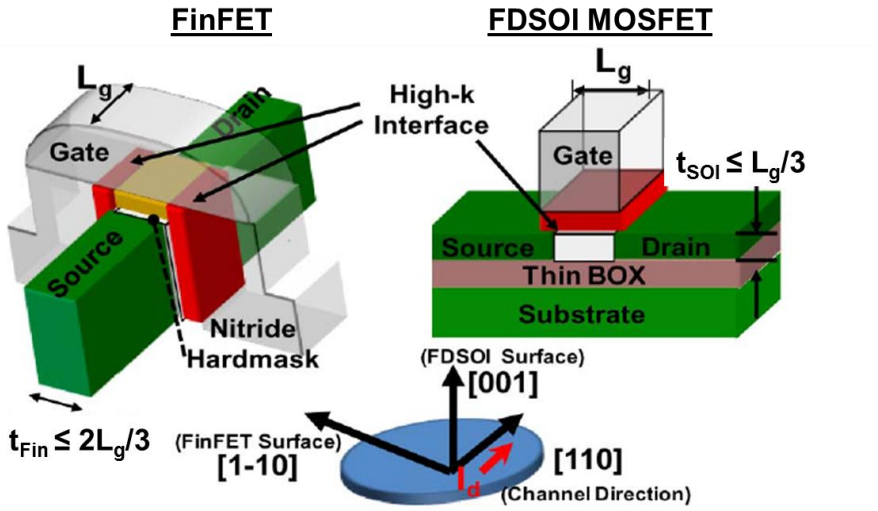

Fig. 1.6. Schematic view of the FinFET (left) and FDSOI MOSFET (right). Adapted from [14].

the amount of Si in the device in this fashion, the capacitive coupling between the gate and channel increases while the coupling between drain and channel commensurately decreases. For FDSOI MOSFETs, a good rule of thumb to maintain good SCE is for the Si film thickness (T_{Si}) to be no thicker than $L_G/3$ [14]. A practical lower limit of T_{Si} for SOI substrates is likely around 5 nm, beyond which quantization and mobility degradation effects become too severe [15]. In addition the special SOI substrates are more expensive than bulk Si wafers. The main advantage of the FDSOI MOSFET over other advanced transistor structures is the relative ease of processing due to the planarity of the structure; most conventional bulk MOSFET fabrication processes can be used for UTB SOI MOSFETs with little modification.

The DG MOSFET also utilizes a thin body but sandwiches it between two gates, providing better electrostatic control and thus relaxes the T_{Si} thinness requirement compared to the FDSOI MOSFET by a factor of two (*i.e.* T_{Si} can be $2/3*L_G$) [16]. The most manufacturable of all proposed DG designs is the FinFET (Fig. 1.6) [17], a 3-dimensional (3-D) structure where the thin Si body is achieved by etching a narrow Si stripe (hence the "fin" moniker) with the gate electrodes straddling the sidewalls of the Si stripe. FinFETs can be fabricated on either bulk or SOI substrates and are already implemented in high-volume production [18]. The main drawback of FinFET technology is the need to form high aspect ratio stripes (narrow stripe width to control SCE and tall stripe height to achieve high current per unit layout area). Since the FinFET stripe width must be less than L_G (which has historically been the smallest printed feature size), the ability to form high aspect ratio stripes at tight stripe pitches (to maximize layout area efficiency) for future technology nodes may pose a major technological challenge.

Both the FDSOI MOSFET and FinFET structures represent *revolutionary* changes to the planar bulk MOSFET. FDSOI MOSFETs require a different, more costly substrate while the 3-D FinFET requires high aspect ratio stripes that could reduce manufacturability. Both thin body structures rely on constraining the channel geometry to control SCE instead of doping as in the

conventional MOSFET structure. Although an elegant solution to suppressing SCE, the thickness of the thin-body channel becomes the critical parameter and may be difficult to control in actual implementation. Instead, perhaps a more *evolutionary* structure would be more pragmatic, one that combines both doping and channel geometry in a hybrid approach to improve SCE and performance without resorting to new substrates or high aspect ratio structures. This design – the segmented-channel MOSFET (SegFET) – will be discussed in Chapters 2 and 3. The results indicate that the SegFET provides better scalability than planar bulk MOSFETs and can achieve performance comparable to thin-body MOSFET structures.

1.3 High-Mobility Channels – A Path to Improved MOSFET Performance?

Another active research topic in the semiconductor industry is the integration of high-mobility channels in CMOS technology. The mobility in modern Si MOSFETs is degraded due to high transverse electric field, and is exacerbated with the adoption of HKMG. Although strain techniques have boosted mobility in Si, the efficacy of these stressors may diminish with the transition to thin body MOSFET structures and shrinking device pitch [19]. Thus, the main motivation for using high mobility materials is to improve the drive current for high-performance CMOS applications at ultra-scaled dimensions.

Table 1.1 lists various semiconductor materials and their respective bulk electron and hole mobilities. Most III-V materials such as GaAs, InAs, and InSb can provide extremely high electron mobilities and would be most suitable for n-channel MOSFETs (nMOSFET). Ge, on the other hand, is a good candidate for p-channel MOSFETs (pMOSFET) because of its high hole mobility.

III-V MOSFET research has demonstrated its potential for high-performance CMOS [20]. The largest obstacle is integration of III-V materials on Si substrates because bulk III-V substrates are very costly and mechanically fragile. Epitaxy of III-V materials on Si requires the growth of thick buffer layers to decouple the mechanical stress that arises due to the lattice mismatch between most III-V alloys and Si. This adds significant cost and poses large process integration issues. In addition, fundamental research on suitable gate oxides and contact metals for III-V materials is still being conducted [21], and implementation of III-V channels for mainstream CMOS applications is likely many years from realization.

Ge and silicon-germanium ($Si_{1-x}Ge_x$) alloys are Group IV materials like Si and thus are more promising from a process integration perspective. Indeed, the semiconductor industry has more experience using Ge, as it was the first material to successfully demonstrate transistor action. In addition, embedded $Si_{1-x}Ge_x$ source/drain stressors are now commonly used in modern MOSFETs, demonstrating relatively easy processing compatibility with Si. Ge and $Si_{1-x}Ge_x$ channels have successfully demonstrated good pMOSFET performance [22-23]; for Ge nMOSFETs, problems with contact resistance [24], n-type dopant activation [25], and gate oxide interface states [26] have yet to be satisfactorily solved, preventing the realization of all-Ge

TABLE 1.1
BULK CARRIER MOBILITIES OF VARIOUS SEMICONDUCTOR MATERIALS

Material	RELATIVE PERMITTIVITY	Mobility ($cm^2/V/s$)	
		Electron	**Hole**
Si	11.9	1400	470
Ge	16.2	3900	1900
GaAs	12.9	8500	400
InAs	15.2	40000	500
InSb	16.8	77000	850

CMOS. Still, due to the semiconductor industry's history and experience with Ge, Ge and $Si_{1-x}Ge_x$ alloys represent the most straightforward path to integrating high-mobility materials with Si.

From a physics standpoint, one drawback of these alternative channel materials is that the bandgap E_G is inversely proportional to the mobility. If E_G is too low, conduction-to-valence band (and vice versa) tunneling current from drain-to-bulk or drain-to-source increases the off-state leakage currents. Furthermore, a smaller E_G is usually associated with higher dielectric constant, which degrades SCE and the scalability of the device. In order to minimize the deleterious effects of these attributes, high-mobility materials will likely be confined in a thin film (< 10 nm thick) within the channel region of the MOSFET, where the gate has the most electrostatic control. In addition, a thin channel will effectively increase E_G through quantization effects. Careful design and implementation will be needed to successfully integrate high mobility channels in future technology nodes, and this is explored in Chapters 4, 5, and 6.

1.4 A Fork in the Silicon Road…

The semiconductor industry is at a crossroads. Not only are there significant obstacles in device physics and process integration of new transistor structures and channel materials, but the economics of the semiconductor industry is also changing. The explosive growth of mobile devices and cloud computing is signaling a future world where electronic devices and sensors become ubiquitous. Some have termed this pervasiveness of electronics as the "internet of things," [27] which will undoubtedly enable new exciting applications. However, for these devices to be attractive to the average consumer, the cost of these ICs must be small. Going forward, a new transistor structure is certainly needed for continued scaling, but will the cost of the proposed revolutionary alternative designs outweigh the performance benefits? Is there a more evolutionary structure of the bulk planar MOSFET that poses less technological challenge and is less expensive to fabricate? Do high mobility channels provide improved MOSFET performance at small L_G and are they worth the investment? This work investigates and attempts to help shed light on these important economic considerations from a device physics and process integration perspective. Chapter 2 introduces a novel segmented-channel MOSFET structure

(SegFET) that is an evolution, rather than a revolution, of the bulk planar design. Chapter 3 presents performance comparisons (simulated with technology computer-aided design (TCAD)) for the SegFET and the leading alternative transistor structure, the FinFET. In Chapter 4, $Si_{1-x}Ge_x$ is explored as a possible high mobility channel material for pMOSFETs, and in Chapter 5, $Si_{1-x}Ge_x$ channels are experimentally implemented on a SegFET structure. Chapter 6 investigates the use of Ge channels for ultimate scalability at the end of the ITRS roadmap within a DG structure. Finally Chapter 7 summarizes the contributions of this work and offers suggestions for future research in this area.

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Chapter 2

Segmented-Channel MOSFET (SegFET) Design

2.1 Introduction

As discussed in Chapter 1, continued CMOS scaling will necessitate an evolution of the MOSFET structure. Although the FinFET and FDSOI MOSFET are leading candidates, these alternatives either require high-aspect ratio structures that reduce manufacturability or more expensive SOI substrates. The segmented-channel MOSFET (SegFET) structure is an evolutionary alternative that combines the benefits of the bulk planar MOSFET and the improved gate control of more revolutionary multiple-gate device architectures into a low-aspect ratio channel structure on a bulk substrate. This section describes the SegFET structure and reports the first experimental demonstration of SegFETs fabricated using a conventional process flow but starting with a corrugated-silicon substrate. The performance of the SegFETs is compared against that of control devices fabricated using the same process flow but starting with a planar silicon substrate.

2.2 SegFET Structure

The channel region of a SegFET (ref. Fig. 2.1) is built on a corrugated-silicon substrate, which consists of one or more parallel Si segments ("stripes") of equal width W_{STRIPE} that can be wider than the effective channel length. These Si stripes are isolated from each other by a very shallow trench isolation (VSTI) dielectric material. Within each Si stripe, the channel- and source/drain-doping profiles are similar to those in a planar bulk MOSFET (cutline AA' in Fig. 2.1). The VSTI regions extend to a depth below the source/drain extension (SDE) regions but which can be much shallower than the conventional shallow trench isolation (STI) oxide, *e.g.* the

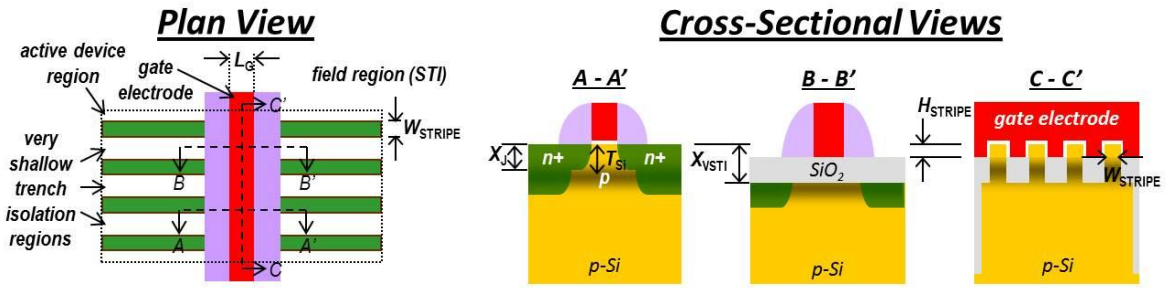

Fig. 2.1. Plan view (left) and various cross-sectional views (right) of the SegFET structure. Adapted from [1].

deep source/drain (S/D) regions are contiguous beneath the VSTI to help reduce S/D resistance (cutline BB' in Fig. 2.1). Because of the relaxed geometry of the SegFET (W_{STRIPE} can be larger than the effective channel length and the VSTI depth is much shallower than the STI), it should be more manufacturable than thin-body structures. Due to fringing electric fields through the VSTI regions, gate control is enhanced for the SegFET as compared to a conventional planar MOSFET. Gate control can be further enhanced by slightly recessing the VSTI dielectric prior to gate-stack formation to allow the gate to wrap around the top portions of the channel stripes (cutline CC' in Fig. 2.1). The effective channel width of the SegFET is adjusted by changing the layout width of the active region to change the number of channel stripes which it encompasses. Since each stripe has the same geometry and hence the same electrical characteristics, SegFETs should exhibit negligible layout-width dependencies of the threshold voltage (V_T) and the normalized current, in contrast to conventional MOSFETs which show significant layout-width dependencies due to sub-wavelength patterning abberations/misalignment, narrow-width effects, layout-dependent stress effects, etc. Although it may seem that channel segmentation should reduce layout area efficiency (since a portion of the device width is replaced by non-conducting VSTI stripes), recessing the VSTI can help regain the lost layout area efficiency and improve electrostatic integrity to allow for lower V_T; also, it will be shown later in Section 2.5 that reduced transverse electric fields in the SegFET channel increases mobility to enhance drive current and further improve the layout area efficiency.

2.3 SegFET Fabrication Process Overview

Although the SegFET structure may seem quite different from the planar bulk MOSFET, its fabrication process flow is identical to that of the planar bulk MOSFET and is illustrated schematically in Fig. 2.2. The only additional step in a typical SegFET process is the fabrication of the corrugated-silicon substrate, comprising of alternating channel and VSTI stripes (discussed in Section 2.3.1). After fabricating the corrugated-silicon substrate, the active channel region is lithographically defined. This is followed by STI isolation and well/channel implant. Before gate stack formation, the channel stripes can be elevated above the VSTI to enhance gate

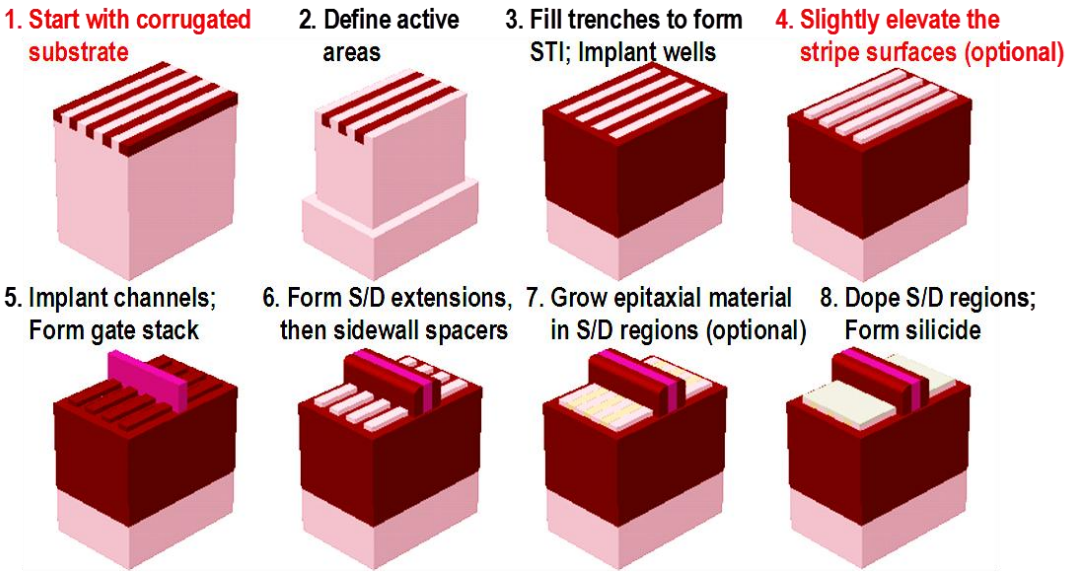

Fig. 2.2. Overview of the SegFET fabrication process.

control by either growing semiconductor material on the channel stripes via selective epitaxy or by recessing the VSTI by etching. After gate definition, S/D extension implants and gate-sidewall spacers are formed, followed by S/D formation (epitaxial raised S/D can also be implemented) and silicidation. Note that performance-enhancing techniques used in state-of-the-art planar bulk transistors (*i.e.* high-*k*/metal gate, embedded S/D and contact etch stop layer (CESL) stressors, back-biasing) can be readily applied to the SegFET due to the commonality with a planar bulk technology process flow and low-aspect-ratio channel structure.

2.3.1 Corrugated-Silicon Substrate Fabrication

The corrugated-silicon substrate approach to fabricating segmented-channel MOSFETs is essentially a smart double-patterning technique that provides for reduced process variability due to the highly geometrically regular pattern of the corrugated substrate and the elimination of the need to form high-aspect-ratio semiconductor structures. To obtain the tight pitch for the segmented Si/VSTI stripes of the corrugated-silicon substrate with 193nm deep-ultraviolet wavelengths, double patterning techniques such as litho-process-litho-etch [2] or spacer lithography [3] can be used. The increased design and process complexity normally associated with these double-patterning techniques for IC fabrication [4] are minimal for the corrugated-silicon substrate fabrication because of the geometric regularity.

There are two main methods to corrugated-silicon substrate fabrication. One method ("etch-fill") involves patterning lines and spaces on the Si substrate and performing a dry anisotropic reactive-ion etch (RIE) to form Si lines and trenches. A thick layer of dielectric material is then deposited across the substrate and planarized to fill the trenches with VSTI material. The other method ("etch-epi") etches lines and trenches into a dielectric layer previously deposited on the Si substrate. The lines of dielectric material eventually become the VSTI stripes and within the

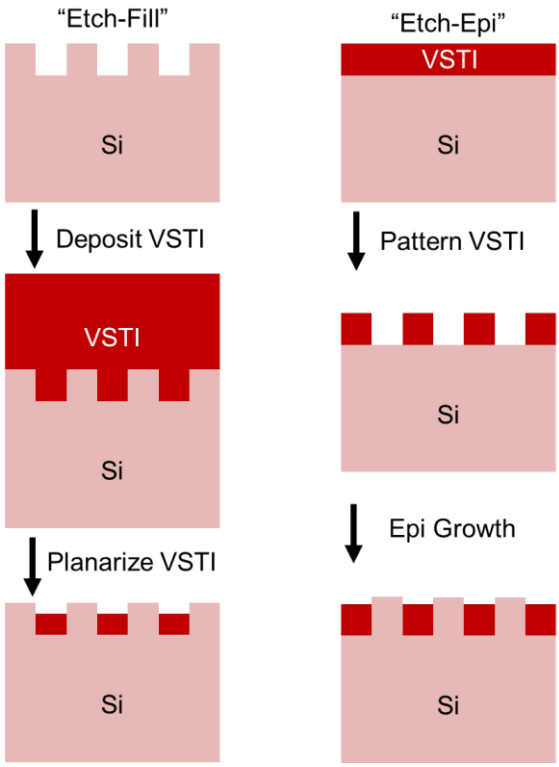

Fig. 2.3. Schematic of the "etch-fill" (left) and "etch-epi" (right) methods to fabricating a corrugated-silicon substrate.

trenches, semiconductor material is selectively epitaxially grown to form the semiconductor stripes. The "etch-fill" and "etch-epi" method are shown schematically in Fig. 2.3. In this work, both the "etch-fill" and "etch-epi" methods are used to fabricate the corrugated-silicon substrate (ref. Chapter 3 and 5, respectively). Note that one benefit of the "etch-epi" method is that high-mobility semiconductor materials (Ge, GaAs, etc.) can be epitaxially grown within trenches with a depth:width aspect ratio larger than 1:1. Crystalline defects due to stress are annihilated at the VSTI sidewalls, resulting in a high-quality surface [5], facilitating the integration of high-mobility channel materials or optoelectronic devices directly on a Si substrate.

2.4 Experimental SegFET Fabrication

Having summarized the general SegFET structure and fabrication process in the above sections, the rest of this chapter is devoted to results of the first experimental demonstration of the SegFET and comparison to planar bulk devices. As discussed above, the SegFET was proposed originally as a more scalable bulk MOSFET structure. However, due to the unavailability of a shallow trench isolation process in our university laboratory, a simple mesa isolation process was used to fabricate n-channel MOSFETs with channel lengths down to 45

nm, which required the use of SOI wafer substrates. The SOI is relatively thick (90 nm), so that the fabricated devices have partially depleted channel regions. Channel doping and halo doping are used to suppress short-channel effects, similarly as for bulk-silicon MOSFETs. The effect of the buried oxide layer on the doping profiles and DC electrical characteristics was confirmed through advanced TCAD process and device simulations [6] to be negligible (Fig. 2.4) so the results of this work are applicable to bulk devices. (The simulations showed that devices fabricated on an SOI wafer have identical subthreshold swing (*S*) and drain-induced barrier lower (DIBL) as devices fabricated on a bulk silicon wafer.)

The "etch-fill" method was used to form the corrugated-silicon substrate in this work. 193 nm immersion lithography was used to print resist lines and spaces with 120 nm pitch, and then the SOI in the spaces was recessed by 35 nm using reactive ion etching (RIE). After resist removal, the VSTI was formed by thermally growing a 2 nm-thick oxide layer and then depositing a 300-nm-thick layer of Si_3N_4; the Si_3N_4 layer was subsequently etched back using RIE, resulting in VSTI regions that are slightly recessed from the top surface of the silicon stripes (Fig. 2b). Si_3N_4 instead of SiO_2 was used as the VSTI material to ensure that it remained intact after multiple dilute-hydrofluoric-acid cleaning steps during the fabrication process. It should be noted that the higher dielectric constant of the VSTI material is beneficial for improved gate control (via fringing electric fields) if the VSTI recess depth is shallower than the retrograde channel doping. In fact, the VSTI recess depth can be made shallower (resulting in a more planar substrate) if a higher permittivity VSTI material is used, while providing the same amount of gate control [7]. As the VSTI dielectric constant and/or the VSTI recess depth increases, the retrograde/halo doping can be made deeper to reduce the transverse electric field in the channel region and to reduce band-to-band tunneling leakage.

Devices were fabricated on the corrugated-silicon substrate as well as a control SOI wafer substrate, using a conventional bulk MOSFET fabrication process after mesa isolation (active

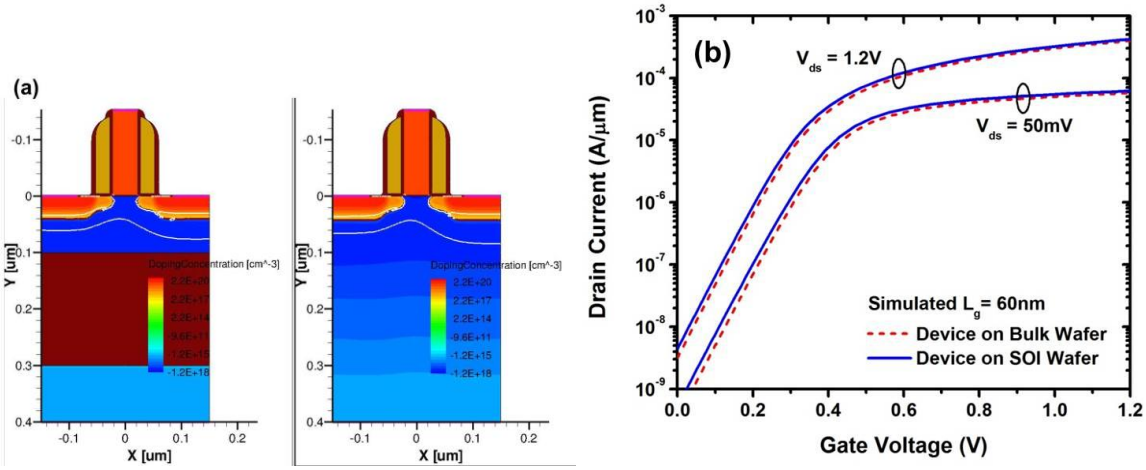

Fig. 2.4. TCAD (a) process and (b) device simulations of the device fabricated with and without a BOX layer. The effect of the BOX on the doping profiles and transfer characteristics are negligible.

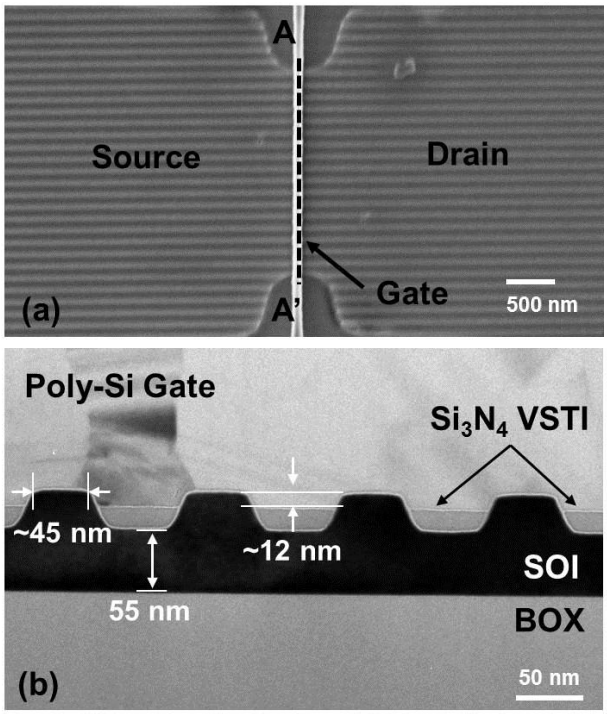

Fig. 2.5. (a) Plan-view scanning electron micrograph (SEM) of SegFET after poly-Si gate etch. (b) Cross-sectional transmission electron micrograph (TEM) taken along the poly-Si gate of a fabricated SegFET (cutline AA' in (a)), showing the channel stripes separated by Si_3N_4 VSTI regions. W_{STRIPE} ~ 45 nm. The VSTI is recessed by ~12 nm.

area lithography and etch). Images during and after the fabrication process are shown in Fig. 2.5. The gate stack was formed by 2.5 nm dry thermal oxidation followed by deposition of *in-situ* phosphorus-doped poly-Si and a low-temperature oxide (LTO) hardmask. Photoresist ashing and LTO trimming were used to achieve short gate linewidths (~40-50 nm). After gate patterning and poly-Si reoxidation, arsenic (As) source/drain extension (SDE) and boron (B) halo implants were performed. Next, Si_3N_4 gate sidewall spacers were formed, followed by As deep source/drain implants and a 20-s 950°C activation anneal. Back-end process steps included deposition of a LTO passivation layer, contact-hole formation, sputtering and patterning of a TiN barrier and Al/2% Si metal layer, and a forming-gas anneal. Process details are found in Appendix A.

It should be noted that the devices in this work do not have the benefit of silicided source/drain regions for reduced parasitic resistance, metal/high-permittivity gate stacks for improved gate control, or process-induced strain for enhanced carrier mobility, so that their performance is not comparable to that of state-of-the-art MOSFETs. Such performance boosters would provide similar or enhanced benefit (*e.g.* more strain enhancement due to narrow active widths [8]-[9]) for the SegFETs as for the control devices. The purpose of this study is simply to demonstrate the benefit of the segmented-channel design as compared to the conventional channel design.

2.5 Experimental SegFET Electrical Characteristics

All of the devices reported in this work have an active-area width of 2 um; the measured transistor currents are normalized to this width. Each SegFET comprises 16 channel stripes, amounting to an electrical channel width that is ~1 um, taking into account the gated stripe sidewalls (ref. Fig. 2.5). The effective channel length (L_{eff}) was extracted using the Y-function method [10] and was found to be well correlated with the physical L_G measured after gate patterning. Measured transfer (I_D-V_G) characteristics for devices with L_{eff} values of 75 nm and 45 nm are shown in Figs. 2.6a and 2.6b, respectively. The threshold voltage (V_{TH}) of the SegFET is lower than that of the control device because of reduced depletion charge per unit channel width due to the effect of channel sidewall gating, which also results in lower transverse electric field (Fig. 2.7) and hence higher peak effective mobility and lower gate leakage (Fig. 2.7 inset). (Strain induced within the channel regions of the Si stripes by the recessed Si_3N_4 VSTI was determined from TCAD process simulations to be negligible, and hence cannot account for the lower V_{TH}.) The superior electrostatic integrity of the SegFET becomes evident at 45 nm L_{eff}, in the steeper subthreshold swing and reduced drain-induced barrier lowering.

From a comparison of super-threshold current and linear transconductance (g_m) characteristics (Fig. 2.6c-d), it can be seen that parasitic series resistance (R_{SD}) is larger for the SegFET than the control device. (The extracted value of R_{SD} [11] is 4.5 kΩ·µm for the SegFET as compared with 3.6 kΩ·µm for the control device.) Since the VSTI dielectric is slightly recessed from the top surface of the silicon stripes, the implanted As dose in the top ~12 nm of the SDE regions was slightly lower for the SegFET than for the control device, which can be addressed by using a slightly higher SDE implant dose for the SegFET. R_{SD} can be further reduced by using angled implants and laser/spike anneal or *in-situ*-doped raised source/drain regions [12]. In addition to

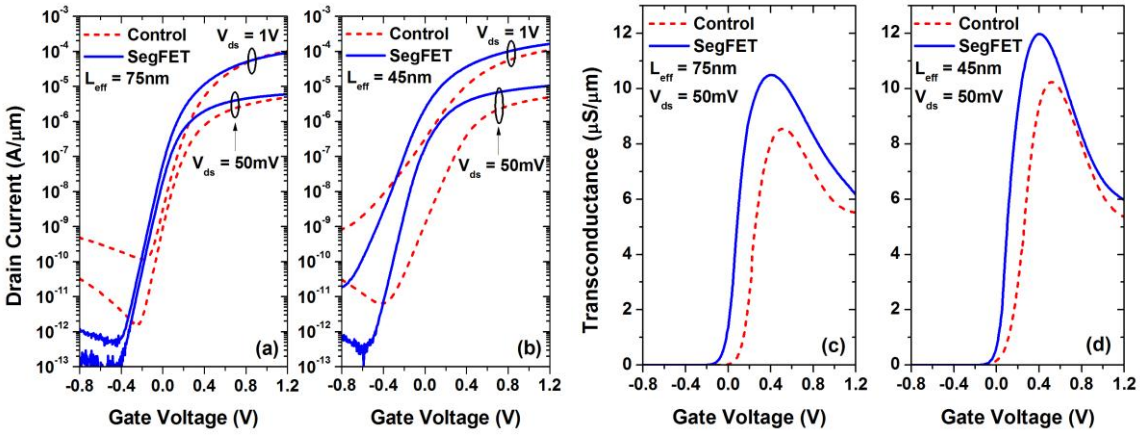

Fig. 2.6. Measured transfer characteristics for a SegFET and a control device for electrical channel lengths of (a) 75 nm and (b) 45 nm; measured linear transconductance for (c) L_{eff} = 75 nm and (d) 45 nm. Data is normalized to the device layout width.

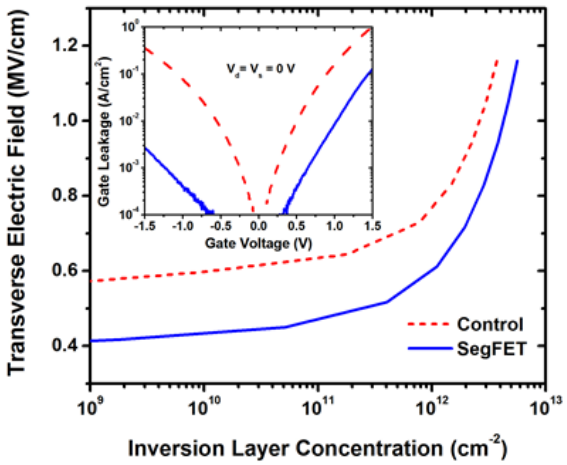

Fig. 2.7. TCAD simulations of the transverse electric field at the oxide/channel interface as a function of inversion layer concentration. The inset graph shows measured gate leakage characteristics for the SegFET and control devices, normalized to the channel layout area.

the lower As dose, the Si stripes within the source/drain regions were eroded during the various etching steps in the fabrication process (Fig. 2.8), further increasing R_{SD} for the SegFET. From the output characteristics (I_D-V_D) for the same gate overdrive (Fig. 2.9), the effect of the higher R_{SD} is clearly seen in the earlier drain saturation voltage of the SegFET, even though the current in the linear regime is larger compared to the planar bulk control device.

The leakage floor of the SegFET is much lower than that of the control device, due to reduced gate-induced drain leakage (GIDL). This reduction in GIDL is likely due to the lower SDE implant dose (as discussed above) and also the effect of sidewall gating, which result in a lower transverse electric field strength in the gate-drain overlap region.

Fig. 2.10 shows how the subthreshold swing, drain-induced barrier lowering (DIBL), and saturation V_{TH} ($V_{TH,SAT}$) change with gate-length scaling. The SegFET structure shows reduced short-channel effects as compared to the conventional MOSFET structure, confirming its superior electrostatic integrity. Note that short-channel effects are well suppressed even if L_G is shorter than the channel stripe width. As mentioned above, V_{TH} is lower for the SegFET due to reduced depletion charge per unit channel width. TCAD process and device simulations for L_G ~ 200 nm indicate that boron segregation during the VSTI oxidation (prior to Si_3N_4 deposition) accounts for 50 mV reduction in V_{TH} while the effect of sidewall gating [13] accounts for 150 mV reduction in V_{TH}.

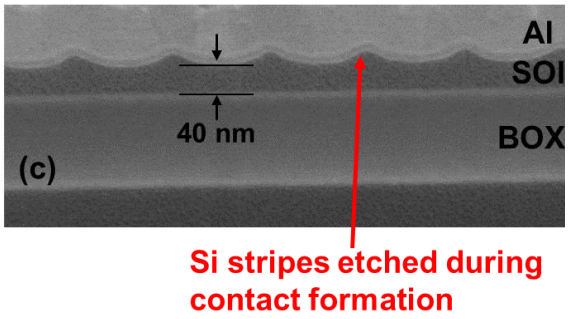

Fig. 2.8. Cross-sectional SEM of the SegFET source/drain contact region, showing the erosion of the stripes which increase R_{SD}.

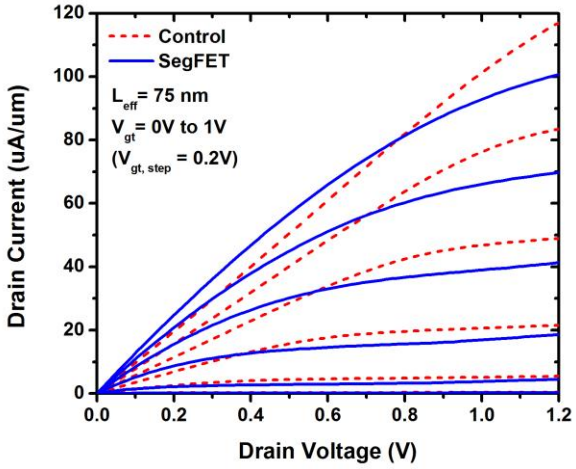

Fig. 2.9. Measured output characteristics for a SegFET and control device for the same gate overdrive. L_{eff} = 75 nm. Data are normalized to device layout width.

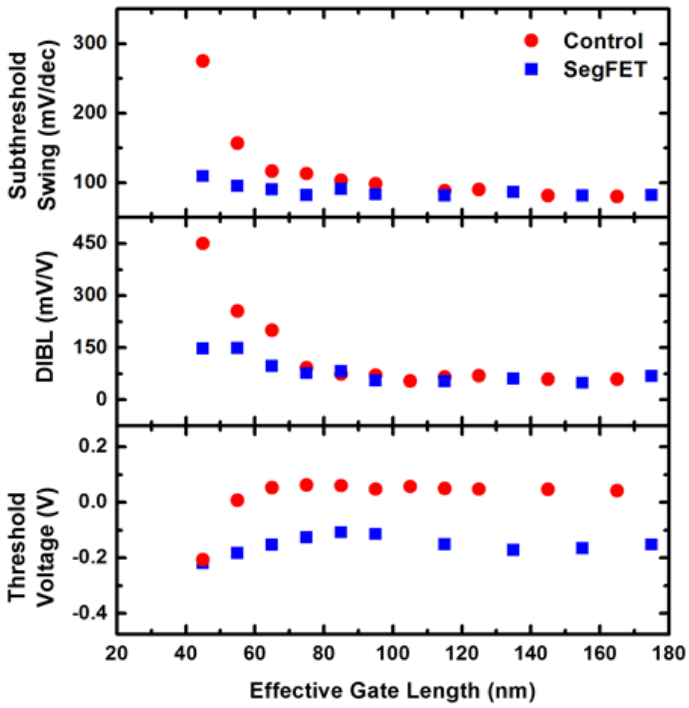

Fig. 2.10. Average (over 6 die) measured subthreshold swing, drain-induced barrier lowering (DIBL), and $V_{TH,SATt}$ as a function of L_{eff}. SegFETs show improved scalability compared to the control devices.

2.6 Summary

Segmented-channel MOSFETs (SegFETs) can be fabricated in a straightforward manner using a conventional process flow, by starting with a corrugated-silicon substrate. Due to enhanced gate control, SegFETs show reduced short-channel effects and can achieve comparable drive current per unit layout area as conventional planar MOSFETs. The SegFET design requires neither high-aspect-ratio channel stripes nor an ultra-thin SOI layer to achieve good electrostatic integrity; therefore it is an evolutionary solution for continued low-cost scaling of planar bulk MOSFET technology.

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Chapter 3

Comparison of SegFET and FinFET Performance

3.1 Introduction

Chapter 2 presented experimental and TCAD results that demonstrate the benefits and scalability of the SegFET compared to planar bulk MOSFETs. However, the leading alternative transistor design pursued by industry to supplant the planar bulk transistor is the FinFET. As mentioned in Chapter 1, the FinFET [1] utilizes the combination of a thin channel region (which eliminates sub-surface leakage paths) with a double-gate structure (which increases capacitive coupling between the gate and the channel) to suppress SCE and variability due to random dopant fluctuation (RDF) (as long as the channel doping level is low [2]). The FinFET can be fabricated on either bulk-silicon (bulk-Si) or silicon-on-insulator (SOI) wafer substrates [2-3]. FinFETs already are in mass production [4] but present significant challenges for manufacturing because they require the formation of narrow (sub-gate-length) Si fins [5] with uniform width [6] and large (>1) aspect ratio [7] particularly if a bulk-Si wafer is to be used [8]. In addition, a deep retrograde doping profile is needed for bulk-Si FinFETs at the base of the fin channel region to prevent sub-fin leakage between the source and drain regions.

Unlike the FinFET, the SegFET is comprised of low-aspect-ratio Si stripes with stripe widths greater than or equal to the gate length. A minimum-width (single-stripe) SegFET is essentially a quasi-planar bulk tri-gate MOSFET, where the top surface of the Si channel stripe contributes comparably to the transistor drive current as the sidewall surfaces of the channel stripe. Although multi-stripe SegFETs have improved scalability over planar bulk MOSFETs (ref. Chapter 2), it is also useful to optimize the design and benchmark the performance of single-stripe SegFETs (hereafter called tri-gate bulk MOSFETs in this chapter) to bulk FinFETs [8] using TCAD.

3.2 Device Simulation Methodology

Sentaurus 3-dimensional (3-D) device simulations were performed using advanced physical models [9] to optimize and compare the performances of the bulk FinFET and the tri-gate MOSFET (single-stripe SegFET). 3-D quantization effects were included using the density gradient quantization model. To accurately model the on-state drive current (I_{ON}) for the short gate lengths in this study, the hydrodynamic energy model was used. The hydrodynamic model is an approximation of the Boltzmann transport equation; with careful calibration, it can give results similar to the inflexible and computationally-intensive Monte Carlo simulation method. In this work, 2-dimensional Monte Carlo simulations of planar bulk-Si transistor structures with the same gate lengths as the 3-D transistor structures studied in this work were performed. These 2-D transistor structures were then re-simulated using the hydrodynamic model, and the energy relaxation times for electrons and holes were adjusted to match the Monte Carlo simulation results. Specifically, the default values for energy relaxation time of electrons and holes (0.3ps and 0.25ps, respectively) were changed to 0.14ps for both carriers.

Device capacitance was extracted from the small-signal admittance response calculated by the device simulator for each contact node. The values used for the supply voltage V_{DD} and other device design parameters were based on ITRS low-operating-power (LOP) specifications at physical gate length (L_G) values of 18nm and 13nm [10] (V_{DD} = 0.7 V and 0.6 V for L_G = 18nm and 13nm, respectively). For simplicity, no mobility enhancement or gate leakage was assumed.

3.3 Device Structure

Multi-gate bulk MOSFETs comprise Si channel stripes elevated above the surface of the surrounding isolation oxide by a distance H_{STRIPE}. In the bulk FinFET, the source and drain regions are also segmented, so that each fin is completely isolated by shallow trench isolation (STI) oxide. Fig. 3.1 shows 3-D and cross-sectional views (across the width of the transistor) of the tri-gate and FinFET structures, for L_G = 18nm. As shown, W is defined to be the width of the channel stripe, while t_{Si} is defined to be the depth of the peak of the retrograde doping profile. In this work, t_{Si} corresponds to the top surface of the STI so that H_{STRIPE} is equal to t_{Si}. The Gaussian retrograde doping profile has a peak concentration of 1E19 cm^{-3} and a gradient of 4nm/dec (as a practical steepness limit) for both the FinFET and tri-gate structures. (In practice, retrograde doping profiles with gradients as steep as 3 nm/dec can be achieved by utilizing diffusion-barrier layers [11].) The source/drain lateral doping profile, which is the same for the FinFET and tri-gate, is also Gaussian with a peak concentration of 1E20 cm^{-3} and gradient of 2nm/dec [10]. Note that there is no intentional channel doping; *i.e.* the only dopants in the channel region come from the tail of the retrograde doping profile and therefore the channel dopant concentration is relatively low (~5E17 cm^{-3}).

In principle, the height (H_{STRIPE}) of a FinFET can be made to be very tall to achieve high layout efficiency, *i.e.* large effective channel width (W_{eff}) per unit layout area. In practice,

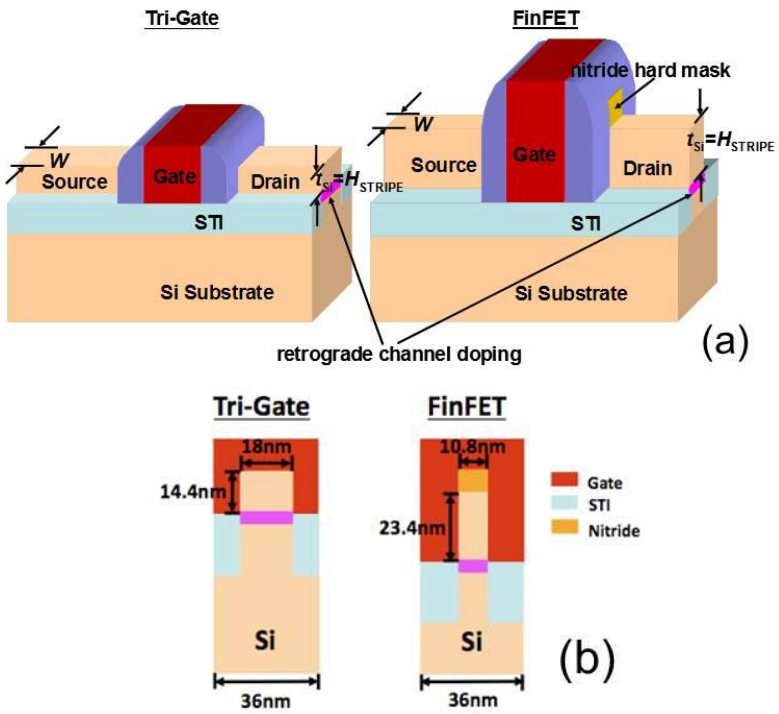

Fig. 3.1. (a) 3-D and (b) cross-sectional views (across the channel) of the simulated tri-gate and FinFET bulk MOSFET structures, for L_G = 18nm.

however, shorter fins are preferred for ease of manufacture and for design flexibility (*i.e.* to allow for finer increments in designed W_{eff}). Therefore, optimized bulk tri-gate and FinFET designs of the same W_{eff} are compared (for each H_{STRIPE} of the tri-gate design). The Si stripe pitch (SP) for the FinFET and tri-gate MOSFET are assumed to be the same ($2*L_G$, which is an aggressive estimation) as this is set by lithography limitations and experimental precedent: the smallest SP reported for FinFETs in the published literature is $2*L_G$ [2, 3], with all other reported SP values larger than $2*L_G$ [4].

To maximize layout efficiency for the tri-gate design, H_{STRIPE} should be as large as possible. However, it should be noted that if H_{STRIPE} is too high, the retrograde channel doping alone is no longer effective to suppress DIBL so that a narrower stripe width is needed. From TCAD simulations, the upper bound of H_{STRIPE} for the tri-gate design with $W=L_G$ is $0.8*L_G$ for highest I_{ON} while maintaining DIBL less than 100mV/V. (For $H_{STRIPE} > 0.8*L_G$, short channel effects degrade performance.) A lower value of H_{STRIPE} of $0.6*L_G$, which provides for easier manufacturability while maintaining good layout efficiency, is also investigated. To optimize the tri-gate MOSFET design, L_{eff} is first adjusted (by adjusting the width of the gate-sidewall spacers) to maximize I_{ON} for a fixed 7nm/μm off-state leakage current (I_{OFF}) as specified for double-gate FETs [3], while maintaining DIBL to be less than 100mV/V [12]. (Low DIBL is necessary to attain high effective current I_{eff} [13] as well as high output resistance.) The gate workfunction is then tuned in the range from 4.2eV to 4.5eV (which is experimentally achievable

[14]) to meet the I_{OFF} specification at V_{GS} = 0V; I_{ON} is then taken to be the transistor drive current for $V_{GS} = V_{DS} = V_{DD}$.

From a circuit-level perspective, the intrinsic delay is often more important than I_{ON}, so L_{eff} is further optimized to minimize intrinsic delay $C_{total}*V_{DD}/(2*I_{eff})$, where C_{total} is the total gate capacitance, and I_{eff} is the average of the drain current I_D for $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}/2$ and I_D for $V_{GS} = V_{DD}/2$ and $V_{DS} = V_{DD}$ [13].

For the FinFET design, the value of $H_{STRIPE} = t_{Si}$ is selected to provide the same W_{eff} as the tri-gate design, *i.e.* $H_{STRIPE,FinFET} = 0.5*[W_{Tri\text{-}Gate}+2*H_{STRIPE,Tri\text{-}Gate}]$. W was adjusted to maximize I_{ON} without having DIBL exceed 100mV/V, resulting in $W = 0.6*L_G$. (A wider fin results in unacceptable SCE, while a narrower fin results in increased parasitic source/drain resistance and is more difficult to manufacture. L_{eff} is also adjusted to maximize I_{ON} and to minimize delay, as is done for the tri-gate MOSFET design. The thickness of the nitride hard-mask layer is assumed to be equal to L_G.

A lower-aspect-ratio tri-gate bulk MOSFET design with $W = 2*L_G$ and channel stripe pitch = $4*L_G$ (which is the worst case for layout area efficiency and fringing capacitance) is also investigated to determine the impact of W on design optimization for the tri-gate bulk MOSFET. For all designs, the source/drain contacts are assumed to be made along the top and sidewall surfaces of the source/drain regions. The gate dielectric is silicon dioxide of physical thickness 9Å and 8Å for 18nm and 13nm L_G, respectively.

3.4 Device Performance Comparison

3.4.1 DC Characteristics

The simulated DC transfer characteristics for the optimized tri-gate bulk MOSFET and FinFET with same W_{eff} and L_G = 18 nm are shown in Fig. 3.2a. I_{ON} normalized to W_{eff} is 2.5% larger for the FinFET design (691μA/μm *vs.* 674μA/μm) because of the deeper retrograde doping profile (*i.e.* $t_{Si,FinFET} > t_{Si,Tri\text{-}gate}$) and hence lower average channel doping. This results in larger effective carrier mobility in the FinFET due to reduced impurity scattering and lower transverse electric field. It should be noted that, in practice, it is more difficult to form a steep retrograde or abrupt source/drain doping profile at the base of a tall Si stripe (due to the increased probability of channeling for a higher energy ion implant), so that the FinFET simulations are optimistic, *i.e.* I_{ON} is overestimated for bulk FinFETs in this work.

Fig. 3.3 shows the dependence of the subthreshold swing S, saturation threshold voltage V_{TH}, and DIBL on L_{eff} (keeping all other geometrical design parameters constant). Both multi-gate MOSFET designs show similar behavior for S and V_{TH}. The tri-gate MOSFET has larger DIBL at longer L_{eff} because the retrograde channel doping results in slightly larger capacitive coupling between the drain and channel. For the FinFET, DIBL is negligible at longer L_{eff} because the narrow Si stripe effectively reduces the capacitive coupling between the drain and channel. However, as L_{eff} is scaled down (so that W/L_{eff} increases), DIBL increases more rapidly for the FinFET because it relies solely on channel geometry to suppress DIBL and SCE. The tri-gate

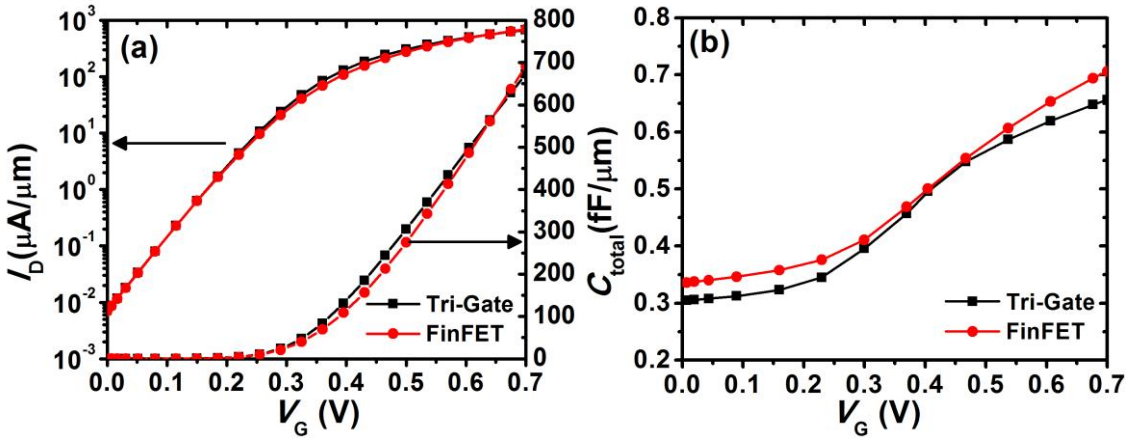

Fig. 3.2. Comparison of simulated characteristics for bulk MOSFETs: (a) DC characteristics, (b) AC characteristics. L_G = 18nm, t_{ox} = 9A, V_{DD} = 0.7V, L_{eff} = 22nm, SP = 2*L_G.

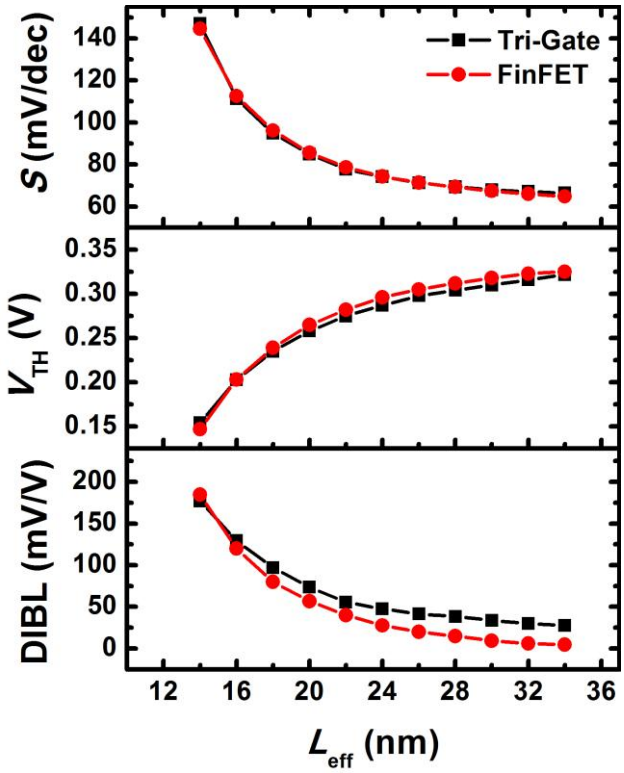

Fig. 3.3. L_{eff} dependence of subthreshold swing S, saturation threshold voltage V_{TH}, and DIBL for the tri-gate and FinFET designs. L_G = 18nm, t_{os} = 9A, $X_{J,SD}$ = 1.2*H_{STRIPE}, t_{Si} = H_{STRIPE}, V_{DD} = 0.7V.

MOSFET shows less sensitivity to L_{eff} because it relies on the retrograde channel doping in addition to the tri-gated channel geometry to achieve good electrostatic integrity. Thus, at short L_{eff}, it has DIBL similar to that for the FinFET.

3.4.2 AC Characteristics

3-D simulated total gate-to-source/drain capacitance (C_{total}) is shown in Fig. 3.2b. Following [15], C_{total} includes the intrinsic gate-to-source/drain capacitance C_{GS} and the capacitance from fringing electric fields (C_{TSB}) between the gate electrode and the top and sidewalls ($C_{fG\text{-}T/S}$), as well as the bottom ($C_{fG\text{-}B}$) of the Si stripe ($C_{TSB} = C_{fG\text{-}T/S}+C_{fG\text{-}B}$, as illustrated schematically in Fig. 3.4). Because the stripe pitch has been assumed to be the same for both the FinFET and tri-gate MOSFET in this work, and the FinFET has a narrower and taller stripe, the thickness and height of the gate electrode along the channel-stripe sidewalls are larger for the FinFET design. As a result, C_{TSB} for the FinFET is larger than for the tri-gate MOSFET. Note that C_{TSB} does not scale with W_{eff} (*i.e.* $C_{total} = C_{TSB}+C_{GS}*W_{eff}$); extrapolating C_{total} to zero W_{eff} gives C_{TSB} as shown in Fig. 3.5. For L_G = 18nm and a stripe pitch of $2*L_G$, the FinFET and tri-gate MOSFET have C_{TSB} values of 6.50 aF and 4.73 aF, or 41.4% and 33.0% of C_{total} at V_{GS} = 0V, respectively. Only by aggressively reducing the FinFET stripe pitch can C_{TSB} be reduced; for instance, if the stripe pitch of the FinFET is reduced to $2*W$ (where $W = 0.6*L_G$), C_{TSB} decreases to 4.57 aF or 34.6% of C_{total} at V_{GS} = 0V, but this narrow stripe pitch would result in reduced manufacturability due to lithography and etch limitations. For L_G = 13nm and a stripe pitch of $2*L_G$, the FinFET and tri-gate MOSFET have C_{TSB} values of 3.82 and 1.81 aF at V_{GS} = 0V, respectively.

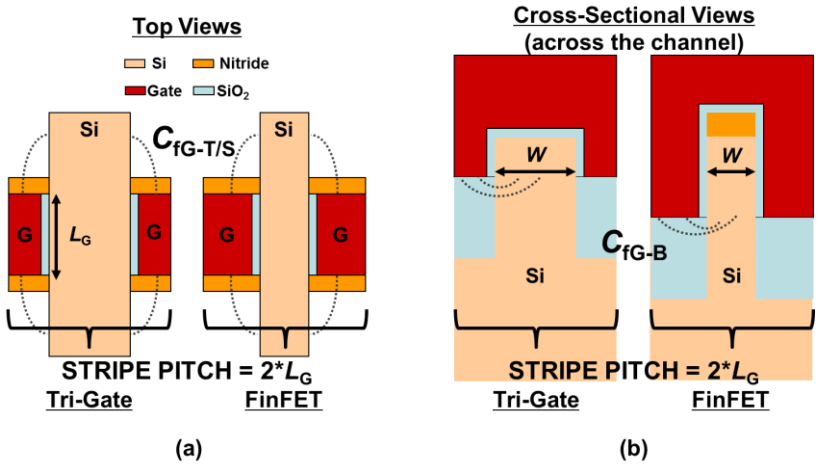

Fig. 3.4. Illustration of parasitic capacitances in multi-gate MOSFET structures. (a) Gate-to-top/sidewall capacitance $C_{fT\text{-}G/S}$, (b) Gate-to-substrate capacitance $C_{fG\text{-}B}$. $C_{TSB} = C_{fG\text{-}T/S}+C_{fG\text{-}B}$.

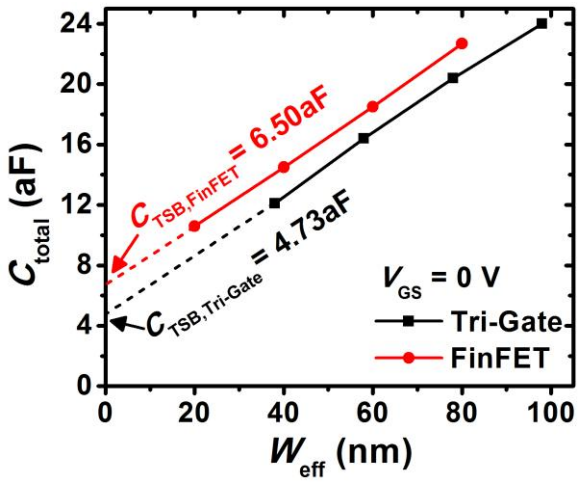

Fig. 3.5. C_{total} as a function of W_{eff} for the tri-gate and FinFET design. C_{TSB} is extrapolated at W_{eff} = 0nm. L_G = 18nm, H_{STRIPE}=0.8*L_G.

At high V_{GS}, where the intrinsic C_{GS} capacitance dominates, the tri-gate MOSFET still has lower $C_{total,}$ in part because the top gate shares part of the channel with the sidewall gates in the corner regions, resulting in an electrical stripe width that is less than W_{eff}. For the double-gate FinFET, there are no corners, and the electrical stripe width equals W_{eff}. Thus, the tri-gate has less C_{GS} for the same physical W_{eff} while still achieving comparable I_{ON}.

3.4.3 I_{ON} and Intrinsic Delay Dependence on L_{eff}

Figs. 3.6a and 3.6b show the L_{eff} dependencies of I_{ON} and intrinsic delay, respectively, for the tri-gate MOSFET with different values of H_{STRIPE}, W = 1*L_G, and channel SP = 2*L_G = 2*W. It can be seen from Fig. 3.6b that the optimal design with larger H_{STRIPE} has larger L_{eff} (wider gate-sidewall spacers, smaller C_{TSB}) and smaller minimum intrinsic delay. As L_{eff} is reduced, I_{ON} and intrinsic delay are degraded because of degraded SCE. (The gate overdrive is reduced because the threshold voltage must increase to meet the I_{OFF} specification.) The tri-gate MOSFET design with W = 2*L_G and channel stripe pitch = 4*L_G shows poorer intrinsic delay (Fig. 3.7b) because the sidewall gates are too far from the center of the channel to adequate suppress SCE for such a thick t_{Si}. The degraded SCE negatively impacts I_{ON}, consistent with a larger scale length [16]. For the FinFET design with SP = 2*L_G, a larger value of H_{STRIPE} is advantageous to achieve smaller delay, since the ratio of C_{TSB} over total gate capacitance is smaller (Fig. 3.8b). Based on the results in Figs. 3.6, 3.7, and 3.8, the FinFET design with H_{STRIPE} = 1.1*L_G is optimal to maximize I_{ON}, whereas the tri-gate bulk MOSFET design with W = 1*L_G is optimal to minimize intrinsic delay, assuming SP = 2*L_G for both designs. The intrinsic delay of the FinFET can be reduced by ~90 fs if SP is reduced to 2*W (where W = 0.6*L_G); however, this scenario is unlikely given that the smallest reported SP value for FinFETs to date is 2*L_G [3].

Although retrograde doping gradients only as steep as 3 nm/dec have been reported [11], Fig. 3.9 shows the effect of retrograde channel doping gradient on MOSFET performance, even for

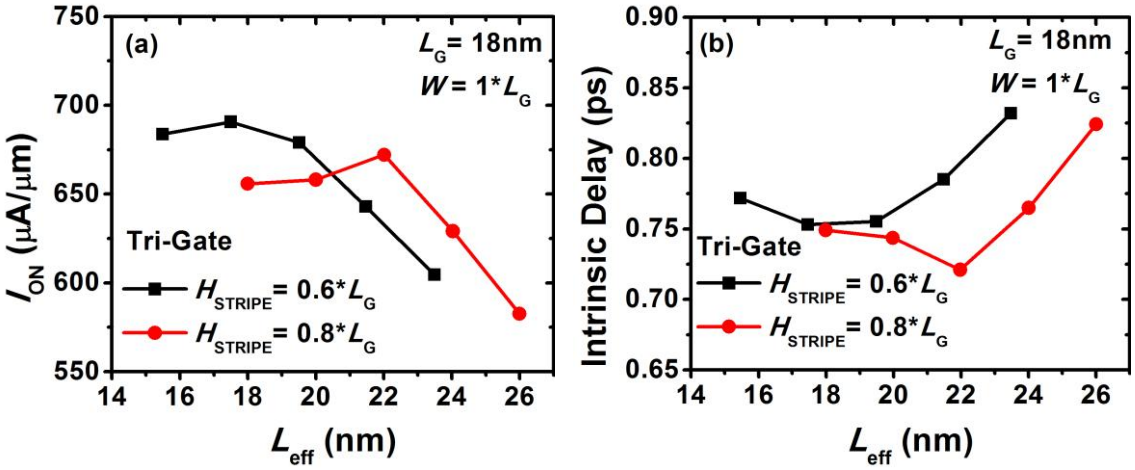

Fig. 3.6. Tri-gate bulk MOSFET design optimization for channel stripe width $W = L_G$. (a) I_{ON} vs. L_{eff}, for I_{OFF} = 7 nA/μm, (b) Delay vs. L_{eff}. L_G = 18nm, t_{ox} = 9A, $X_{J,SD}$ = 1.2*H_{STRIPE}, t_{Si} = H_{STRIPE}, V_{DD} = 0.7V.

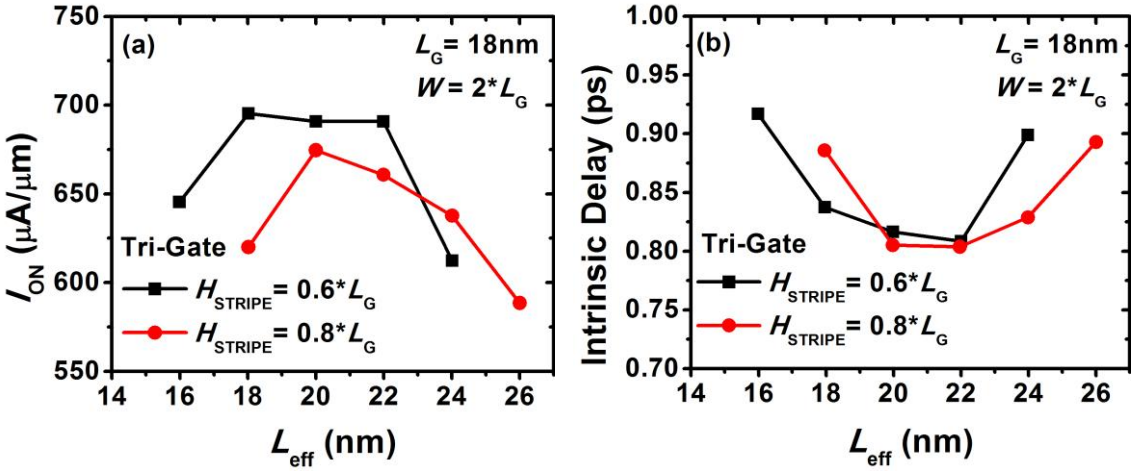

Fig. 3.7. Tri-gate bulk MOSFET design optimization for channel stripe width $W = 2*L_G$. (a) I_{ON} *vs.* L_{eff}, for I_{OFF} = 7 nA/μm, (b) Delay *vs.* L_{eff}. L_G = 18nm, t_{ox} = 9A, $X_{J,SD}$ = 1.2*H_{STRIPE}, t_{Si} = H_{STRIPE}, V_{DD} = 0.7V.

gradients steeper than 3 nm/dec. For the tri-gate MOSFET, there exists an optimal value of retrograde doping gradient that optimizes the trade-off between improved average carrier mobility (due to reduced transverse electric field with increasing depth of retrograde doping) and improved SCE suppression (with decreasing depth of retrograde doping); for the FinFET design, which relies on a thin body (*i.e.* small *W*) instead of retrograde channel doping to suppress SCE, the retrograde doping gradient generally should be as steep as possible in order to maximize the average carrier mobility. Assuming that an abrupt retrograde doping profile can be achieved in the bulk FinFET, the lowest achievable intrinsic delay is similar for the optimized FinFET and tri-gate MOSFET designs, for SP = 2*L_G. However, considering practical doping gradient limits (*i.e.* 3 nm/dec), the optimal tri-gate MOSFET design has better intrinsic delay for both L_G =

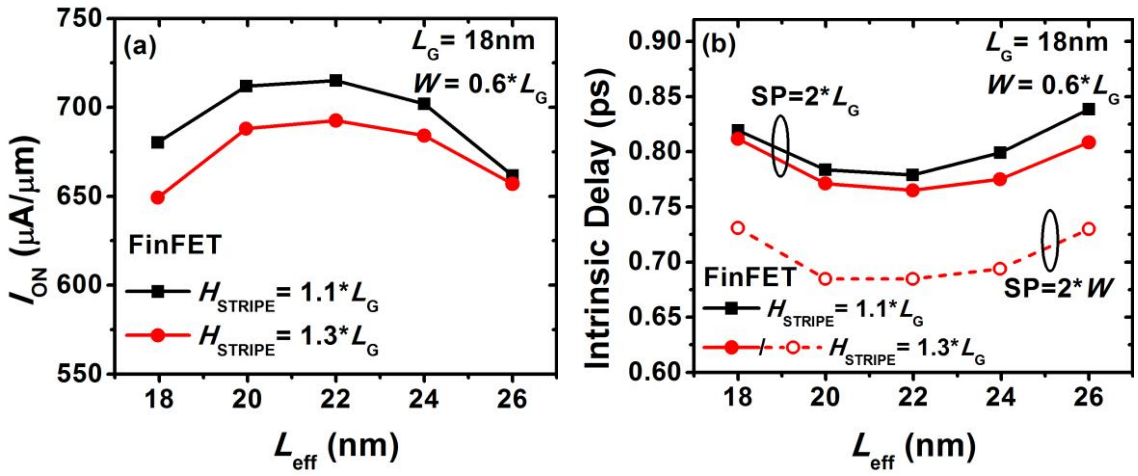

Fig. 3.8. FinFET bulk MOSFET design optimization. (a) I_{ON} vs. L_{eff}, for I_{OFF} = 7 nA/μm, (b) Delay vs. L_{eff}. L_G = 18nm, W = 0.6*L_G, t_{ox} = 9A, $X_{J,SD}$ = 1.2*H_{STRIPE}, t_{Si} = H_{STRIPE}, V_{DD} = 0.7V. Solid lines are for SP = 2*L_G; dashed line is for SP = 2*W.

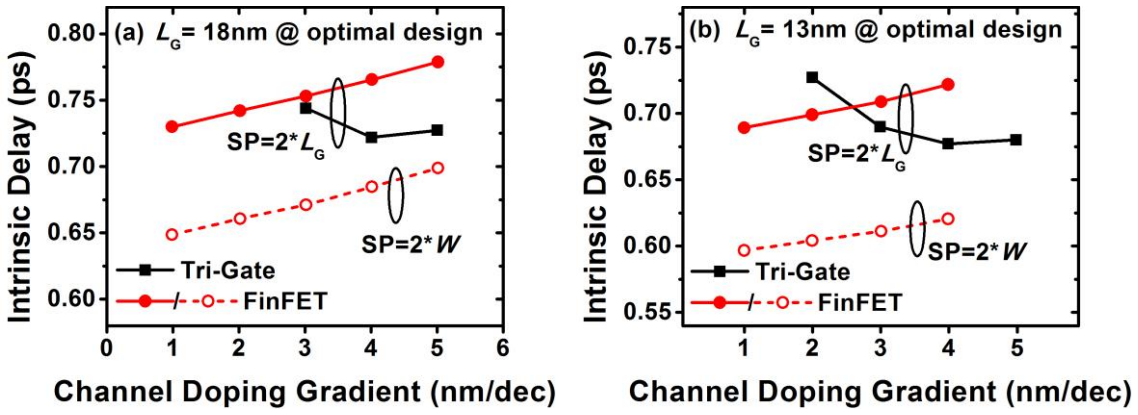

Fig. 3.9. Impact of retrograde channel doping gradient on the performance of tri-gate bulk and FinFET bulk MOSFETs. For the tri-gate design, W = 1*L_G, H_{STRIPE} = 0.8*L_G; for the FinFET design, W = 0.6*L_G, H_{STRIPE} = 1.3*L_G. (a) L_G = 18nm, t_{ox} = 9A, t_{Si} = H_{STRIPE}, V_{DD} = 0.7V, (b) L_G = 13nm, t_{ox} = 8A, t_{Si} = H_{STRIPE}, V_{DD} = 0.6V. Solid lines are for SP = 2*L_G; dashed line is for SP = 2*W.

18nm and L_G = 13nm. Therefore, the optimal retrograde channel doping gradient for the tri-gate design is less steep than that for the FinFET design, is easier to attain in practice, and provides for better performance. Although lower delay can be achieved in principle by reducing SP (ref. Fig. 3.9), there are no published reports to date which demonstrate this.

Table 3.1 summarizes the parameters for the optimized tri-gate and FinFET bulk MOSFET designs with SP = 2*L_G. For the same stripe pitch, the tri-gate bulk MOSFET design offers comparable (or even less) delay with less aggressive features (stripe width, stripe aspect ratio, retrograde doping gradient) for improved manufacturability.

TABLE 3.1
OPTIMAL DESIGNS FOR TRI-GATE AND FINFET BULK MOSFETS

PARAMETER		FinFET		Tri-Gate	
Design Parameters					
L_G	Gate length (nm)	18	13	18	13
T_{ox}	Gate oxide thickness (nm)	0.9	0.8	0.9	0.8
--	Gate workfunction (eV)	4.51	4.55	4.35	4.34
L_{eff}	Effective channel length (nm)	22	17	22	17
--	W_{STRIPE}/L_G	0.6	0.6	1.0	1.0
--	H_{STRIPE}/L_G	1.3	1.3	0.8	0.8
--	Retrograde well gradient (nm/dec)	1	1	4	4
Performance Metrics					
I_{ON}	On-state current (μA/μm) (I_{OFF} = 7 nA/μm)	754	592	673	531
τ	Delay (C_{total} * V_{DD}/ ($2I_{eff}$) (ps)	0.73	0.69	0.72	0.68

†SP = 2*L_G

3.5 Random Variability in the SegFET and FinFET

Two large sources of random variability as L_G is scaled are RDF and gate line-edge roughness (LER). Because the bulk tri-gate requires the use of retrograde channel doping to help suppress SCE, the effect of RDF on variability is likely worse compared to FinFETs. However, due to LER, the FinFET has discrete different L_G on the two fin sidewalls whereas the LER variation is averaged over the wider bulk tri-gate stripe. In [17], the effect of RDF and LER-induced variation is quantified with TCAD. Kinetic Monte Carlo simulations [9] were used to simulate RDF in the SegFET and FinFET. Note that the FinFETs in these simulations are for an SOI substrate instead of bulk substrate (*i.e.* there is no retrograde channel doping at the base of the fin), so that this analysis represents the best-case scenario for the FinFET. Gate LER is sampled from a scanning electron micrograph of extreme ultraviolet resist profiles, with LER (3σ) of 4nm and line-width roughness (LWR) of 6.4nm. Fig. 3.10a shows the V_T variation due to simulated RDF and LER in the bulk tri-gate and SOI FinFET. Taking into account both RDF and LER, the bulk tri-gate MOSFET has similar random V_T variation compared to the SOI FinFET, even though the FinFET has no channel doping. In addition to RDF and LER, the FinFET V_T is more sensitive to W_{STRIPE} variation (Fig. 3.10b) since it relies on geometric confinement instead of retrograde channel doping to control SCE.

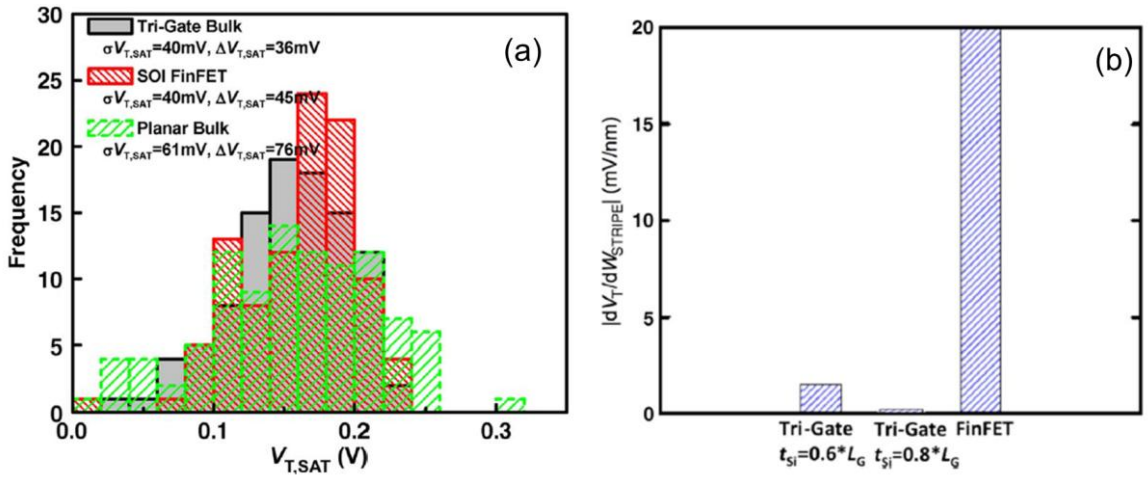

Fig. 3.10. (a) RDF and LER-induced V_T variation for the bulk tri-gate, SOI FinFET, and planar bulk MOSFET structures. L_G=20nm, H_{STRIPE} = 0.6*L_G. (b) Simulated V_T sensitivity to W_{STRIPE} variation. From [17].

3.6 Summary

As compared with the bulk FinFET design, the tri-gate bulk MOSFET design can achieve comparable intrinsic delay. Although the optimized FinFET design has 12% higher on-state current compared to the optimized tri-gate bulk MOSFET, the tri-gate bulk MOSFET has lower parasitic capacitance. The channel stripe height/width aspect ratio is lower for the tri-gate bulk MOSFET (0.8 *vs.* 2.17) than for the bulk FinFET, and the retrograde channel doping profile can be less steep for the tri-gate bulk MOSFET (4 nm/dec *vs.* 1 nm/dec) than for the bulk FinFET to minimize delay. Thus, the tri-gate bulk MOSFET design is advantageous for ease of manufacturing, especially as device pitch continues to scale in future technology nodes. It should be noted that the bulk FinFET can achieve better layout area efficiency and intrinsic delay if the height of the channel stripe is increased and/or the stripe pitch is aggressively reduced, at the cost of reduced manufacturability. Taking into consideration a balance of performance and manufacturability, the tri-gate bulk MOSFET is a promising structure for CMOS transistor scaling to the end of the technology roadmap.

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Chapter 4

Silicon-Germanium Alloys for p-channel MOSFETs

4.1 Introduction

The preceeding chapters discussed evolutionary and revolutionary transistor structures to continue gate length scaling. To further improve performance, strain technology has been developed; for instance, embedded silicon-germanium ($Si_{1-x}Ge_x$) source/drain stressors are used in state-of-the-art CMOS technologies to effectively boost hole mobility and p-channel MOSFET (pMOSFET) performance [1]. In addition to strain, the use of a high-mobility channel material also has been explored as an approach to enhance transistor performance (especially for high-performance applications) [2]. Although some III-V systems have been shown to provide very high hole mobilities [3]-[4], germanium (Ge) and silicon-germanium alloys ($Si_{1-x}Ge_x$) are attractive because they also offer higher low-field hole mobilities than Si [5]-[6] and can be more easily integrated into a Si CMOS process flow.

Recent work has demonstrated high performance Ge and $Si_{0.65}Ge_{0.35}$ pMOSFETs for gate length (L_G) down to 20 nm [7]-[8] with reasonable off-state currents. Higher Ge concentration (X_{Ge}) within a $Si_{1-x}Ge_x$ channel is beneficial for increasing hole mobility, but it is detrimental for scaling due to decreased bandgap energy (E_G) and increased dielectric permittivity which exacerbate band-to-band tunneling (BTBT) [9] and SCE, respectively. However, if the $Si_{1-x}Ge_x$ channel is very thin (e.g. < 5 nm), BTBT can be suppressed because E_G is effectively increased by quantization effects [10]. Furthermore, SCE are suppressed for very thin $Si_{1-x}Ge_x$ channels since the amount of higher-permittivity material (and hence the penetration of the drain electric field which affects the source-side potential barrier) is reduced.

If the $Si_{1-x}Ge_x$ channel is epitaxially grown on a Si substrate below a critical thickness (T_{crit}), it will be under biaxial compressive strain due to the lattice mismatch between Si and $Si_{1-x}Ge_x$. (The lattice constants of Si and Ge are 5.43Å and 5.65Å, respectively.) This strain splits the

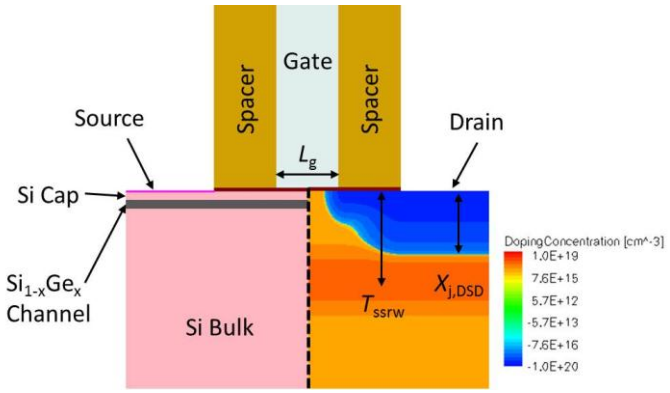

Fig. 4.1: Composite schematic cross-section illustrating the heterostructure channel (left) and doping profiles and parameters (right) of the bulk pMOSFET device.

energy degeneracy within the valence band so that inter-subband scattering is reduced and hence hole mobility is increased [11]. Thus, the use of a very thin $Si_{1-x}Ge_x$ channel on Si is promising for boosting pMOSFET performance while maintaining reasonable scalability. Since phonon scattering increases due to increased quantum confinement in very thin channels [12]-[13], however, it is important to carefully examine the mobility enhancement in thin $Si_{1-x}Ge_x$ channels as a function of X_{Ge} and channel thickness (T_{SiGe}). In this chapter, the enhancement of inversion-layer hole mobility in thin $Si_{1-x}Ge_x$ channels with various stressors is investigated via numerical simulations. The benefit of the $Si_{1-x}Ge_x$-channel heterostructure for pMOSFET performance is then assessed through TCAD simulations of devices with L_G of 18 nm.

4.2 Modeling Approach

4.2.1 Mobility Calculation Methodology

The pMOSFET heterostructure channel and doping profiles each are illustrated in Fig. 4.1. The $Si_{1-x}Ge_x$ is assumed to be coherently strained to maintain the same lattice constant as the underlying (001) Si substrate, and this $Si_{1-x}Ge_x$ layer is capped with an ultra-thin unstrained layer of Si to provide for a good interface with the gate dielectric [14]. A standard channel crystalline orientation ((001)/[110]) is assumed. The subband structure of the $Si_{1-x}Ge_x$ heterostructure channel is computed for a one-dimensional MOS capacitor structure using a self-consistent 6×6 $k \cdot p$ Poisson-Schrödinger solver. The Luttinger parameters for $Si_{1-x}Ge_x$ are extracted using the empirical pseudopotential method (EPM) [15], and a third-order polynomial expression is used to compute the parameters over the range $0.0 < X_{Ge} < 1.0$. Strain in the $Si_{1-x}Ge_x$ channel is taken into account using the Pikus-Bir strain Hamiltonian [16].

Inversion-layer hole mobility is calculated using the Kubo-Greenwood formalism. Acoustic phonon scattering, optical phonon scattering, alloy scattering, and surface roughness scattering

TABLE 4.1
PARAMETERS FOR MOBILITY CALCULATIONS

Parameter	UNITS	Material	
		Si	**Ge**
γ_1	–	$4.1+3.8X_{Ge}-7.7X_{Ge}^2+8.8X_{Ge}^3$	
γ_2	–	$0.3+1.9X_{Ge}-4.4X_{Ge}^2+4.8X_{Ge}^3$	
γ_3	–	$1.3+1.8X_{Ge}-3.9X_{Ge}^2+4.5X_{Ge}^3$	
Δ_{SO}	eV	0.043	0.297
a_v	eV	2.05	-0.35
b	eV	-2.1	-2.86
d	eV	-4.9	-6.06
$\hbar\omega$	meV	62.0	38.0
D_{ac}	eV	9.2	11
D_tK	eV/cm	13.0×10^8	6.0×10^8
Δ_{rms}	nm	0.8	--
$L_{correlation}$	nm	3.0	--

Material parameter values used for the 6×6 $k \cdot p$ mobility calculations. $\gamma_{1,2,3}$ are the Luttinger parameters used for 6×6 $k \cdot p$ method; Δ_{SO} is the split-off band energy separation; a_v, b, d, are the absolute, biaxial, and shear strain deformation potentials, respectively; $\hbar\omega$ is the optical phonon energy; D_{ac} and D_tK are the acoustic and optical deformation potential for holes, respectively; and Δ_{rms} and $L_{correlation}$ are the surface rms roughness and correlation length, respectively.

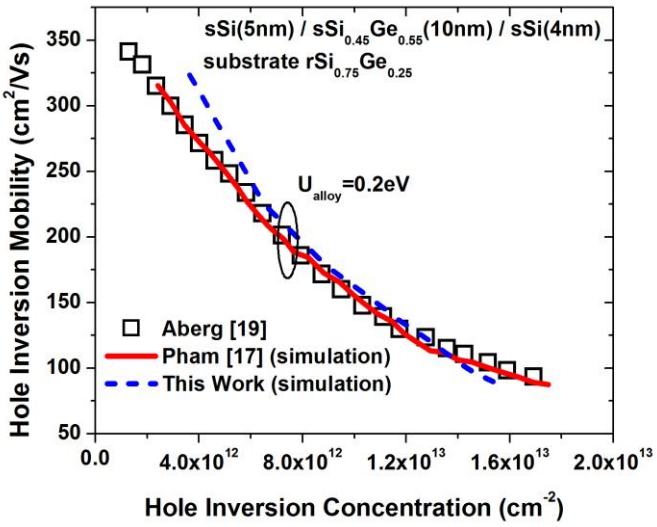

Fig. 4.2: Calibration of the mobility simulator to experimental and simulation data. The device structure comprises a strained-Si/strained-$Si_{0.45}Ge_{0.55}$/strained-Si heterostructure channel on a relaxed $Si_{0.75}Ge_{0.25}$ virtual substrate, as reported in [19].

are considered in the mobility calculation and are treated similarly as in Ref. 17. The form factor [16] is calculated separately for each layer of the heterostructure channel, and scattering between the semiconductor layers is neglected [17]. Table 4.1 lists the phonon energies and deformation potentials for relaxed Si and Ge, from which the phonon scattering parameters and deformation potentials for $Si_{1-x}Ge_x$ alloys are linearly interpolated. Alloy scattering within the $Si_{1-x}Ge_x$ layer is fitted using an alloy scattering potential (U_{alloy}) [18]. The interface between Si and $Si_{1-x}Ge_x$ is assumed to be ideal, and surface roughness scattering is taken into account only for the Si/SiO_2 interface. Surface roughness parameters are also shown in Table I.

Experimental mobility data for $Si_{1-x}Ge_x$ heterostructure channels [19] as well as previous simulation results [17] were used to calibrate and validate the parameters used in this study. Fig. 4.2 shows good agreement of the mobility simulator results to experimental data if a U_{alloy} value of 0.2 eV is used, which is the same value of U_{alloy} used in [17].

4.2.2 TCAD Simulation Methodology

Sentaurus Device [20] is used to assess the benefit of the mobility gains provided by the heterostructure channel for improving pMOSFET performance for L_G = 18 nm. The gate dielectric is assumed to be SiO_2 with a thickness (T_{OX}) of 1 nm, and the default value of the Si cap thickness (T_{CAP}) is 1 nm. The Si_3N_4 gate-sidewall spacers each have a length of 15 nm. Following ITRS specifications [21], the deep-source/drain (DSD) junctions have a depth ($x_{j,DSD}$) of 22 nm and peak doping of 10^{20} cm^{-3}. The length of the DSD regions is set at 24 nm. The source/drain extensions (SDE) also have peak doping of 10^{20} cm^{-3} and are laterally offset from the gate edge by 2 nm. The retrograde well doping profile, with a peak concentration of 10^{19} cm^{-3}, is used to optimize the effective channel length (L_{eff}) by adjusting the well depth (T_{SSRW}) and doping abruptness to achieve the highest drive current for an off-state leakage current specification (I_{OFF}) of 100 nA/μm (appropriate for high-performance applications [21]) while maintaining drain-induced barrier lowering (DIBL) below 100 mV/V, at a supply voltage (V_{DD}) of 0.8 V. L_{eff} is separately optimized for each combination of X_{Ge} and T_{SiGe}.

Conventional drift-diffusion (DD) models are used to simulate the on-state drive current (I_{ON}). The mobility data from the 6×6 $k \cdot p$ solver is implemented in *Sentaurus* by adjusting the fitting parameters of a model based on [22], which can successfully capture the mobility dependence on channel layer thickness and transverse electric field. One weakness of the DD model is that at high electric fields or short L_G, non-stationary transport effects such as velocity overshoot cannot be physically captured; instead, DD relies on a saturation velocity model. To overcome this, a heuristic approach is used in which the thermal injection velocity is extracted from the 6×6 $k \cdot p$ bandstructure by calculating the group velocity at each point in k-space and integrating over all k-space and subbands [23]; the default saturation velocity value is then replaced by this calculated injection velocity. Although this approach still cannot model velocity overshoot in the channel, it does correctly capture the trend of increasing injection velocity with increasing X_{Ge} (in contrast to the bulk saturation velocity which decreases with increasing X_{Ge}); if the device is operating close to the ballistic regime, this approach also sets the correct upper limit on injection velocity at the source [24]. To take into account quantization effects due to the thin $Si_{1-x}Ge_x$ channel, a one-dimensional Schrödinger equation is solved within the $Si_{1-x}Ge_x$ channel

and Si cap region using hole masses linearly interpolated between those of Si and Ge. E_G of the $Si_{1-x}Ge_x$ channel is adjusted for biaxial compressive strain induced valence-band offsets as calculated in [25] for $Si_{1-x}Ge_x$ grown pseudomorphically on Si. Linear interpolation is also used to derive the dielectric constant and effective density of states (DOS) of the $Si_{1-x}Ge_x$ channel. As it is difficult to model every subtle effect of the $Si_{1-x}Ge_x$ heterostructure channel architecture (such as DOS dependence on strain and non-stationary transport effects), the TCAD simulation results will not be quantitatively precise but are intended to provide qualitative insight for $Si_{1-x}Ge_x$ heterostructure channel design optimization.

4.3 Results and Discussion

4.3.1 Mobility Impact of $Si_{1-x}Ge_x$ Heterostructure Channel Design

Subband energy splitting due to biaxial strain reduces inter-subband scattering and thereby increases mobility. Fig. 4.3 shows a contour plot of hole mobility at an inversion-layer concentration (P_{inv}) of 10^{13} cm^{-2} as a function of T_{SiGe} and X_{Ge}. It can be seen that hole mobility generally increases with X_{Ge}. For low X_{Ge}, there is little mobility dependence on T_{SiGe} because the valence-band offset between $Si_{1-x}Ge_x$ and Si is negligible so that there is little confinement of holes to the $Si_{1-x}Ge_x$ channel. As X_{Ge} increases, the valence-band offset and hence hole confinement increase. As a result, carriers experience more phonon scattering [26] and hence have degraded mobility in thinner $Si_{1-x}Ge_x$ channels. The $Si_{1-x}Ge_x$ thickness beyond which the

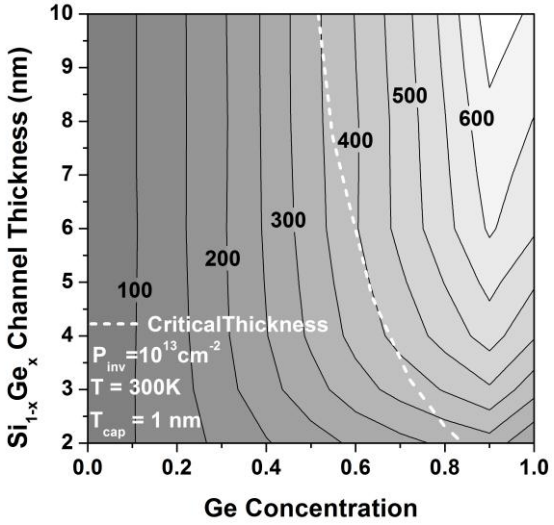

Fig. 4.3: Inversion-layer hole mobility contour plot for a $Si/Si_{1-x}Ge_x/Si$ heterostructure channel. Contour lines are shown for increments of 50 $cm^2 V^{-1} s^{-1}$.

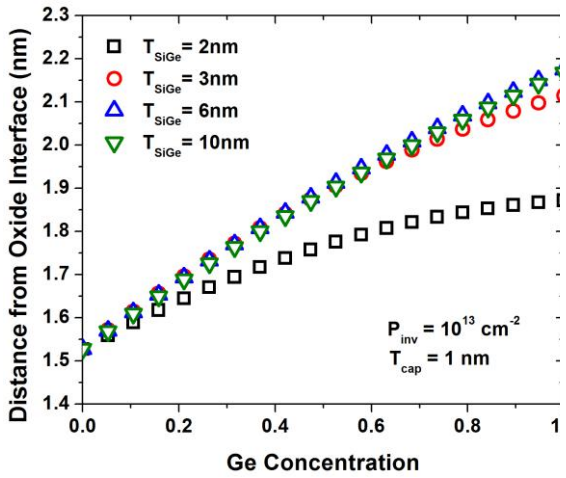

Fig. 4.4: Hole inversion-layer centroid distance from gate-oxide interface *vs*. X_{Ge} for various T_{SiGe}. T_{CAP} = 1 nm.

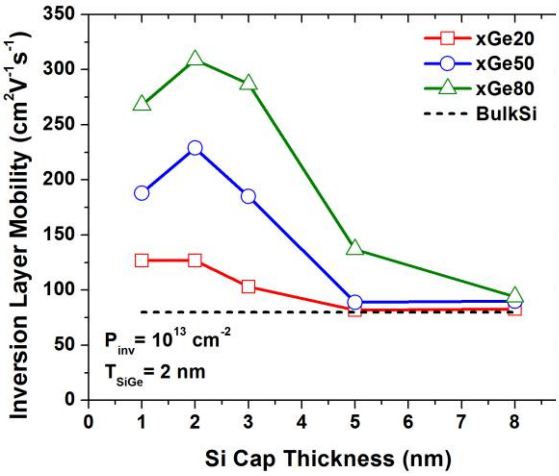

Fig. 4.5: Dependence of inversion-layer hole mobility on T_{CAP} for various X_{Ge}.

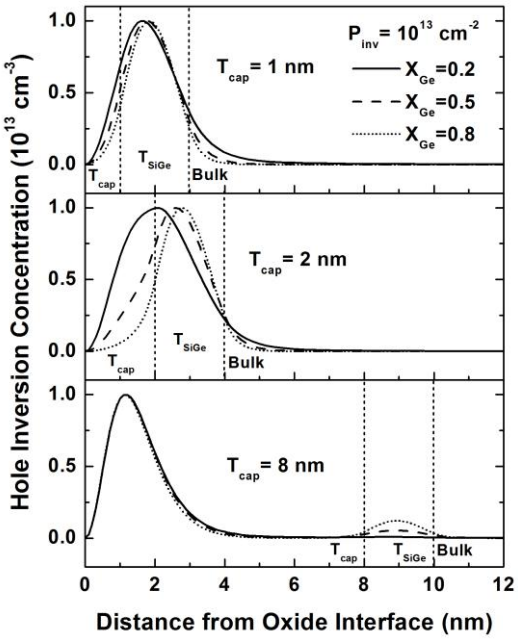

Fig. 4.6: Inversion-layer hole concentration depth profile for various T_{CAP} and X_{Ge} (T_{SiGe} = 2 nm).

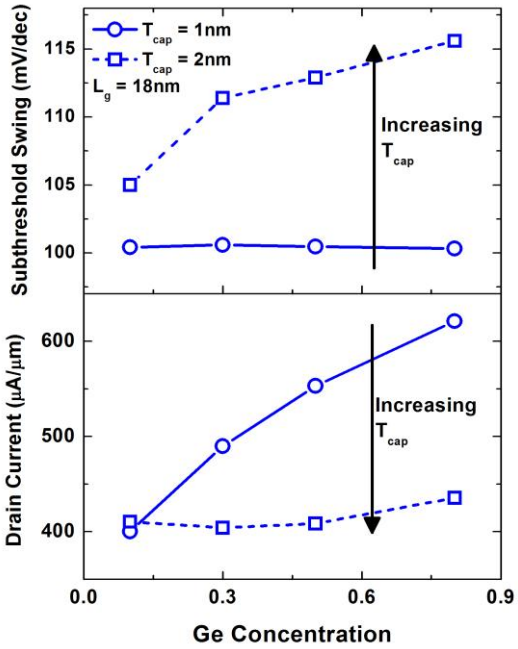

Fig. 4.7: Subthreshold swing (top) and drain current (bottom) as a function of X_{Ge} for T_{CAP} = 1 nm or 2 nm.

strain from the lattice mismatch relaxes by creating line defects (*i.e.*, T_{crit}) [27] is indicated in Fig. 4.3. Taking into account this thickness constraint and the mobility degradation for very thin T_{SiGe}, the maximum mobility achievable is ~400 $cm^2V^{-1}s^{-1}$ at X_{Ge} = 0.6 and T_{SiGe} = 5 nm.

Fig. 4.4 plots the distance between the peak of the inversion-layer charge distribution and the gate-oxide interface as a function of X_{Ge}, for various values of T_{SiGe}. From this figure, the peak moves further away from the gate oxide interface as X_{Ge} and T_{SiGe} increase. Therefore, to maintain sufficient capacitive coupling between the gate and the channel at short L_G, T_{SiGe} must be kept thin (< 2 nm), especially for large X_{Ge}. The impact of T_{CAP} on hole mobility is shown in Fig. 4.5 for various values of X_{Ge}. Mobility peaks at T_{CAP} = 2 nm and then decays to the bulk-Si mobility value as the fraction of the inversion-layer holes in the Si cap increases with increasing T_{CAP} (Fig. 4.6). Although hole mobility is maximized for T_{CAP} = 2 nm, I_{ON} is maximized for T_{CAP} = 1 nm due to improved gate control. This can be seen from Fig. 4.7, which compares the subthreshold swing (S) and I_{ON} values for optimized 18 nm $Si_{1-x}Ge_x$-channel pMOSFETs (with DIBL < 100 mV/V) for T_{CAP} values of 1 nm and 2 nm. Note that the S of L_G = 18 nm devices with T_{CAP} = 2 nm degrades much faster with increasing X_{Ge}, resulting in a lower gate overdrive and reduced I_{ON}.

4.3.2 Mobility Impact of CESL-Induced Uniaxial Compressive Stress

To assess the impact of uniaxial compressive stress induced by a contact etch-stop liner (CESL), 500 MPa of compressive stress (in addition to the biaxial strain induced by the underlying Si substrate) was simulated in the $Si_{1-x}Ge_x$ channel and Si cap layers. Uniaxial compressive stress not only breaks the degeneracy in the heavy and light hole bands, but also warps the bands and reduces the effective mass [11], so that it is more effective for increasing mobility as compared to biaxial compressive strain. The mobility contour plot in Fig. 4.8 shows that the addition of uniaxial compressive stress enhances mobility by ~1.5× so that a maximum

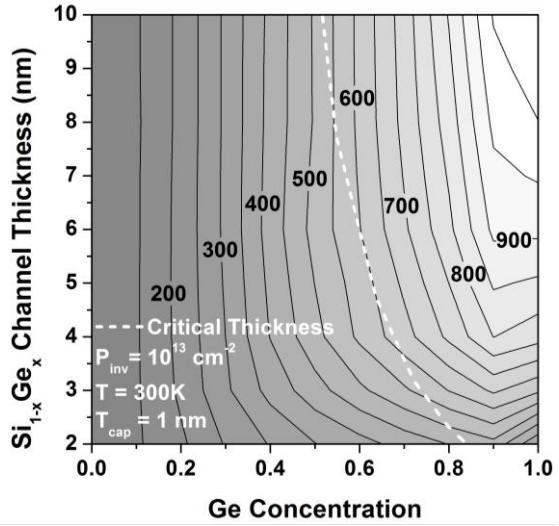

Fig. 4.8: Inversion-layer hole mobility contour plot for a pMOSFET with $Si/Si_{1-x}Ge_x/Si$ heterostructure channel and CESL stressor (500 MPa uniaxial compressive stress). Contour lines are shown for increments of 50 $cm^2 V^{-1} s^{-1}$

mobility of ~600 $cm^2V^{-1}s^{-1}$ is reached at X_{Ge} = 0.6 and T_{SiGe} = 5 nm. Thus, the addition of uniaxial stress is beneficial for a $Si_{1-x}Ge_x$ heterostructure channel.

4.3.3 Mobility Impact of Embedded-Source/Drain-Induced Uniaxial Compressive Stress

Sentaurus Process simulations are used to model the stress profile within a pMOSFET with embedded $Si_{0.6}Ge_{0.4}$ ($eSi_{0.6}Ge_{0.4}$) stressors. The Ge concentration is fixed at 40% (a practical upper limit) for the embedded stressors. The pocket shape of the $eSi_{0.6}Ge_{0.4}$ regions (Fig. 4.9) is similar to that reported in [28], with a pocket depth of 22 nm. The pocket "notch" is located midway through the $Si_{1-x}Ge_x$ channel thickness at the edge of the gate electrode, and for the simulation parameters used, the stress induced in the channel is not very sensitive to the vertical position of the notch.

From these process simulations, it is found that after the etching step to recess the silicon in the source/drain regions, the original biaxial compressive strain within the $Si_{1-x}Ge_x$ channel partially relaxes (a similar effect observed in narrow-width strained $Si_{1-x}Ge_x$ channel pMOSFETs [29]), as shown in Fig. 4.9. Afterwards, the uniaxial stress induced in the channel by the $eSi_{0.6}Ge_{0.4}$ stressors may not be sufficient to compensate for this loss in stress, especially for large X_{Ge} and T_{SiGe} values. Fig. 4.10 plots the level of additional uniaxial stress induced at the center of the channel by the $eSi_{0.6}Ge_{0.4}$ stressors, as a function of T_{SiGe} and for various values of X_{Ge}. It can be seen that the additional compressive stress induced in the channel by the $eSi_{0.6}Ge_{0.4}$ stressors decreases with increasing X_{Ge} and T_{SiGe}, so that the net impact of the

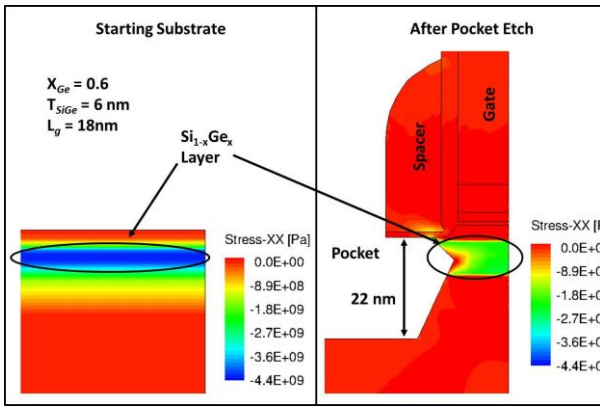

Fig. 4.9: Stress contour plots showing the $Si/Si_{1-x}Ge_x/Si$ heterostructure (left) and the $Si/Si_{1-x}Ge_x$/Si-channel pMOSFET structure after pocket etch (right) for subsequent growth of $eSi_{0.6}Ge_{0.4}$ stressors.

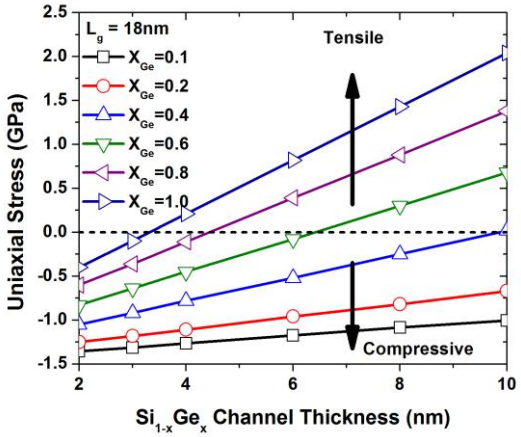

Fig. 4.10: Additional uniaxial stress at the center of the $Si_{1-x}Ge_x$ channel induced by $eSi_{0.6}Ge_{0.4}$ stressors.

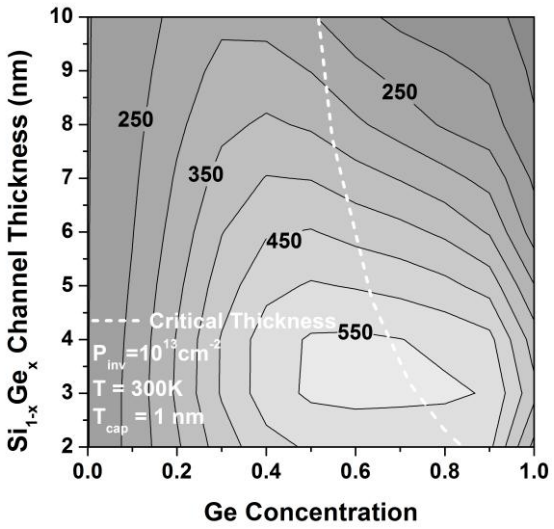

Fig. 4.11: Inversion-layer hole mobility contour plot for a pMOSFET with $Si/Si_{1-x}Ge_x/Si$ heterostructure channel and $eSi_{0.6}Ge_{0.4}$ stressors. Contour lines are shown for increments of 50 $cm^2 V^{-1} s^{-1}$.

$eSi_{0.6}Ge_{0.4}$ stressors is to induce tensile channel stress at large X_{Ge} and T_{SiGe} values. Because of the partial relaxation of the $Si_{1-x}Ge_x$ channel during the $eSi_{0.6}Ge_{0.4}$ formation process, hole mobility does not monotonically increase with increasing X_{Ge} and T_{SiGe}, which is reflected in the mobility contour plot in Fig. 4.11. The maximum achievable mobility (taking into account the critical thickness constraint) in Fig. 4.11 is similar to the maximum achievable mobility for the CESL-stressed configuration (at $P_{inv} = 10^{13}$ cm^{-2}). However, for lower X_{Ge} values ($X_{Ge} < 0.4$), the mobility is improved by 2x – 2.5x and by 1.5x – 2x over the intrinsic biaxial strain and CESL-stressed configurations, respectively, showing that $eSi_{0.6}Ge_{0.4}$ stressors can provide more mobility improvement than CESL for $X_{Ge} < 0.4$.

4.3.4 MOSFET Performance

The contour plots in Fig. 4.12a show I_{ON} (for a constant I_{OFF} = 100 nA/μm) from TCAD device simulations of an L_G = 18 nm $Si_{1-x}Ge_x$ heterostructure p-channel MOSFET, for the intrinsic biaxial strain configuration. I_{ON} reaches a maximum at X_{Ge} = 0.7, T_{SiGe} = 2 nm, representing a ~65% improvement over the bulk-Si device (X_{Ge} = 0.0). For thicker values of T_{SiGe}, the device has worse SCE and the resultant reduction in gate overdrive lowers I_{ON}, especially for high values of X_{Ge} (large dielectric constant); the higher mobilities for larger values of T_{SiGe} are negated by the accompanying degradation in electrostatic integrity. Thus, T_{SiGe} should be kept very thin (~2 – 3 nm).

Fig. 4.12b is the I_{ON} contour plot for the CESL-stressed configuration. (Note: The stress-enhanced mobility in the bulk-Si device, *i.e.* for X_{Ge} = 0, calculated from the 6x6 $k \cdot p$ solver was fitted with the same TCAD model used for the heterostructure device.) Transistor drive current

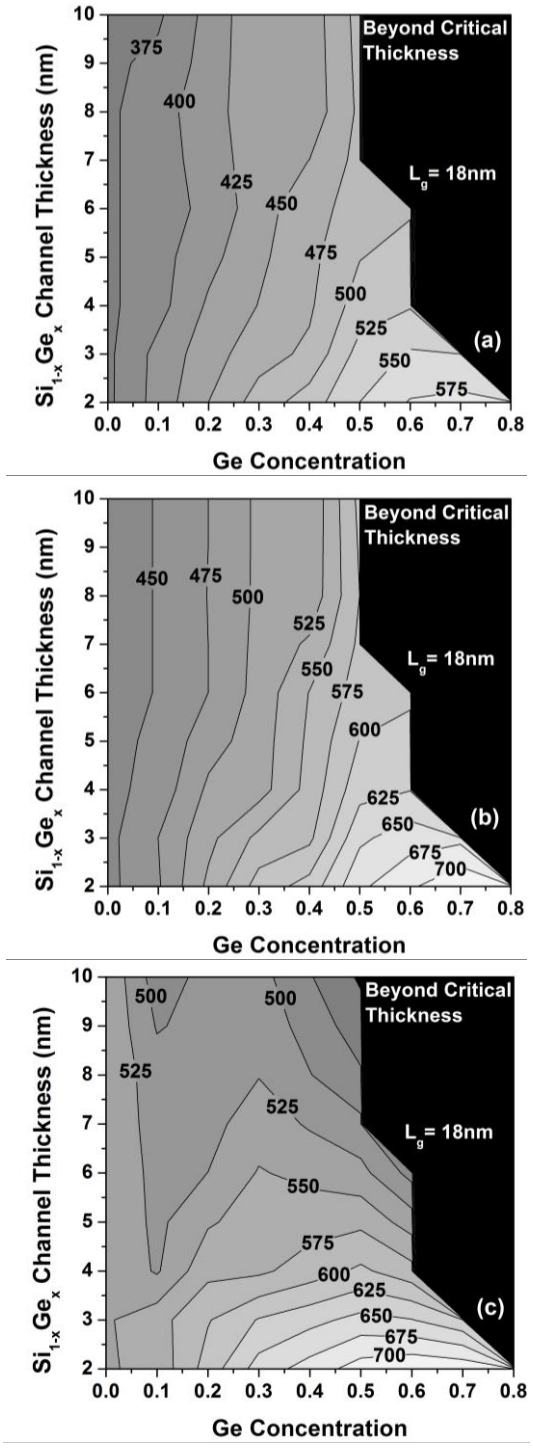

Fig. 4.12: I_{ON} (in µA/µm) achieved with a L_G = 18 nm $Si/Si_{1-x}Ge_x/Si$ heterostructure channel structure (at a constant I_{OFF} = 100 nA/µm) for pMOSFETs with (a) intrinsic biaxial strain, (b) 500 MPa CESL stress, and (c) $eSi_{0.6}Ge_{0.4}$ stressors. Contour lines are shown for increments of 25 µA/µm

is enhanced as compared with the intrinsic biaxial strain configuration, and the same trends are seen with increasing X_{Ge} and T_{SiGe}. Again, ~65% improvement over the bulk-Si device (X_{Ge} = 0.0) is achieved at X_{Ge} = 0.7, T_{SiGe} = 2 nm.

Fig. 4.12c is the I_{ON} contour plot for the $eSi_{0.6}Ge_{0.4}$-stressed configuration. (The uniaxial channel stress in the bulk-Si channel device, *i.e.* for X_{Ge} = 0, is extrapolated from Fig. 10.) In contrast to the results for the intrinsic biaxial and CESL-stressed configurations, the I_{ON} contours mirror the mobility contours. As explained above, the $Si_{1-x}Ge_x$ channel partially relaxes due to the $eSi_{0.6}Ge_{0.4}$ stressor formation process, reducing the maximum mobility that can be achieved; thus, the maximum I_{on} for the $eSi_{0.6}Ge_{0.4}$-stressed configuration is similar to that for the CESL-stressed configuration, and the maximum performance improvement over the bulk-Si device (X_{Ge} = 0.0) is ~30% at X_{Ge} = 0.6, T_{SiGe} = 2 nm. Note, however, that for X_{Ge} < 0.4, I_{on} for the $eSi_{0.6}Ge_{0.4}$-stressed configuration shows improvement over the CESL-stressed configuration, showing the efficacy of the $eSi_{0.6}Ge_{0.4}$ stressors.

For all three stress cases, the highest I_{ON} is achieved at very high X_{Ge} and very thin T_{SiGe}. However, it is important to note that at higher X_{Ge}, I_{ON} is more sensitive to T_{SiGe} (*i.e.* the contour lines are spaced more closely together). This increased sensitivity would result in more process-induced variation. It has also been experimentally shown that $Si_{1-x}Ge_x$ channels with higher X_{Ge} have more sensitivity to layout geometry [29]. In addition, the coefficient of Ge diffusion in the $Si_{1-x}Ge_x$ channel will also increase with larger X_{Ge} and stress, making it more difficult to maintain the integrity of the $Si_{1-x}Ge_x$ channel [30] during the fabrication process. Due to these process-related issues, the optimal $Si_{1-x}Ge_x$ heterostructure channel should have thin T_{SiGe} and moderate X_{Ge} ($0.2 < X_{Ge} < 0.4$).

4.4 Summary

Calculations of $Si_{1-x}Ge_x$ heterostructure channel hole mobility show that the enhancement over Si channel hole mobility generally increases with increasing Ge content (X_{Ge}) and that the use of uniaxial stressors can provide additional mobility improvements. TCAD simulations are used to assess the implications for pMOSFET performance, to provide qualitative guidance for X_{Ge} and T_{SiGe} optimization. Since short-channel effects worsen with increasing $Si_{1-x}Ge_x$ thickness, enhancement in I_{ON} is generally maximized at low values of T_{SiGe} (2 – 3 nm). The maximum I_{ON} enhancement provided by a $Si_{1-x}Ge_x$ heterostructure channel as compared with a bulk-Si channel is ~65% (depending on X_{Ge} and the stressor used). However, due to process-induced variability considerations, a moderate value of X_{Ge} ($0.2 < X_{Ge} < 0.4$) is optimal. For these ranges of T_{SiGe} and X_{Ge}, the I_{ON} enhancement provided by the $Si_{1-x}Ge_x$ heterostructure channel ranges from 10% to 40% for a p-channel MOSFET with 18 nm gate length.

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Chapter 5

$Si_{1-x}Ge_x$/Si p-Channel SegFETs for Improved I_{ON} and Reduced Variability

5.1 Introduction

As mentioned in Chapter 4, silicon-germanium alloy ($Si_{1-x}Ge_x$) has been investigated as an alternative channel material for p-channel MOSFETs (pMOSFETs) due to the higher hole mobility compared to silicon (Si) [1]-[3]. Because of its higher dielectric constant, however, only a thin $Si_{1-x}Ge_x$ should be used, avoiding increasing drain-induced barrier lowering (DIBL) [4]. $Si_{1-x}Ge_x$/Si heterostructure pMOSFETs have been demonstrated to have enhanced mobility at narrower device widths, due to the transformation of biaxial strain (in the as-grown $Si_{1-x}Ge_x$) into uniaxial strain after active-area patterning. This effect is amplified for high Ge concentration channels, which leads to increased layout complexity and places an upper bound on the amount of Ge that can be incorporated – and thus limits the amount of mobility improvement achievable – in a practical $Si_{1-x}Ge_x$ channel technology [5]. Ideally, all transistors on a chip with $Si_{1-x}Ge_x$ channels should have the same width to avoid this layout width-dependent behavior.

Instead of impractically constraining all transistors to be of the same width, the channel area can be segmented into parallel stripes of equal width to achieve the same effect. The effective channel width of this segmented-channel device is then adjusted by changing the layout width of the active region to change the number of channel stripes which it encompasses. This device structure is essentially a segmented-channel MOSFET (SegFET), as described in Chapter 2, and can be used to mitigate the adverse layout width-dependent behavior of $Si_{1-x}Ge_x$ channel devices.

In this work, the beneficial combination of the SegFET design for reduced layout-width dependencies and the $Si_{1-x}Ge_x$/Si heterostructure channel for enhanced mobility and performance are experimentally demonstrated.

5.2 Device Fabrication

SegFETs are fabricated using a conventional planar process, but starting with a substrate that has a corrugated semiconductor surface (comprising stripes of equal width, isolated by VSTI regions) instead of a planar wafer. In this work, the corrugated substrate was formed using the "etch-epi" method by first depositing a layer of SiO_2 (the VSTI material) on the Si substrate and applying double patterning to form 20nm-wide SiO_2 lines and 80nm-wide spaces (trenches). 20nm of Si was then selectively epitaxially grown in the trenches followed by a thin $Si_{0.5}Ge_{0.5}$ channel layer. A 3nm-thick Si capping layer was grown on top of the $Si_{0.5}Ge_{0.5}$ channel layer to provide a better interface to the gate oxide. The same epitaxial growth was performed on planar wafers for fabrication of the control devices. In this work, a 2nm-thick $Si_{0.5}Ge_{0.5}$ channel layer was grown on both the corrugated and planar control wafers to assess the impact of segmenting the active channel region. A 5nm-thick $Si_{0.5}Ge_{0.5}$ channel layer also was grown on a separate corrugated substrate to assess the effect of increasing the $Si_{0.5}Ge_{0.5}$ channel layer thickness for SegFETs. Challenges to achieving high-quality epitaxial material with minimal defects included: (1) maintaining a pristine Si surface prior to epitaxy, (2) tightly controlling *in-situ* and auto-doping within the epitaxial layers, and (3) controlling the faceting of the $Si_{1-x}Ge_x$ epitaxy to prevent overgrowth onto the VSTI. A cross-sectional TEM (X-TEM) in Fig. 5.1 compares the corrugated substrate before and after optimizing the epitaxial process conditions [6].

Note that the geometrical regularity of the channel region is assured so long as the active-area pattern encompasses an integral number of channel stripes; that is, no variability in effective channel width is introduced by a non-rectangular active-area pattern for a SegFET, in contrast to a conventional MOSFET.

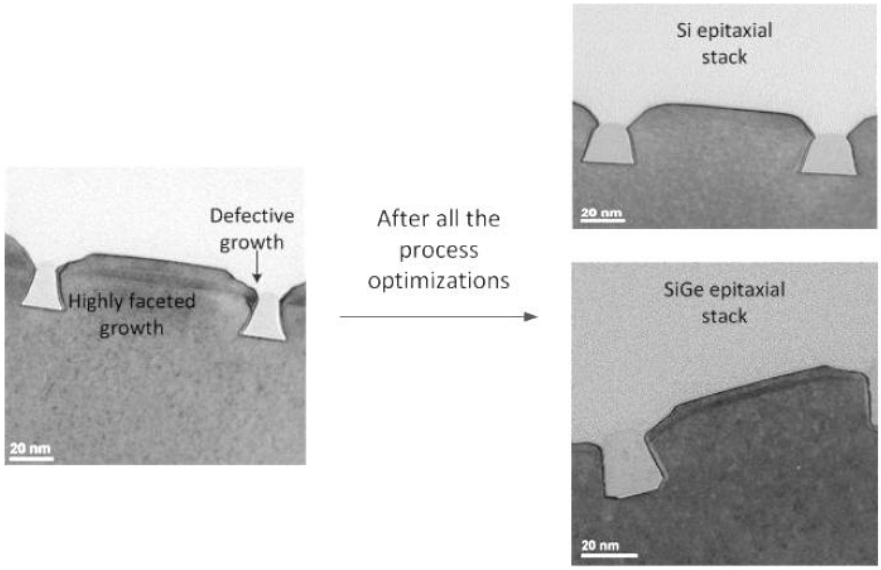

Fig. 5.1. X-TEM of the corrugated substrate before (left) and after (right) epitaxial growth process optimization.

After the corrugated and planar control substrates were fabricated, a conventional planar bulk process was then used to achieve sub-70nm L_G pMOSFETs. In addition to the epitaxially-grown SegFET and planar control wafers, the same process was also applied to planar bulk Si wafers for Si reference devices. First, the active-area was patterned, followed by the growing of a thermal gate-oxide layer at 750°C. *In-situ* boron doped poly-$Si_{1-x}Ge_x$ was deposited as the gate material and was patterned using a combination of resist ashing and oxide hardmask trimming. After gate patterning and reoxidation, phosphorus and BF_2 ion implantation steps were performed to form the halo and SDE regions, respectively. Low-temperature-oxide (LTO) spacers were formed, followed by BF_2 ion implantation to form the source/drain regions. The implanted dopants were activated with a 10s 900°C rapid thermal anneal. After deposition of a LTO passivation layer, contact hole formation, and Al/2%Si metallization, the devices were sintered in forming gas at 400°C. Process details are found in Appendix B.

The cross-sectional transmission electron micrograph (X-TEM) along the poly-$Si_{1-x}Ge_x$ gate in Fig. 5.2 shows the SegFET device after fabrication; the VSTI oxide is tapered at the top and the channel stripes are very slightly elevated above the VSTI surface, resulting in 90nm effective stripe width. Fig. 5.3 shows an X-TEM of the channel/oxide interface for the as-grown 2nm-thick $Si_{0.5}Ge_{0.5}$ channel; after fabrication, the thickness of the $Si_{1-x}Ge_x$ channel increased to ~2.5nm. For the as-grown 5nm-thick $Si_{0.5}Ge_{0.5}$ channel, the $Si_{1-x}Ge_x$ thickness increased to ~7nm after processing (not shown). The gate oxide thickness is ~2.3nm and is consistent for all experimental splits. Note that the Si capping layer is not apparent; this is likely due to Si consumption during the cleaning and oxidation processes, and Ge diffusion from the $Si_{1-x}Ge_x$ layer during device fabrication.

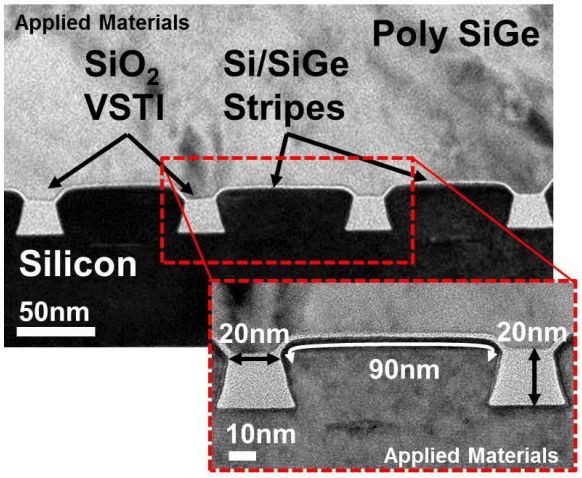

Fig. 5.2. X-TEM of SegFET along the gate. Active stripes and VSTI oxide are 90 nm and 20 nm wide, respectively.

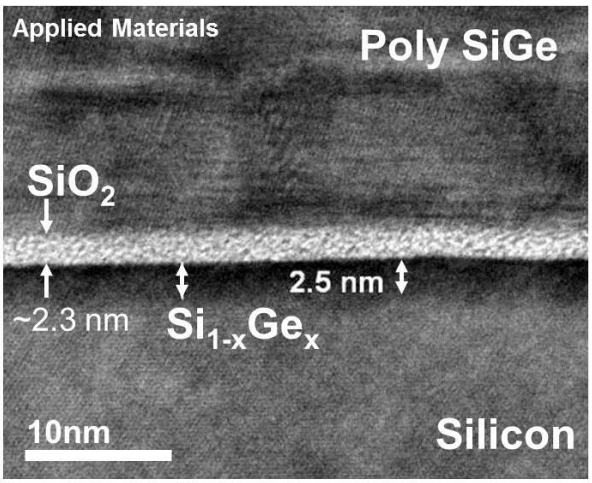

Fig. 5.3. X-TEM of the channel showing a diffused 2.5nm $Si_{1-x}Ge_x$ layer. The Si cap was consumed during fabrication.

5.3 Electrical Results and Discussion

5.3.1 Benefits of Using a Corrugated Substrate

Split capacitance-voltage (C-V) measurements of a 2.5nm-thick $Si_{1-x}Ge_x$ channel SegFET are shown in Fig. 5.4. C-V curves with similar characteristics were also seen for the other experimental splits. There is minimal frequency dispersion and only a slight bump in the depletion regime for low frequencies, indicating a good quality gate oxide/channel interface, despite the fact that the Si capping layer is not apparent in the X-TEM. In addition, there is no increase in capacitance at high inversion bias, which is further indication that the Si capping layer has been entirely consumed in the fabrication process.

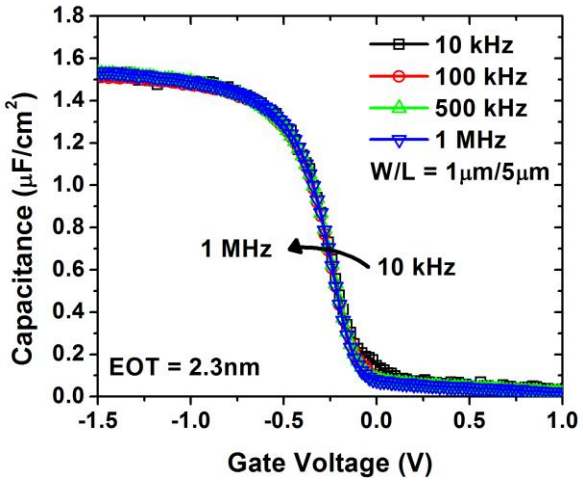

Fig 5.4. Split-*CV* curves of the SegFET at various frequencies show good oxide interface quality (same as control devices).

Measured transfer characteristics of the 2.5nm-thick $Si_{1-x}Ge_x$ channel SegFET and planar devices are shown in Fig. 5.5 for L_G=115nm and 75nm; output characteristics are shown in Fig. 5.6 for L_G=115nm. Note that the plotted transistor currents are normalized to the layout width. The SegFETs show slightly higher linear $|V_T|$, which may be due in part to reduced biaxial strain [7] (resulting in a concomitant increase in uniaxial strain) due to the selective epitaxial growth of the channel regions in stripes rather than across the entire wafer. In addition, as L_G is reduced, the SegFET shows better subthreshold swing and DIBL compared to the planar control device. From both the transfer and output characteristics, the SegFETs show larger current per unit layout width for the same gate overdrive (V_{GT}), despite having 10% smaller effective channel

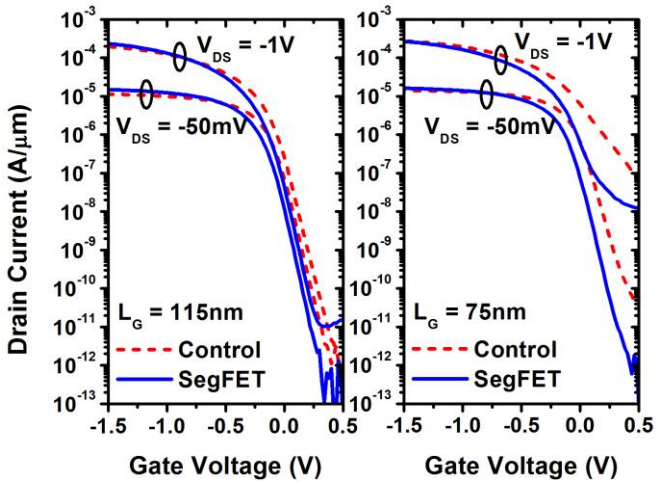

Fig 5.5. I_DV_G for L_G = 115 nm (left) and 75nm (right) of the SegFET and control devices. Current is per μm layout width. Layout width is 0.25 μm.

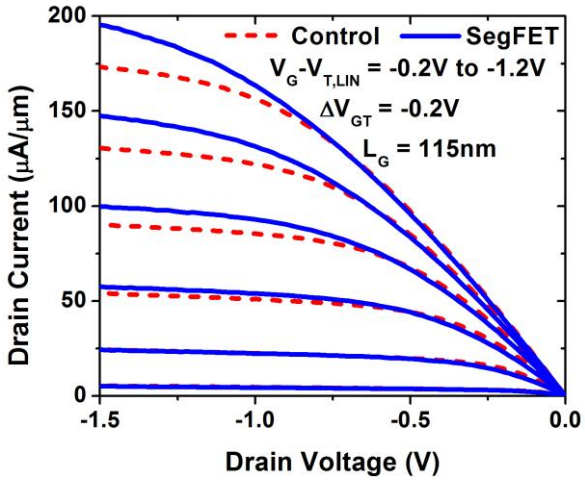

Fig 5.6. I_DV_D of L_G = 115 nm for the SegFET and control devices. Current is per μm layout width. Layout width is 0.25 μm.

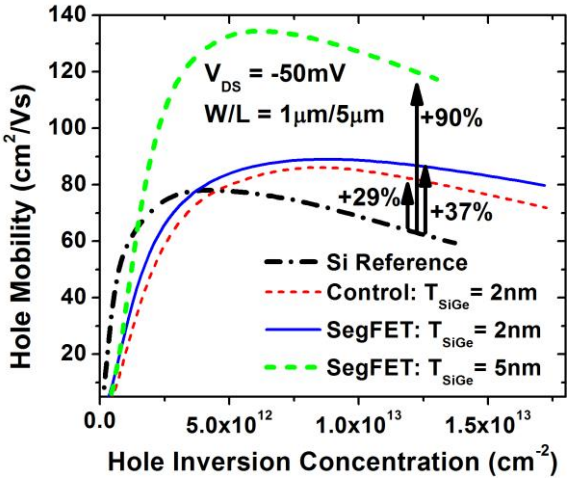

Fig 5.7. Mobility curves for SegFET and control devices. Layout width is 1μm.

width. The improved drive current is partly a result of higher effective mobility as shown in Fig. 5.7. The hole mobilities of the control and SegFET devices with 2nm $Si_{1-x}Ge_x$ channel are 29% and 37% higher, respectively, as compared to the Si reference device, at a hole inversion concentration (P_{INV}) of 1.2 x 10^{13} cm^{-2}. The SegFET exhibits higher mobility than the control device, especially at higher hole inversion concentration, which again can be attributed to changes in $Si_{1-x}Ge_x$ channel strain and reduced transverse electric field within the segmented channel stripes. (At lower P_{inv}, mobility is limited by higher Coulombic scattering.) Degradation of saturation V_T ($V_{T,SAT}$) and DIBL with gate-length scaling is somewhat mitigated for the SegFETs (Figs. 5.8-5.9), and can be better suppressed by slightly recessing the VSTI oxide and/or reducing W_{STRIPE} to improve gate control. The improved mobility and short-channel control of the SegFET boost I_{ON} by 30% in comparison to the $Si_{1-x}Ge_x$-channel control device and an additional 40% in comparison to the Si reference device, for I_{OFF} = 10nA/um (Fig. 5.10).

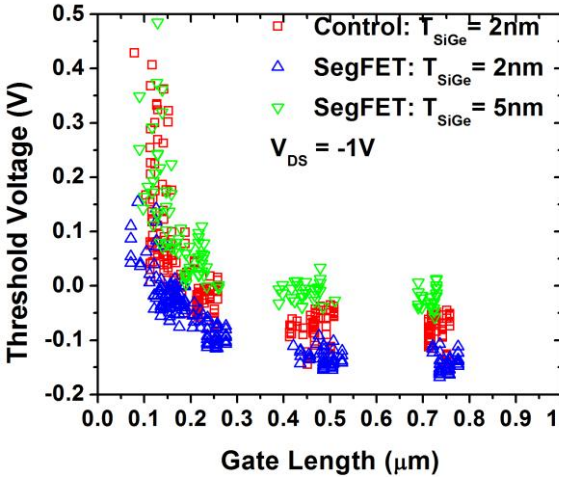

Fig 5.8. $V_{T,SAT}$ of planar control and various SegFET devices for different L_G.

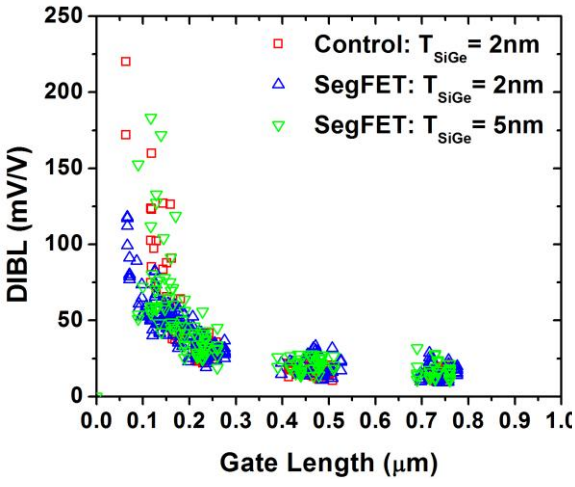

Fig 5.9. DIBL of the planar control and various SegFET devices for different L_G.

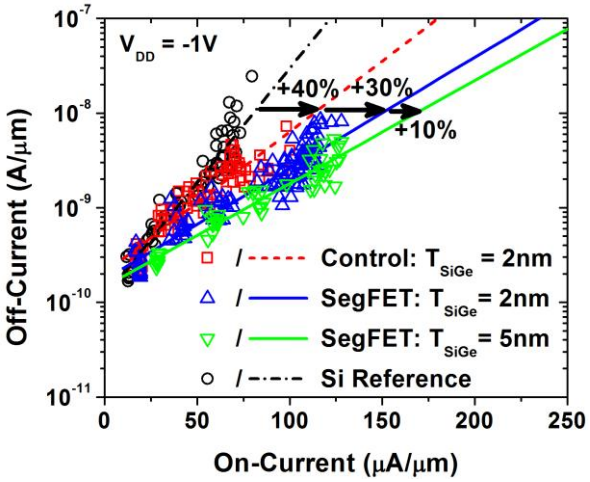

Fig 5.10. Log(I_{OFF})-I_{ON} per μm layout width for the planar control and various SegFET devices. Layout width is 1μm.

5.3.2 Impact of $Si_{1-x}Ge_x$ Channel Thickness on SegFET Performance

From Fig. 5.7 it can be seen that by increasing the thickness of the $Si_{1-x}Ge_x$ channel from 2.5nm to 7nm, the mobility enhancement over the reference Si device increases from 37% to 90% at P_{INV} = 1.2 x 10^{13} cm^{-2}. This large improvement is due to reduced confinement of the hole wavefunction and subsequent reduction in phonon scattering, as described in [8] and also experimentally observed in [9]. However, a thicker $Si_{1-x}Ge_x$ channel region also degrades the electrostatic integrity of the SegFET, as evidenced by the worse short-channel effects seen in Figs. 5.8-5.9. The net effect is that the thicker $Si_{1-x}Ge_x$ channel results in a relatively small (10%) improvement in I_{ON} at I_{OFF} = 10 nA/um, as compared to the thinner $Si_{1-x}Ge_x$ channel.

5.3.3 Comparison of Layout Width Dependence

Fig. 5.11 shows the change in $V_{T,SAT}$ ($\Delta V_{T,SAT}$), referenced to $V_{T,SAT}$ for a device with 1 μm layout width, as a function of layout width, for control and SegFET devices. Because of the geometrical regularity of the SegFET channel region, $\Delta V_{T,SAT}$ is reduced from 30mV for the control device to 9mV and 6mV for the thin- and thick-$Si_{1-x}Ge_x$-channel SegFETs, respectively, at 0.25 μm layout width. The small but nonzero variation with layout width seen for the SegFETs is due to misalignment of the active-area mask to the corrugated substrate, resulting in narrower channel stripe(s) at the active region edge(s). Smaller layout widths and better alignment accuracy could not be achieved due to the limitations of the photolithographic exposure tool used in this work, which has an alignment accuracy of +/- 45 nm and can only reliably resolve features as small as 0.25 μm (without using special linewidth-narrowing techniques). The exposure tools used in modern CMOS manufacturing facilities have better alignment accuracy (within 20 nm) so that the active area can be aligned to the corrugated substrate to encompass an integer number of channel stripes.

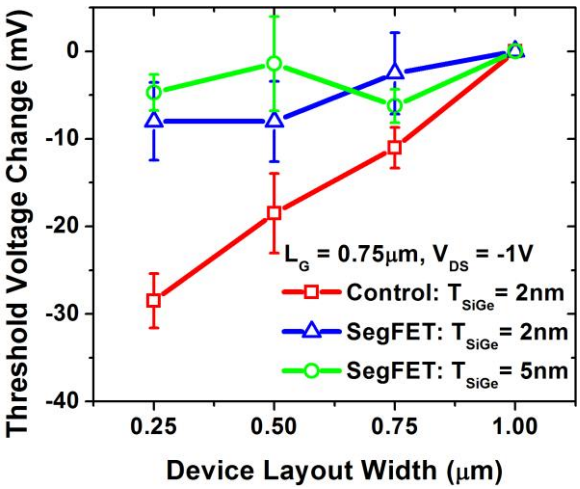

Fig 5.11. $\Delta V_{T,SAT}$ for control and SegFET devices, for different layout widths. The error bars indicate +/- one standard deviation in $\Delta V_{T,SAT}$. L_G = 0.75 μm.

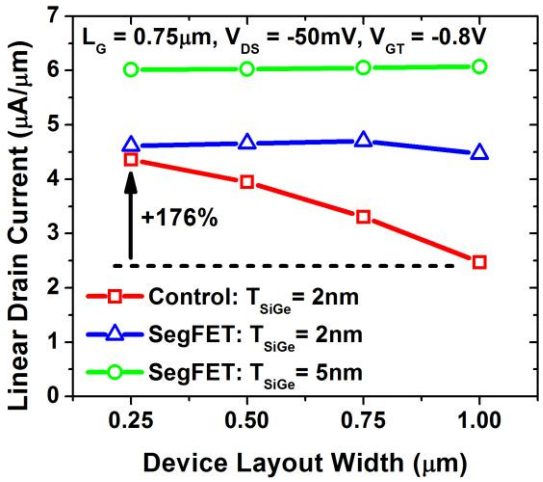

Fig 5.12. $I_{D,LIN}$ of the planar control and various SegFET devices for different layout widths. Current is per μm layout width. L_G = 0.75μm.

Fig. 5.12 shows that the SegFETs have dramatically reduced dependence of linear drain current on layout width. (The linear drain currents were extracted at $|V_G-V_T|$ = 0.8 V, where V_T is defined at a constant current of 70nA*W/L_G.) This is in contrast to the control devices, for which the normalized current increases by 176% with decreasing layout width as the biaxial channel strain changes to uniaxial channel strain.

5.4 Summary

Fabrication of $Si_{1-x}Ge_x$/Si pMOSFETs on a corrugated substrate results in improved performance (better layout efficiency) due to higher hole mobility and improved electrostatic

control, and reduced variability due to geometrical regularity of the channel region. This allows the use of higher Ge concentration channels to maximize mobility and performance. Corrugated substrate technology is therefore advantageous for facilitating continued CMOS scaling and the adoption of high-mobility channel materials.

5.5 References

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Chapter 6

Ge Channels for Scaling to the End of the Roadmap

6.1 Introduction

The previous chapters investigated the use of silicon-germanium ($Si_{1-x}Ge_x$) alloys to improve MOSFET performance. In this chapter, pure germanium (Ge) channels will be studied for implementation in high-performance digital applications near the fundamental limit of transistor scaling. Historically, high-performance Ge n-channel MOSFETs (nMOSFETs) have been difficult to achieve due to degraded field-effect mobility and high contact resistance [1-2]. Although recent improvements in Ge gate dielectric interface and contact resistance for Ge nMOSFETs have been demonstrated [3-5], recent experimental results for Ge p-channel MOSFETs (pMOSFETs) [6-7] using mature and conventional processing techniques show more immediate promise. Therefore, this chapter focuses on Ge pMOSFET scaling to the end of the International Technology Roadmap for Semiconductors (ITRS).

Uniaxial compressive strain is currently used in state-of-the-art CMOS technologies to enhance Si pMOSFET performance. Monte Carlo (MC) simulations have shown that strained-Ge pMOSFETs can achieve higher drive currents than strained-Si pMOSFETs, for gate length (L_G) down to 15 nm [8-9]. Since the introduction of high-mobility channel materials has been pushed out to future CMOS technology generations (beyond the 15 nm node), it is important to assess the benefit of Ge pMOSFETs for even shorter L_G. Due to the higher dielectric permittivity of Ge, suppression of short-channel effects will be even more challenging for Ge MOSFETs than for Si MOSFETs and can limit their performance benefits at very short gate lengths. Also, the lower electron and hole masses for Ge result in larger direct tunneling between the source and the drain in the off state. Since direct source-to-drain tunneling (DSDT) leakage current sets the ultimate limit for channel-length scaling (for a given off-state leakage current specification), a Ge MOSFET is less scalable than a Si MOSFET. DSDT has been

studied for Ge n-channel MOSFETs [10] but not for Ge p-channel MOSFETs. In this work, DSDT and MC simulations are used to assess the potential performance benefit of Ge for high-performance (HP) pMOSFETs near the end of the ITRS (L_G down to 8 nm).

6.2 Modeling Approach

6.2.1 Simulation Methodology

The *Sentaurus* device simulator within the *Sentaurus* TCAD software suite [11] was used to optimize the geometry of the pMOSFET to obtain the highest on-state drive current (I_{ON}) for the 2009 ITRS HP off-state leakage current (I_{OFF}) specification of 100 nA/um [12]. This design optimization was done using drift-diffusion (DD) simulations. The only material parameters modified for Ge device simulation are the bulk electron and hole mobilities, energy bandgap, dielectric constant, and the effective density of states for holes and electrons. The values of these parameters are summarized in Table 6.1. Although DD simulation cannot accurately predict the magnitude of I_{ON} for very short channel lengths, it can be used to study relative changes in I_{ON} for the purpose of design optimization.

DD simulations are also used to predict the subthreshold and off-state characteristics of the Si and Ge devices using default Si parameters and the Ge parameter set in Table 6.1. Since electrostatic integrity, rather than carrier mobility, plays a larger role in determining subthreshold behavior, the approximate mobility parameters used in the DD simulations should not result in significant errors in the subthreshold regime. Quantization effects in the transverse direction are captured in the DD simulations with a 1-D Schrödinger model, which accounts for the change in threshold voltage (V_T) and gate capacitance due to channel inversion charge redistribution and energy sub-band splitting. The inversion-layer hole concentration calculated by this 1-D Schrödinger model agrees well with more rigorous 6×6 $k \cdot p$ Poisson-Schrödinger calculations described in the following DSDT section. Ideal threshold voltage tuning through gate work-function engineering is assumed to set I_{OFF} = 100 nA/um for V_{GS} = 0 V and V_{DS} = V_{DD}. In this study, the supply voltage V_{dd} = 0.6 V. Gate leakage and oxide interface states are not included because these effects strongly depend on specific materials and processing conditions; their

TABLE 6.1
MATERIAL PARAMETERS FOR DRIFT-DIFFUSION SIMULATIONS

Parameter	UNITS	Material	
		Si	**Ge**
$\mu_{electron}$	$cm^2 V^{-1} s^{-1}$	1400	3900
μ_{hole}	$cm^2 V^{-1} s^{-1}$	470	1900
E_g	eV	1.12	0.66
ε_r	–	11.7	16.2
N_c	cm^{-3}	3.2×10^{19}	1.0×10^{19}
N_v	cm^{-3}	1.8×10^{19}	5.0×10^{18}

exclusion from this study will result in more ideal device performance metrics for both Si and Ge. Band-to-band tunneling (BTBT) is also not accounted for in these simulations because of the complex interaction between conduction and valence bands. (DSDT, on the other hand, is only an intra-band tunneling mechanism.) Although BTBT is more severe for Ge than Si pMOSFETs due to the smaller bandgap [13] and it occurs in the same off-state regime as DSDT, BTBT can be suppressed by using a thin body to effectively increase the bandgap (quantum confinement effect) [14] and by adjusting the doping profile or the applied voltage to reduce the electric field at the drain junction. Current BTBT models in *Sentaurus* cannot capture the dependence of BTBT on quantum confinement effects, but as will be discussed later, the optimized device has a thin body (4 nm) and an undoped channel that should help suppress BTBT. Even with changes in device geometry to suppress BTBT, it would still negatively impact Ge MOSFETs more so than Si MOSFETs, and the exclusion of BTBT from this study results in a best-case comparison for Ge.

The MC capability within the *Sentaurus* TCAD suite [15] is used to simulate the on-state characteristics of Ge and Si devices. MC solves the Boltzmann transport equation using statistical methods and is useful for highly-scaled device dimensions since it can physically capture non-stationary transport effects, such as velocity overshoot and ballistic transport. The hole energy band structure in the semi-classical MC simulator is modeled by a 6×6 $k \cdot p$ calculation [16]. Since uniaxial stressors are routinely applied to modern HP devices and different channel orientations are being investigated for better device performance, these effects are also captured physically in the simulator by performing the $k \cdot p$ calculation for specific crystal directions and uniaxial strain conditions. The resulting dispersion relations are then used for transport simulations [15]. The Luttinger-Kohn parameters and deformation potentials used for Si and Ge were fitted to full-band empirical pseudopotential (EPM) calculations and are given in Table 6.2. Acoustic and optical phonon scatterings are included, with their deformation potentials adjusted to match Si and Ge low-field bulk hole mobilities with $k \cdot p$ simulations. To verify these parameters, the Ge band structure calculated from both $k \cdot p$ and EPM methods as well as steady-state hole drift velocities as a function of electric field for bulk Si and Ge are shown in Fig. 6.1. Surface roughness scattering parameters are the same for Si and Ge channels

TABLE 6.2
PARAMETERS FOR MONTE CARLO SIMULATIONS

Parameter	UNITS	Material	
		Si	**Ge**
γ_1	–	4.306	9.136
γ_2	–	0.354	2.654
γ_3	–	1.44	3.740
Δ_{SO}	eV	0.043	0.297
a_v	eV	2.46	2.1
b	eV	-2.316	-2.07
d	eV	-4.78	-6.06

6×6 $k \cdot p$ parameters and deformation potentials for Monte Carlo simulations. The shear deformation potential d for Ge is taken from [17].

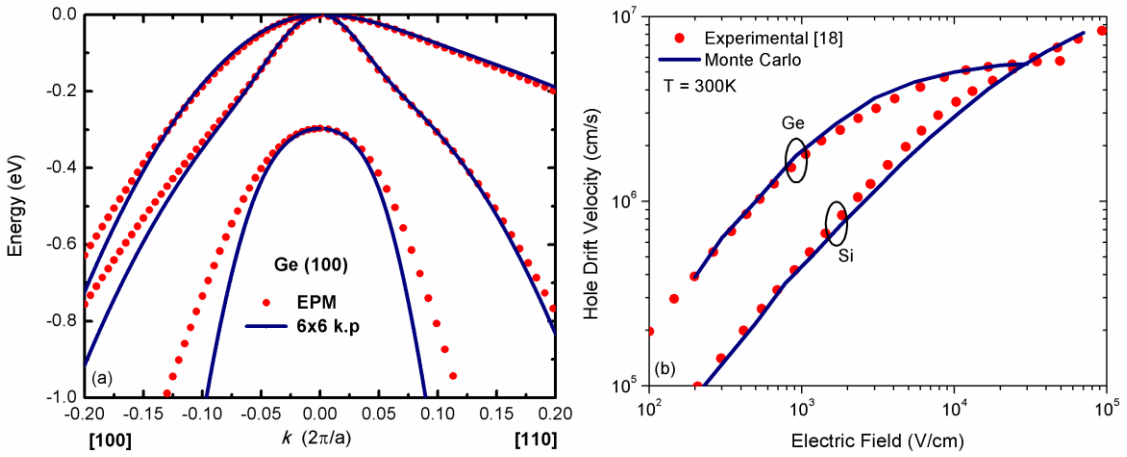

Fig. 6.1: (a) Ge (100) band structure calculated using the 6×6 k•p method and fitted to EPM. Band parameters are listed in Table 6.2. Acoustic and optical phonon scattering parameters were obtained by using Monte Carlo k•p simulation to match the (b) steady-state hole drift velocities for bulk Si and Ge with experimental values [18].

and are unchanged from the default parameters in *Sentaurus* (correlation length L_c = 2.2 nm, RMS roughness Δ_{RMS} = 0.18 nm). As in the DD simulations, gate leakage, interface states, and BTBT are not taken into account in the MC simulations.

6.2.2 Device Structure and Design Optimization

The 2009 ITRS projects physical gate lengths down to 7.5 nm at the end of the roadmap for HP devices. For this study, L_G = 8 nm was used, with a total contact-to-contact spacing of 16 nm. A double-gate (DG) MOSFET structure is used because it is highly scalable [19-20]. The geometrical design parameters that were optimized are illustrated in Fig. 6.2.

For 8 nm gate length and 16 nm contact-to-contact spacing, the gate-sidewall nitride spacer length (L_{SP}) cannot exceed 4 nm. Because L_G is so short, the maximum allowable L_{SP} (4 nm) provides for the best gate control over the channel potential. The gate oxide material is assumed to be silicon dioxide with thickness T_{OX} = 1 nm. The source/drain (S/D) doping profile is Gaussian with a peak concentration of 10^{20} cm^{-3}. L_{SD} is defined to be the distance from the peak position of the doping profile (at the contact-channel interface) to the location where the dopant concentration drops to 10^{19} cm^{-3}. The effective channel length (L_{eff}) is defined to be the distance between the locations where the source and drain doping concentrations equal 10^{19} cm^{-3}. The channel region is lightly doped p-type (10^{15} cm^{-3}). The optimal L_{SD} for L_G = 8 nm is that which results in the largest L_{eff}, because higher I_{ON}/I_{OFF} is achieved by reducing short-channel effects *vs.* lowering parasitic resistance. Thus, L_{SD} is set to be 2 nm, assuming it to be the practical lower limit. As will be discussed in the next section, the abrupt S/D doping also helps to minimize DSDT. Finally, the channel thickness T_{CH} is optimized to yield the highest I_{ON}/I_{OFF} ratio for drain induced barrier lowering (DIBL) below 100 mV/V. The optimal value of T_{CH} is 4 nm for both the Si and Ge DG MOSFETs, although the DIBL for the Si device is 58 mV/V whereas it is

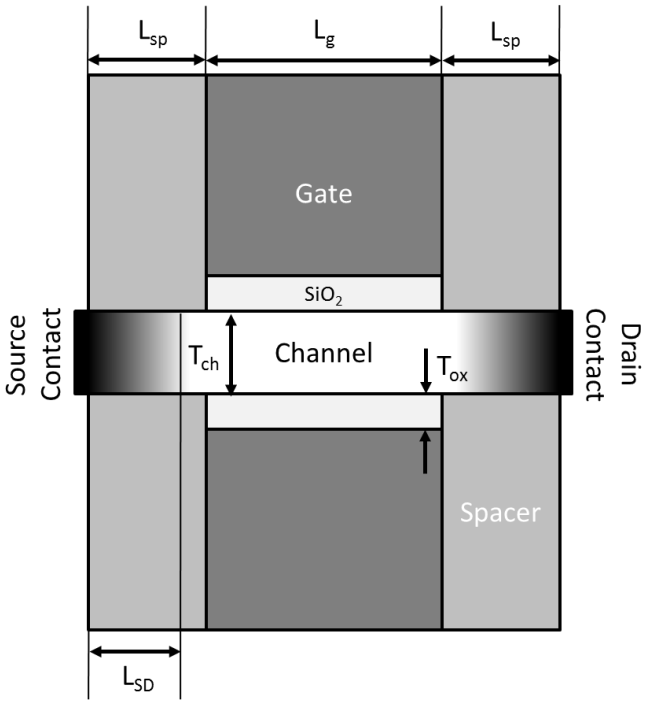

Fig. 6.2: Cross-section of the double-gate MOSFET structure used in this study. Optimized design parameters are: L_G = 8 nm, T_{CH} = 4 nm, T_{OX} =1 nm, L_{SP} = 4 nm, L_{SD} = 2 nm. The specific contact resistivity for source and drain contacts is 10^{-8} Ω-cm^2.

90 mV/V for the Ge device. A thinner T_{CH} will help further suppress SCE in Ge, but it also increases parasitic series resistance. Although not included in the simulations, mobility degradation due to increased phonon scattering occurs in ultra-thin channels [21-22]. Increased series resistance and reduced mobility for channels thinner than 4 nm would result in reduced drive current.

6.2.3 Direct Source-to-Drain Tunneling Current

DSDT contributes an additional component of current in the subthreshold regime, which effectively degrades the subthreshold swing (*S*). (When the MOSFET is biased in the on state, the source potential barrier is low so that DSDT is negligible compared to drift current.) For this study, DSDT is modeled using a non-local 1-D Schrödinger solution to compute the tunneling probability through the source potential barrier. Currently *Sentaurus* can only compute tunneling rates with a single sub-band approximation, using an effective tunneling hole mass in the Schrödinger equation. The effective tunneling hole mass used in this model should be the same as the hole transport mass in the longitudinal direction (along the channel). A 6×6 *k•p* Poisson-Schrödinger calculation of the valence band structure for the optimized DG MOSFET design was used to calculate the longitudinal effective hole mass of the top-most valence sub-band. Because the valence band is highly anisotropic, especially in the presence of strain, a curvature effective mass near the Gamma point does not give a meaningful value of the average effective

mass in the sub-band. Instead, an occupancy-weighted effective mass m_{xx} is calculated, as described by

$$\frac{1}{m_{xx}} = \frac{\sum_i \frac{1}{(2\pi)^2} \int d^2k \frac{1}{\hbar^2} \frac{\partial^2 E_i}{\partial k^2} [1 - f(E_i)]}{P_{inv}}. \qquad (1)$$

This definition of effective mass integrates the inverse curvature hole mass over all of *k*-space weighted by the probability of occupancy calculated from the Fermi-Dirac distribution $f(E_i)$, and is summed over all subbands *i*. This quantity is normalized to the total hole inversion population P_{inv} and gives a more reasonable estimate of the hole transport effective mass for anisotropic dispersions. The effect of uniaxial compressive strain on the effective transport mass was also investigated. Luttinger-Kohn parameters and deformation potentials for Si and Ge are the same as those used in the MC simulations previously described. These effective transport masses m_{xx} for Si and Ge are shown in Fig. 6.3 for different channel orientations and varying uniaxial compressive stress values. Generally, the Si hole masses are heavier than the Ge masses for a given orientation. For both Si and Ge, the hole transport mass in the conventional <110>/{100} channel orientation is very sensitive to uniaxial compressive stress. At 1.5 GPa uniaxial compressive stress, the <110>/{100} Si and Ge hole masses decrease to 33% and 38% of their unstrained values, respectively. Although decreased transport mass is beneficial for enhanced hole transport in the on-state, it also results in increased DSDT in the off-state. Thus, device performance will be impacted more significantly by DSDT at higher levels of stress.

To check the validity of the single-sub-band assumption of the DSDT model, the same 6×6 *k•p* Poisson-Schrödinger calculations used for extracting the tunneling mass were also used to evaluate the sub-band occupation of carriers in Si and Ge by matching the inversion-layer hole concentrations with the quantized DD simulation in the off-state (inversion hole concentration ≈

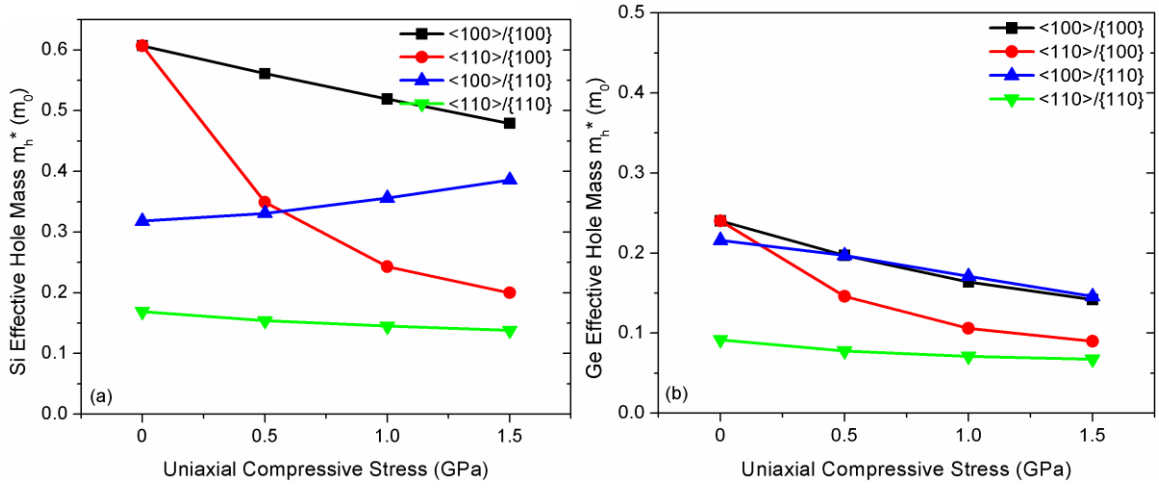

Fig. 6.3: Effective hole transport masses m_{xx} for (a) Si, and (b) Ge.

10^9 cm^{-3}). The percentage of holes in the top three valence sub-bands was subsequently extracted from the *k•p* calculation. Significant quantization due to the very thin body produces subband splitting, resulting in hole redistribution mainly to the top-most valence subband, even for very low gate bias. In Si and Ge, ~75% and ~99% of the holes are contained in the top-most sub-band, respectively, which indicates that the single-sub-band approximation used to calculate DSDT is reasonable.

To determine the impact of DSDT, conventional DD simulations are performed with and without the DSDT tunneling model turned on. (Again, the DD model should be reasonable for subthreshold current simulation because mobility does not play as large a role in this regime of operation.) With DSDT turned on, S is degraded so that the gate voltage corresponding to I_{OFF}, which is defined to be the off voltage (V_{OFF}), is shifted. I_{ON} is then taken from MC simulations at $|V_{GS}| = |V_{OFF} - V_{DD}|$. In this manner, the impact of DSDT on I_{ON} can be assessed.

6.3 Results and Discussion

The effect of DSDT on S as a function of L_{SD} is shown in Fig. 6.4 for Ge and Si pMOSFETs with unstrained <110>/{100} channels. S is extracted from simulations by taking the average derivative of the interpolated $\log(I_{DS})$-V_{GS} curve at I_{OFF}. For the Si device, DSDT degrades S for $L_{SD} > 4$ nm. Thus, abrupt S/D doping profiles are even more important for achieving good electrostatic integrity in the presence of DSDT. For the Ge device, DSDT degrades S even for $L_{SD} = 2$ nm, and S increases more rapidly with increasing L_{SD}. As shown in Fig. 6.5, the effect of DSDT is diminished by increasing L_G (keeping all other design parameters the same) – but this comes at the cost of reduced layout efficiency. For both unstrained and strained channels, the Si MOSFET shows no S degradation due to DSDT if $L_{SD} = 2$ nm. The unstrained Ge MOSFET shows a little degradation in S due to DSDT, while the strained Ge MOSFET shows increased sensitivity to DSDT for $L_G < 12$ nm. This is due to worse short channel control (larger DIBL) and lower hole transport effective mass in the Ge device.

Figs. 6.6a and 6.6b plot I_{ON} (normalized to channel width, per gate) for <110>/{100} and <110>/{110} channel orientations, respectively, as a function of L_G for various levels of uniaxial compressive stress. The impact of DSDT is not taken into account for these curves. (Results for <100> channel orientation are not shown because they show lower I_{ON} and thus are not attractive for high-performance applications.) The Si MOSFET drive currents do not change very much as L_G is reduced from 20 nm to 8 nm, peaking at $L_G \approx 14$ nm. The Ge MOSFET drive currents, on the other hand, decrease monotonically as L_G is reduced, due to more severe short-channel effects. It is worthwhile to note that stress has more significant beneficial impact for the Si MOSFETs than for the Ge MOSFETs. As a result, for the conventional <110>/{100} channel orientation with 1.5 GPa uniaxial compressive stress, Ge outperforms Si only for $L_G > 15$ nm. Maximum Si and Ge device drive currents are increased by 10% and 5%, respectively, by using a (110) substrate rather than a (100) substrate. For <110>/{110} channel orientation with 1.5 GPa uniaxial compressive stress, Ge outperforms Si only for $L_G > 17$ nm.

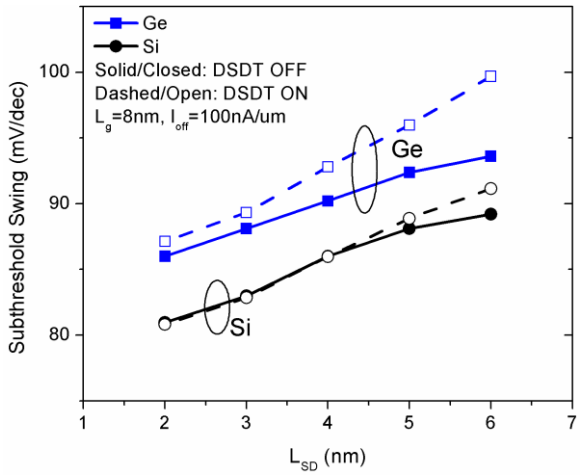

Fig. 6.4: S as a function of L_{SD}, with and without DSDT, for MOSFETs with <110>/{100} channel orientation.

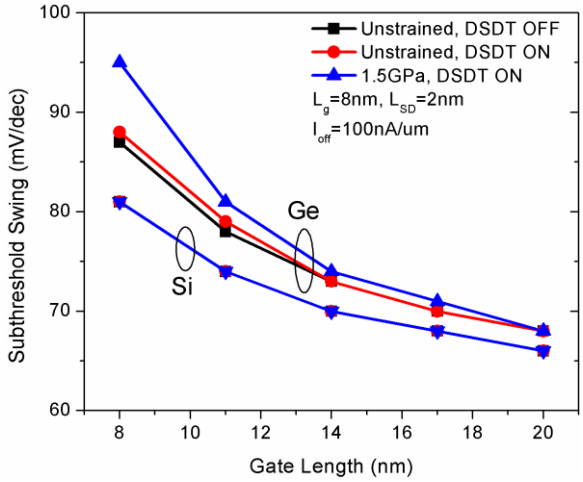

Fig. 6.5: S as a function of gate length, with and without DSDT, for MOSFETs with <110>/{100} channel orientation.

Effective current (I_{eff}) has been shown to be a better metric for circuit performance than I_{ON} [23]. In this study, effective current is calculated using

$$I_{eff} = \frac{I_d\left(V_{gs} = V_{dd}, V_{ds} = \frac{V_{dd}}{2}\right) + I_d\left(V_{gs} = \frac{V_{dd}}{2}, V_{ds} = V_{dd}\right)}{2}. \quad (2)$$

Figs. 6.7a and 6.7b plot I_{eff} (calculated from MC simulation results) for <110>/{100} and <110>/{110} channel orientations, respectively, as a function of L_G for various levels of uniaxial compressive stress. For either channel orientation, the strained Ge MOSFET never outperforms

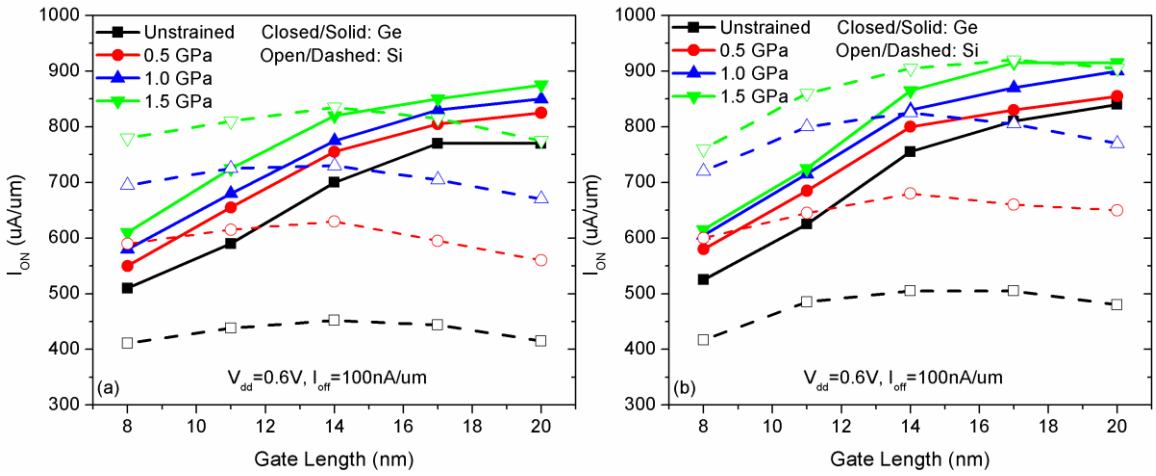

Fig. 6.6: On-state drive current for Si and Ge MOSFETs as a function of gate length for (a) <110>/{100} and (b) <110>/{110} channel orientations, for various levels of channel stress.

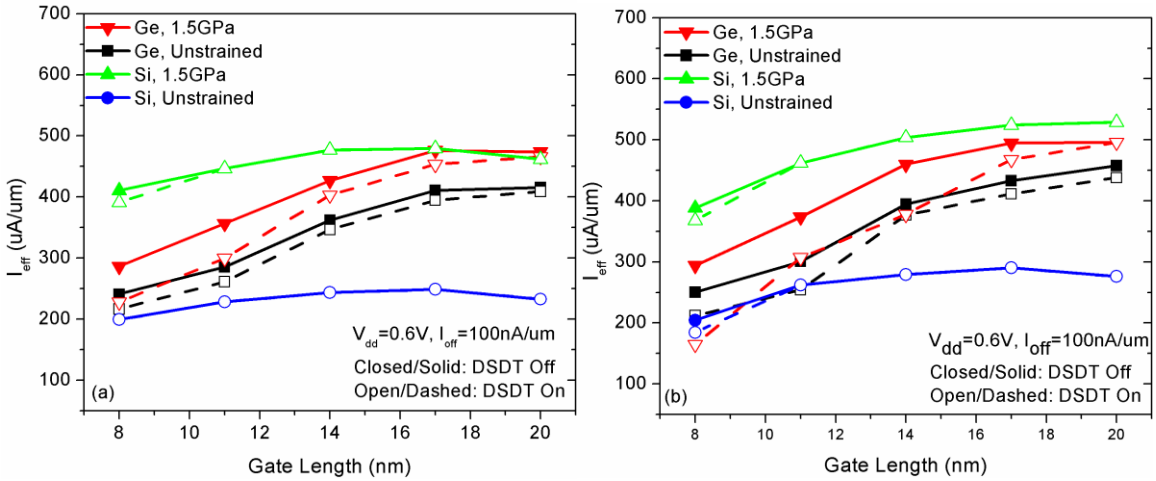

Fig. 6.7: Effective drive current for Si and Ge MOSFETs as a function of gate length for (a) <110>/{100} and (b) <110>/{110} channel orientations, for various levels of channel stress.

the strained Si MOSFET for L_G < 20 nm. This is due to the larger DIBL for Ge MOSFETs. The impact of DSDT is indicated by the dashed curves, and is negligible for Si MOSFETs. DSDT has minimal effect on Ge MOSFET I_{eff} at L_G = 20 nm; however, as L_G is reduced, the Ge MOSFET is affected more by DSDT due to the lighter hole transport mass. Compressive strain further reduces the mass, which results in more DSDT-induced degradation for the strained Ge MOSFET. The strained <110>/{110} hole transport mass is so light that the strained Ge device has worse performance at L_G = 8 nm than the unstrained Ge device.

To elucidate the cause of the poorer performance for Ge compared to Si, the <110>/{100} hole velocity and inversion concentration were extracted at the virtual source (top of the hole potential barrier) [24] and are plotted in Fig. 6.8. For both Si and Ge devices, the hole velocity

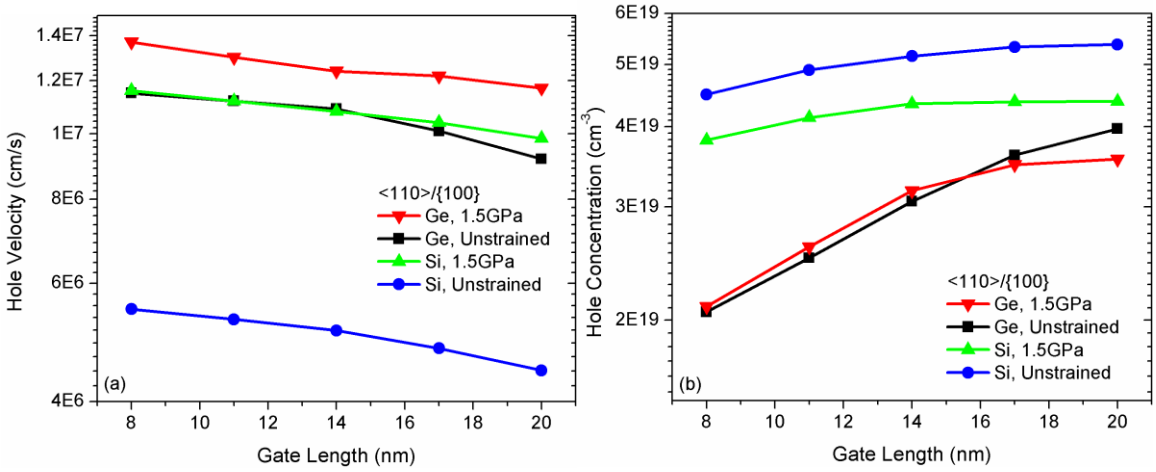

Fig. 6.8: Inversion-layer (a) hole velocity and (b) hole concentration at the virtual source as a function of gate length, for various levels of channel stress.

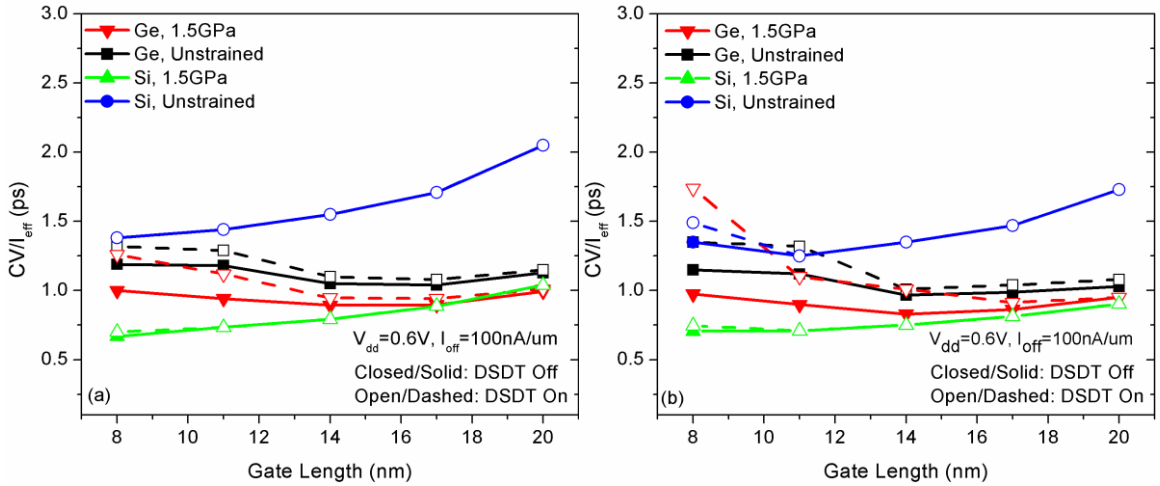

Fig. 6.9: Intrinsic delay as a function of gate length, for (a) <110>/{100} and (b) <110>/{110} channel orientations with and without DSDT.

increases as L_G is reduced, but it is always higher for Ge than for Si. (It is interesting to note that the Si hole velocity increases greatly with strain, so that it is almost as high as the unstrained Ge hole velocity, for 1.5 GPa uniaxial compressive stress). On the other hand, the inversion-layer hole concentration at the virtual source is lower for Ge than for Si, and it decreases more rapidly with decreasing L_G for Ge. This is due to poorer gate control which results in larger V_T and reduced drive current for the Ge MOSFETs.

The total gate capacitance (C_{total}) for the Si and Ge devices was extracted from simulated *C-V* curves at V_{DD} and used to compute the intrinsic delay $\tau = C_{total}V_{DD}/I_{eff}$ plotted in Fig. 6.9. The capacitance values for the Si and Ge devices are similar (< 5% difference); thus Ge devices suffer from higher delay due to lower I_{eff}. The lowest delay of 0.67 ps is achieved by the strained

Si device at L_G = 8 nm for a <110>/{100} channel orientation and 1.5 GPa uniaxial compressive stress; with DSDT, this increases negligibly to 0.7 ps. The lowest delay for a Ge device is 0.83ps at L_G = 14 nm for a <110>/{110} channel orientation and 1.5 GPa uniaxial compressive stress; with DSDT, this increases to 1.0 ps. The lowest delay achievable with Ge accounting for DSDT is 0.91 ps at L_G = 17 nm. Gate length scaling beyond this results in higher intrinsic delay for a Ge MOSFET.

6.4 Summary

Through a combination of drift-diffusion and Monte Carlo simulations, it is shown that an optimized Ge pMOSFET cannot outperform an optimized Si pMOSFET at gate lengths below 15 nm. This is due to the inferior electrostatic integrity of the Ge MOSFET, which makes it much more susceptible to direct source-to-drain tunneling (DSDT). The lower effective hole transport mass of Ge amplifies this issue, as does uniaxial compressive channel stress. It should be noted that gate-length scaling has slowed in recent technology nodes [25-27] so that L_G = 8 nm considered in this study may be too aggressive. Also, a relatively high level of channel stress (1.5 GPa) was assumed to be achievable, and may be difficult to achieve in practice as the device pitch (specifically, the lengths of the source and drain regions) continues to scale down [28]. For lower levels of stress, a Ge pMOSFET can outperform a Si pMOSFET for L_G < 15 nm. For instance, if the uniaxial compressive channel stress is only 0.5 GPa, Ge can outperform Si down to $L_G \approx$ 10 nm for the conventional device orientation. If L_G scaling slows dramatically and the level of channel strain decreases with device pitch scaling, then Ge still can be a promising alternative to Si for high-performance pMOSFET technology.

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Chapter 7

Conclusion

7.1 Summary

The semiconductor industry has made great innovations to maintain the pace of CMOS transistor scaling. However, as transistor gate lengths shrink and the distance between the source and drain regions is reduced, short channel effects (SCE) become harder to control. This results in higher off-state leakage and lower effective drive current. To resolve this problem, the industry is already developing thin-body transistor structures, most notably the FinFET and FDSOI MOSFET structure. One manufacturer is already implementing FinFETs in volume manufacturing, with other major IC manufacturers expected to achieve volume production of FinFETs or FDSOI MOSFETs in 2013-2014. The FinFET and FDSOI MOSFET have excellent control over SCE, but have increased cost, which manifests itself in the starting substrate or in more challenging fabrication.

The SegFET was introduced as a more manufacturable, lower-cost alternative to the FinFET and FDSOI MOSFET structures that improves SCE as compared to the planar bulk MOSFET. The first experimental demonstration of the SegFET down to L_{eff} = 45nm indeed showed that SCE can be better suppressed than in a planar bulk MOSFET control device fabricated with the same process flow. In addition, mobility is enhanced and V_{T} is reduced in the SegFET, resulting in comparable layout area efficiency to the planar bulk MOSFET, despite halving the effective Si channel area. Thus, the SegFET is more scalable than the planar bulk MOSFET and is ideal for IC applications where cost, rather than performance, is more critical.

Although the SegFET is emphasized as a lower-cost alternative to thin-body MOSFETs, this does not preclude the SegFET from also achieving similar performance as these revolutionary transistor structures. By carefully optimizing the SegFET structure (*i.e.* adjusting the Si stripe height and retrograde channel doping profile), TCAD simulations show that it can provide similar drive current, intrinsic device delay, and short-channel control compared to a bulk FinFET with the same effective width, while relaxing the Si stripe aspect-ratio and retrograde channel doping abruptness to improve manufacturability. In addition, the V_{T} variation due to

RDF and gate LER is comparable between the SegFET and FinFET. Although the FinFET can achieve higher layout efficiency by making the height of the fin taller, this comes with increased process complexity.

Since the 90nm technology node, MOSFETs have relied on strain engineering to enhance mobility. Today, most high-performance MOSFETs rely on drive current enhancement from strain techniques such as CESL-induced strain, strain memorization technique, and embedded source/drain stressors. As transistors continue to scale and as these strain techniques reach their physical limit, new channel materials with higher intrinsic mobility may be needed. The materials that can be integrated most straightforwardly in modern CMOS processing are Ge and $Si_{1-x}Ge_x$ alloys. TCAD simulations were used to explore the design space of $Si_{1-x}Ge_x$/Si heterostructure channel pMOSFETs and it was shown that higher Ge concentration channels provide more drive current. However, at high Ge concentrations, performance is more sensitive to $Si_{1-x}Ge_x$ channel thickness, possibly resulting in unacceptable process-induced variations. Thus, the optimal $Si_{1-x}Ge_x$ heterostructure channel should be thin (< 2nm) and have a moderate Ge concentration (~ 20%-40%).

Using the information gained from TCAD, thin (2-5 nm) $Si_{0.5}Ge_{0.5}$/Si heterostructure channels were implemented in experimental SegFET and planar (*i.e.* un-corrugated) pMOSFETs. The results showed that $Si_{1-x}Ge_x$ channels on the SegFET structure exhibit better mobility and suppression of SCE, resulting in 30% improvement in I_{ON} per unit layout width for I_{OFF} = 10nA/um compared to planar $Si_{1-x}Ge_x$ channel control devices. The SegFET structure also drastically reduces the layout-width dependencies of V_T and $I_{D,LIN}$ (that arise from $Si_{1-x}Ge_x$ channel strain relaxation) compared to the planar MOSFET structure. This enables the use of thicker $Si_{1-x}Ge_x$ channels (5nm-thick $Si_{1-x}Ge_x$ channel SegFETs show 10% improvement in I_{ON} compared to 2nm-thick channel SegFETs) as well as higher Ge concentration to further boost mobility and performance.

Finally, using TCAD and Monte Carlo simulations, pure Ge p-channel FinFETs were compared to strained Si FinFETs for device geometries near the end of the roadmap (L_G = 8nm). Although the low hole transport mass of Ge (which is reduced further with application of strain) can achieve higher on-state drive current, it also results in more direct source-to-drain tunneling, leading to more off-state leakage and degraded subthreshold swing. Thus, for the same I_{OFF} specification and V_{DD}, strained Ge FinFETs have lower drive current than strained Si FinFETs for L_G < 14 nm (due to smaller gate overdrive). Looking at effective current, Ge FinFETs fare even worse compared to its Si counterpart because of the higher dielectric constant and worse SCE. However, if Si cannot be strained to the level assumed in this study (1.5 GPa) or gate lengths cannot be scaled so aggressively, then Ge may be a promising alternative to Si for providing better transistor performance.

7.2 Suggestions for Future Work

The work described in the preceding chapters has been exploratory in nature and implementing these ideas in industry will require more in-depth investigation. The SegFET

devices presented in Chapters 2 and 5 demonstrated benefits over planar bulk MOSFETs, but to validate the suitability of replacing planar bulk with SegFETs in advanced technology nodes, these benefits must be confirmed with the use of more state-of-the-art technology such as high-*k*/metal gate and strain techniques. Analog performance of SegFETs is another area of exploration, since it is likely easier to integrate SegFETs in a system-on-chip IC than FinFETs. Further experimental work is also needed to validate TCAD simulations and demonstrate the true scalability and performance of the SegFET structure for L_G < 30 nm against its planar bulk and FinFET counterparts. To help guide this future SegFET work, TCAD was used to create a roadmap (modeled on the 2011 ITRS roadmap) for the SegFET structure described in Chapter 3. Whereas planar bulk MOSFETs and FinFETs rely on channel doping profile engineering and Si stripe width, respectively, to suppress SCE, SegFETs use both, and this difference is reflected in the roadmap below for high performance logic (HP), low-operating power (LOP), and low-standby power (LSTP) technology requirements.

Examining this roadmap, it is assumed that the SegFET stripe width is easy to manufacture since the Si stripe width is greater than or equal to L_G, whereas manufacturable solutions for sub-L_G FinFET widths are not known beyond 2020. The junction depth (or, equivalently, the depth of the retrograde channel doping) may pose difficulties for SegFETs beyond 2023. Novel epitaxy techniques need to be developed and optimized to achieve ultra-steep retrograde profiles and/or ultra-shallow junctions. Note, however, that it is generally easier to control the deposition of thin films rather than the etching of narrow lithographically-defined features.

Roadmap for Planar MOSFET, SegFET, and FinFET (Adapted from 2011 ITRS Roadmap)					
	Manufacturable solutions exist		Manufacturable solutions are known		Manufacturable solutions are NOT known

High Performance (HP) Logic Technology Requirements													
Year	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
Physical L_G (nm)	18	17	15.3	14	12.8	11.7	10.6	9.7	8.9	8.1	7.4	6.6	5.9
V_{DD} (V)	0.82	0.8	0.77	0.75	0.73	0.71	0.68	0.66	0.64	0.62	0.61	0.59	0.57
Equivalent Oxide Thickness (nm)													
Planar	0.73	**0.67**	**0.61**	**0.55**									
SegFET	0.86	0.8	0.76	0.72	0.68	**0.65**	**0.62**	**0.59**	**0.56**	**0.53**	**0.5**	**0.47**	**0.45**
FinFET		0.8	0.76	0.72	0.68	**0.65**	**0.62**	**0.59**	**0.56**	**0.53**	**0.5**	**0.47**	**0.45**
Stripe width (nm)													
SegFET	18	17	15.3	14	12.8	11.7	10.6	9.7	8.9	8.1	7.4	6.6	5.9
FinFET		11.3	10.3	9.4	8.5	7.7	**7**	**6.3**	**5.7**	**5.2**	**4.7**	**4.2**	**3.7**
Junction Depth (nm)													
Planar	7.2	**6.4**	**5.7**	**5**									
SegFET	12.6	11.9	10.7	9.8	9.3	8.8	8.2	7.76	7.1	**6.5**	**5.9**	**5.3**	**4.7**

Low Operating Power (LOP) Technology Requirements													
Year	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
Physical L_G (nm)	19	18	16	14.5	13.1	11.9	10.8	9.8	8.9	8.1	7.3	6.5	5.8
V_{DD} (V)	0.65	0.63	0.61	0.59	0.57	0.55	0.53	0.51	0.49	0.48	0.46	0.44	0.43
Equivalent Oxide Thickness (nm)													
Planar	0.75	0.7											
SegFET	0.95	0.9	0.86	0.82	0.78	0.74	0.7	**0.66**	**0.63**	**0.6**	**0.58**	**0.54**	**0.5**
FinFET		0.9	0.86	0.82	0.78	0.74	0.7	**0.66**	**0.63**	**0.6**	**0.58**	**0.54**	**0.5**
Stripe width (nm)													
SegFET	19	18	16	14.5	13.1	11.9	10.8	9.8	8.9	8.1	7.3	6.5	5.8
FinFET		11.8	10.7	9.7	8.7	7.8	**7.1**	**6.4**	**5.7**	**5.2**	**4.6**	**4.1**	**3.6**
Junction Depth (nm)													
Planar	**6.5**	**5.4**											
SegFET	13.3	12.6	11.2	10.5	9.8	9.2	8.6	7.8	7.1	**6.5**	**5.8**	**5.2**	**4.6**

Low Standby Power Power (LSTP) Technology Requirements													
Year	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
Physical L_G (nm)	22	20	17.5	15.7	14.1	12.7	11.4	10.2	9.2	8.2	7.4	6.6	5.9
V_{DD} (V)	0.84	0.81	0.78	0.75	0.72	0.7	0.67	0.65	0.63	0.61	0.59	0.56	0.54
Equivalent Oxide Thickness (nm)													
Planar	0.9	0.8											
SegFET	1.3	1.2	1.1	1.0	0.95	0.9	0.85	0.8	0.75	0.71	0.68	**0.64**	**0.6**
FinFET		1.2	1.1	1.0	0.95	0.9	0.85	0.8	0.75	0.71	0.68	**0.64**	**0.6**
Stripe width (nm)													
SegFET	22	20	17.5	15.7	14.1	12.7	11.4	10.2	9.2	8.2	7.4	6.6	5.9
FinFET		12.5	11.2	10.1	9	8.1	**7.2**	**6.4**	**5.7**	**5**	**4.5**	**4**	**3.5**
Junction Depth (nm)													
Planar	**6**	**5**											
SegFET	15.4	14	12.3	11.4	10.5	9.8	9.1	8.2	7.4	**6.6**	**5.9**	**5.3**	**4.7**

Other interesting projects involving corrugated substrates and SegFETs include integration of other high-mobility materials such as pure Ge and GaAs using the aspect-ratio trapping method (ref. Chapter 2), with the aim of integrating optoelectronic devices (photodiode/receiver and light source/transmitter with Ge and GaAs, respectively) directly on the same chip as Si CMOS logic. In addition, since narrow Si stripes bordered by SiO_2 acts as a waveguide material for the infrared wavelengths used in fiber optic telecommunication, integrated photonic chips may be more feasible using corrugated substrates.

In regard to $Si_{1-x}Ge_x$ channels, experiments need to be performed to validate TCAD simulations of the $Si_{1-x}Ge_x$/Si heterostructure-channel pMOSFETs discussed in Chapter 4. To accomplish this, a high-*k* material with no Si capping layer should be used for the gate oxide to reduce the EOT. In addition, to maintain the integrity of the $Si_{1-x}Ge_x$ channel, new techniques

must be investigated to limit the Ge out-diffusion from the $Si_{1-x}Ge_x$ channel (especially for Ge concentrations > 50%). These techniques can also be applied to $Si_{1-x}Ge_x$/Si channel SegFETs to ascertain the highest Ge concentration that can be practically incorporated within the $Si_{1-x}Ge_x$ channel. For the TCAD simulations of the pure Ge double-gate pMOSFETs, it would be useful to conduct experiments to determine the true performance of Ge and Si FinFETs. Again, this will necessitate work on improving the gate oxide interface on Ge. Thick Ge films on Si (for tall stripe heights) also pose a process integration problem due to strain relaxation and defects at the Si/Ge interface, which must be minimized to achieve good device performance.

7.3 The Silicon Road(s) into the Unknown

For the first time in 40 years, the semiconductor industry is at an enormous crossroads. Although the FinFET is the leading alternative transistor structure being developed by major manufacturing companies and provides better performance than the conventional planar bulk MOSFET, the extra development cost, more restrictive circuit design rules, and more difficult manufacturability may not make it cost-beneficial for the majority of IC applications such as those used in low-power and low-cost mobile devices. High-mobility channel materials are still an active area of research, yet it is still unclear when this technology will be implemented in mainstream products.

As discussed in Chapter 1, the electronics industry is witnessing a movement toward the "internet of things" where electronic devices will pervade consumers' lives, as is already seen in the proliferation of mobile communication devices. These inexpensive embedded ICs and sensors may not need the high performance that the FinFET and FDSOI MOSFET provide, nor the higher process development or substrate costs that are associated with these transistor structures. However, scaling transistor dimensions still benefit these lower-cost chips by reducing die size and cost-per-wafer.

In the future, the semiconductor industry may diverge into two segments. One segment may focus on specialty applications using thin-body structures like the FinFET and high-mobility channel materials for server and datacenter applications where chip costs are of less concern. Another segment may pursue more manufacturable transistor designs like the SegFET for mobile devices and sensors, for which low cost (rather than performance) is a major determining factor in product success.

Regardless of how the landscape of the semiconductor industry will look like in five or ten years, traditional transistor scaling is coming to an end as the planar bulk MOSFET pushes against the limits of process technology. It will take new innovations and breakthroughs in materials and process integration, as well as close collaboration with circuit, system, and software designers to create faster, cheaper, and more functional electronics. Although the electronics industry certainly faces a future full of unknowns, these unknowns also provide new opportunities for human ingenuity to continue pushing the capabilities of computing, technology, and humankind.

Appendix A

Si n-channel SegFET Process Flow

TEL SegFET NMOS PROCESS FLOW TEL = t4, t6, t7, t8, t9, t10 CON = s3, s4						
Step #	Process	Wafers	Tool Name	Description	Notes	Date Done
0.1	Strip PR Preclean	 TEL	sink432c msink8	PRS-3000, 80C, 10mins/DI rinse Pirahna, 10mins 120C / BHF, 10sec		
1	Clear die for PM marks					
1.01	Coat PR	TEL, CON d1.1	svgcoat6	1, 2, 1		3/9/2011
1.02	Expose PR	TEL, CON d1.1	asml300	Kim's Clear exposure test mask Apply coarse wafer rotation	t4: 0.802 / t6: 0.266 / t7: 1.154 t8: 1.131 / t9: 1.179 / t10: 1.068	3/9/2011
1.03	Develop PR	TEL, CON d1.1	svgdev6	1, 1, 9		3/9/2011
1.04	Hardbake	TEL, CON d1.1	uvbake	Process U		3/9/2011
1.05	Si ER Test	d1.1	lam8	8003 OB/ME (3s/10s) asiq	Si ER ~5.5 nm/min	3/10/2011
1.06	Si Etch	TEL, CON	lam8	8003 OB/ME nanoduv	TEL: 31 sec CON: 32 sec	3/10/2011
1.08	Oxide ER Test	ox1.1	centura-mxp	MXP-OXIDE-ETCH	Ox ER: 70 A/sec	3/10/2011
1.09	Oxide etch	TEL, CON	centura-mxp	MXP-OXIDE-ETCH	TEL: 17 sec CON: 26 sec	3/10/2011
2	PM Marks					
2.01	Strip PR,	TEL, CON	matrix	2.5mins, 400W, 200C		3/14/2011

	Preclean d2.1		msink8	Pirahna, 10mins 120C 5:1 HF, 30sec	(remove residual BOX)	
2.02	Coat PR	TEL, CON d2.1	svgcoat6	1, 2, 1		3/14/2011
2.03	Expose PR	TEL, CON d2.1	asml	combi reticle Apply same wafer rotation	t1: 0.83 / t2: 1.09 / t3: 0.23 t4: 0.82 / t5: 1.16 / t6:	3/14/2011
2.04	Develop PR	TEL, CON d2.1	svgdev6	1, 1, 9		3/14/2011
2.05	Hardbake	TEL, CON d2.1	uvbake	Process U		3/14/2011
2.06	Si ER Test	d1.1	lam8	8003 OB/ME (3s/10s) asiq	Si ER ~4.0 nm/min	3/14/2011
2.07	Test Dummy in ASML	d2.1	asml	Test to see if PM can be registered	WORKS!	3/14/2011
2.08	Si Etch	TEL, CON	lam8	8003 OB/ME	Time: 30 sec	3/14/2011
3	VSTI Oxide Dep					
3.01	Strip PR, Preclean	TEL, CON Gox Dummy 1-4	matrix sink8, sink 6	2.5mins, 400W, 200C Pirahna, 10mins 120C / BHF, 10sec		3/29/2011
3.02	Pad oxide	TEL Gox Dummy 1-4	tystar1	1GATEOXA Oxidation: 780 C, 00:01:05 Ramp: 00:35:00 Anneal: 950 C, 00:30:00	Immediately load into tystar11/tystar9	3/29/2011
3.03	Deposit PSG	t4, t6, t7, t8 d3.1-4	tystar11	11SDLTOA, 00:26:00	Thickness ~3000 A	3/29/2011
3.04	Anneal PSG	t4, t6, t7, t8 d3.1-4	tystar2	2HIN2ANA, 01:00:00, 1000C		3/29/2011
3.05	Deposit nitride	t9, t10 d3.5-8	tystar9	9SNITA, 01:15:00	Thickness ~2800 A	
3.06	PSG ER	d3.1, d3.4	nanoduv	MXP-OXSP-ETCH	PSG ER ~66 A/sec	3/29/2011
3.07	Etch oxide	t4, t6, t7, t8	centura-mxp	MXP-OXSP-ETCH	Do O2 clean before Time: 46 sec	3/29/2011
3.08	Nitride ER	d3.5, d3.8	centura-mxp	MSP_NIT-ME	Nit ER ~34 A/sec	3/29/2011
3.09	Etch nitride	t9, t10	centura-mxp	MXP-NIT-ME	Time: 83 sec	3/29/2011

4	Vt Adjust Implant					
4.01	sink8, sink6 clean		sink8 sink6	Pirahna, 10mins 120C / NO HF dip Pirahna 10mins 120C, 5sec 25:1 HF, 2sec transfer to QDR	HF dip time: 5sec+2sec transfer	3/31/2011
4.02	Thin LTO Screen Oxide	TEL, CON d4.1-4	tystar11	11THIN: 450C, 300mT, 02=90sccm, SiH4=1sccm, 00:16:00	Thickness ~ 10-11 nm	3/31/2011
4.03	Boron Channel implant	TEL, CON	CORE	Boron, 4e12, 15keV, 7deg		3/31/2011
4.04	Thin LTO Strip	TEL, CON d4.1, d4.4	sink7	100:1 HF 49%	ER PSG: 3.0A/sec ER LTO: 2.1A/sec Dummy on both sides of dev wafers were beading	3/31/2011
4.05	sink6 clean	TEL, CON	sink6	Pirahna, 10mins 120C / NO HF dip		4/1/2011
4.06	Anneal/Activation	TEL, CON	tystar2	2N2ANNLA, 900C, 01:00:00		4/1/2011
5	Active Area/Mesa Isolation					
5.01	Coat PR	TEL, CON d5.1-2	svgcoat6	1, 2, 1		4/2/2011
5.02	Expose PR	TEL, CON d5.1-2	asml	DEVGRPCLR - ACTV (Image 3)		4/2/2011
5.03	Develop PR	TEL, CON d5.1-2	svgdev6	1, 1, 9		4/2/2011
5.04	Hard Bake	TEL, CON d5.1-2	uvbake	Process U		4/2/2011
5.05	VSTI PSG Etch	t4, t6, t7, t8	centura-mxp	MXP-OXIDE-ETCH	Time: 10 sec	4/2/2011
5.06	VSTI Nit Etch	t9, t10	centura-mxp	MXP-NIT-ME	Time: 21 sec	4/2/2011
5.07	Si ER Test	d5.1	lam8	8003 OB/ME/OE	ME ER: 3.7 nm/sec OE ER: 2.0 nm/sec	4/2/2011
5.08	Si Etch	TEL, CON	lam7	8003 OB/ME/OE	CON: 3/21/15 (10% OE) TEL: 3/8/34 (10% OE)	4/2/2011
5.09	Strip PR, Sink8 clean	TEL, CON	matrix, sink8	Pirahna, 10mins 120C / BHF, 10sec		4/2/2011
6	Gate Stack					
6.01	RCA Clean msink6		msink6	RCA clean 10:1 bath	Time: overnight	4/9/2011
6.02	TCA Clean tystar1		tystar1	1TCA	Time: overnight	4/9/2011

6.03	Sink8, Sink6 clean	TEL, CONT Gox Dummy 1-4	msink8 msink6 msink6	120C Pirahna 120C Pirahna 100:1 HF	Time: 10min Time: 10min Time: 10-20sec	4/9/2011
6.04	Gate Oxidation/Densify	TEL, CONT Gox Dummy 1-4	tystar1	1GATEOXA, 780C, 00:01:05 Ramp to 950C, 00:35:00 950C anneal, 00:30:00	Time: 00:01:05 Time: 00:35:00 Time: 00:30:00	4/9/2011
6.05	Measure oxide thickness	Gox Dummy	sopra		Thickness| 2.5nm	4/9/2011
6.06	Poly Deposition	TEL, CONT ox7.1-5	tystar 10	10SDPLYA, 01:35:00	Thickness ~160 nm	4/9/2011
6.07	LTO hardmask deposition	TEL, CONT ox7.1-3, d7.1-2	tystar11	11SULTOA, 00:12:00	Thickness ~145 nm	4/11/2011
7	Gate Patterning					
7.01	Coat BARC	TEL, CONT	svgcoat6	9, 4, 9	AR3-600 Rohm Haas BARC 3750RPM, 30sec	4/12/2011
7.02	BARC Bake	TEL, CONT	svgcoat6	9, 9, 1	213C, 60sec	4/12/2011
7.03	Coat PR	TEL, CONT ox7.1-3	svgcoat6	9, 2, 1		4/12/2011
7.04	Expose PR	TEL, CONT ox7.1-3	asml	DEVGRPCLR - POLY (Image 1)		4/12/2011
7.05	Develop PR	TEL, CONT ox7.1-3	svgdev6	1, 1, 9		4/12/2011
7.06	Hard Bake	TEL, CONT ox7.1-3	uvbake	Process U		4/12/2011
7.07	Gate CD Measurement	TEL, CONT	leo		Linewidth ~ 200nm for 250nm drawn	4/12/2011
7.08	Resist Trim	TEL, CONT	matrix	280W, 125C ER ~2nm/sec	CONT: Time = 00:01:10 TEL: Time = 00:01:20	4/12/2011
7.09	Gate CD Measurement	TEL, CONT	leo			4/12/2011
7.1	LTO hardmask etch	TEL, CONT	centura-mxp	MXP-OXIDE-ETCH ER ~75A/sec, 15% OE	Time: 15 sec *7 hrs after PR ashing	4/13/2011
7.11	Strip PR	TEL, CONT	matrix	2.5mins, 400W, 200C		4/13/2011
7.12	Polymer Removal	TEL, CONT	sink7	100:1 HF	Time: 15sec	4/13/2011

7.13	Gate CD Measurement	DEV	leo		Linewidth ~ 100-120 nm	4/13/2011
7.14	Oxide Trimming	TEL, CON	msink7	100:1 HF LTO ER: 2 A/sec	TEL: 210 sec CON: 100 sec	4/13/2011
7.15	Gate CD Measurement	TEL, CON	leo		Linewidth ~ 40-60 nm	4/13/2011
7.16	Poly ER Test	ox7.4-5	lam8	8003 OB/ME/OE - 3s/10s/0s 8003 OB/ME/OE - 3s/10s/10s	ME ER ~ 48 A/sec OE ER ~ 21 A/sec	4/18/2011
7.17	Poly gate Etch	ox7.1-3 TEL, CONT	lam8	8003 OB/ME/OE - 3s/16s/20s	50% ME, 50% OE * No thickness OE, selectivity issue	4/18/2011
7.18	Preclean	TEL, CONT Gox Dummy	msink6	120C Pirahna 100:1 HF	Time: 10min Time: 20sec	4/19/2011
7.19	Poly Reoxidation	TEL, CONT Gox Dummy	tystar1	1GATEOXA, 840C, 00:05:00 Ramp to 900C, 00:15:00 900C anneal, 00:30:00	Thickness ~3.4 nm	4/19/2011
7.2	Litho for Die Dropout	TEL, CON	litho tools	Half of dies are opened for LDD, HALO		4/19/2011
8	SDE/Halo Implant					
8.01	N-type S/D extension	TEL, CONT	CORE	As+ / 10keV / 1e13 / 7deg tilt		4/19/2011
8.02	P-type halo doping	TEL, CONT	CORE	B+ / 15keV / 3e12 x 4 / 30deg tilt	0, 90, 180, 270deg wafer rotation 4 implant total	4/19/2011
9	Spacer Formation					
9.01	msink6 Clean	TEL, CONT ox9.1-3, d9.1-2	msink6	120C Pirahna 100:1 HF	Time: 10min Time: 20sec @ 0.4A/s (2nm)	4/26/2011
9.02	Nitride Deposition	TEL, CONT ox9.1-3, d9.1-2	tystar9	9SNITA, 00:06:00		4/26/2011
9.03	Nit ER Test	ox9.1-3, d9.1-2	centura-mxp	MXP-NIT-OE		4/26/2011
9.04	Nit Spacer Etch	TEL, CONT	centura-mxp	MXP-NIT-OE	Time: 00:00:30 Endpt	4/26/2011
10	LTO Implant Screen					
10.1	Polymer Removal	TEL, CONT	msink8 sink7	Piranha, 10min 100:1 HF, 15 sec		4/27/2011
10.2	Preclean	TEL, CONT d10.1-4	msink6	Piranha, 10min 100:1 HF, 10 sec		4/27/2011

10.3	LTO Deposition	TEL, CONT d10.1-4	tystar11	11THIN: 450C, 300mT, 02=90sccm, SiH4=1sccm, 00:16:00		4/27/2011
11	DSD Implant					
11.01	N-type DSD implant	TEL, CONT	CORE	As+ / 15keV / 1e15 / 7deg tilt		4/27/2011
12	SPER + LTO Passivation					
12.01	Preclean	TEL, CONT d10.1-4	msink6	Pirahna, 120C 100:1 HF, 20 sec		4/28/2011
12.02	SPER	TEL, CONT	tystar2	2LTANNLA		4/28/2011
12.03	LTO Passivation Depo	TEL, CONT d12.1-4	tystar11	11SULTOA, 00:08:00		4/28/2011
12.04	Activation anneal		heatpulse4	900C, 20sec	Time: 00:00:20	4/29/2011
13	Contact Definition					
13.01	Coat PR	TEL, CON d12.1-4	svgcoat6	1, 2, 1		4/29/2011
13.02	Expose PR	TEL, CON d12.1-4	asml	DEVGRPDARK - CONT (Image 1)		4/29/2011
13.03	Develop PR	TEL, CON d12.1-4	svgdev6	1, 1, 9		4/29/2011
13.04	Hard Bake	TEL, CON d12.1-4	uvbake	Process U		4/29/2011
13.05	LTO ER Test	d12.1-4	centura-mxp	MXP-OXIDE-ETCH	ER: 10.4A/sec	4/29/2011
13.06	LTO Dry Etch	TEL, CON	centura-mxp	MXP-OXIDE-ETCH	Etch LTO passivation thickness Check contact area over large Poly pad	4/29/2011
13.07	LTO Wet Etch	TEL, CON	msink7	50:1 HF	Time: 00:00:20	4/29/2011
14	Metal Deposition					
14.01	TiN/Al sputter	TEL, CON	UHV Sputtering	backsputter, 50A TiN, 950A Al/2%Si		4/30/2011
15	Metal Definition					
15.01	Coat PR	TEL, CON d14.1-4	svgcoat6	1, 2, 1		5/9/2011
15.02	Expose PR	TEL, CON d14.1-4	asml	DEVGRPDARK - CONT (Image 1)		5/9/2011
15.03	Develop PR	TEL, CON	svgdev6	1, 1, 9		5/9/2011

		d14.1-4				
15.04	Hard Bake	TEL, CON d14.1-4	uvbake	Process U		5/9/2011
15.05	Al ER Test	d14.1-4	lam7	7003		5/9/2011
15.06	Al Etch	TEL, CON	lam7	7003	Time: 00:00:12	5/9/2011
15.07	Strip PR, Metal Clean	TEL, CON	matrix msink5	2.5min, 400W, 250C metal Clean bath		5/9/2011
16	Sintering					
16.01	Al Sintering	TEL, CON	tystar18	H2SINT4A, 00:30:00, 400C		5/10/2011

Appendix B

$Si_{1-x}Ge_x/Si$ p-channel SegFET Process Flow

AMAT SegFET PMOS PROCESS FLOW AMAT = a13, a14, a15, a16, a17, a18, a21, a22, a23 CON = a3, a4, a7, a8						
Step #	Process	Wafers	Tool Name	Description	Notes	Date Done
0	Receive corrugated substrates from AMAT					
0.1	Strip PR Preclean	AMAT	sink432c msink8	PRS-3000, 80C, 10mins/DI rinse Pirahna, 10mins 120C / BHF, 10sec		
1	Clear die for PM marks					
1.01	Coat PR	AMAT, CON d1.1	svgcoat6	1, 2, 1		9/3/2011
1.02	Expose PR	AMAT, CON d1.1	asml300	Kim's Clear exposure test mask		9/3/2011
1.03	Develop PR	AMAT, CON d1.1	svgdev6	1, 1, 9		9/3/2011
1.04	Hardbake	AMAT, CON d1.1	uvbake	Process U		9/3/2011
1.05	Si ER Test	d1.1	lam8	8003 OB/ME (3s/10s) asiq	Si ER ~5.5 nm/min	9/6/2011
1.06	Si Etch	AMAT, CON	lam8	8003 OB/ME nanoduv	TEL: 31 sec CON: 32 sec	9/6/2011
1.08	Oxide ER Test	ox1.1	centura-mxp	MXP-OXIDE-ETCH	Ox ER: 70 A/sec	9/6/2011

1.09	Oxide etch	AMAT, CON	centura-mxp	MXP-OXIDE-ETCH	TEL: 17 sec CON: 26 sec	9/6/2011
2	PM Marks					
2.01	Strip PR, Preclean	AMAT, CON d2.1	matrix msink8	2.5mins, 400W, 200C Pirahna, 10mins 120C 5:1 HF, 30sec	(remove residual BOX)	9/8/2011
2.02	Coat PR	AMAT, CON d2.1	svgcoat6	1, 2, 1		9/8/2011
2.03	Expose PR	AMAT, CON d2.1	asml	combi reticle Apply same wafer rotation		9/8/2011
2.04	Develop PR	AMAT, CON d2.1	svgdev6	1, 1, 9		9/8/2011
2.05	Hardbake	AMAT, CON d2.1	uvbake	Process U		9/8/2011
2.06	Si ER Test	d1.1	lam8	8003 OB/ME (3s/10s) asiq	Si ER ~4.0 nm/min	9/9/2011
2.08	Si Etch	AMAT, CON	lam8	8003 OB/ME	Time: 30 sec	9/9/2011
3	VSTI Oxide Dep					
	N/A					
4	Vt Adjust Implant					
4.01	sink8, sink6 clean		sink8 sink6	Pirahna, 10mins 120C / NO HF dip Pirahna 10mins 120C, 5sec 25:1 HF, 2sec transfer to QDR	HF dip time: 5sec+2sec transfer	10/1/2011
4.02	Thin LTO Screen Oxide	AMAT, CON d4.1-4	tystar11	11THIN: 450C, 300mT, 02=90sccm, SiH4=1sccm, 00:16:00	Thickness ~ 10-11 nm	10/1/2011
4.03	Arsenic Channel implant	AMAT, CON	CORE	Arsenic, 3e12, 35keV, 7deg		10/7/2011
4.04	Thin LTO Strip	AMAT, CON d4.1, d4.4	sink7	100:1 HF 49%	ER LTO: 2.1A/sec Dummy on both sides of dev wafers were beading	10/18/2011
5	Active Area/Mesa Isolation					
5.01	Coat PR	AMAT, CON d5.1-2	svgcoat6	1, 2, 1		10/19/2011
5.02	Expose PR	AMAT, CON d5.1-2	asml	DEVGRPCLR - ACTV (Image 3)		10/19/2011
5.03	Develop PR	AMAT, CON d5.1-2	svgdev6	1, 1, 9		10/19/2011

5.04	Hard Bake	AMAT, CON d5.1-2	uvbake	Process U		10/19/2011
5.05	Si ER Test	d5.1	lam8	8003 OB/ME/OE	ME ER: 3.7 nm/sec OE ER: 2.0 nm/sec	10/19/2011
5.06	Si Etch	AMAT, CON	lam8	8003 OB/ME/OE	CON: 3/21/15 (10% OE) AMAT: 3/8/34 (10% OE)	10/19/2011
5.07	Strip PR, Sink8 clean	AMAT, CON	matrix, sink8	Pirahna, 10mins 120C / BHF, 10sec		10/19/2011
6	Gate Stack					
6.01	RCA Clean msink6		msink6	RCA clean 10:1 bath	Time: overnight	10/24/2011
6.02	TCA Clean tystar1		tystar1	1TCA	Time: overnight	10/24/2011
6.03	Sink8, Sink6 clean	AMAT, CON Gox Dummy 1-4	msink8 msink6 msink6	120C Pirahna 120C Pirahna 100:1 HF	Time: 10min Time: 10min Time: 10-20sec	10/25/2011
6.04	Gate Oxidation/Densify	AMAT, CON Gox Dummy 1-4	tystar1	1GATEOXA, 750C, 00:05:00 Ramp to 750C, 00:00:10 750C anneal, 00:10:00	Time: 00:05:00 Time: 00:00:10 Time: 00:10:00	10/25/2011
6.05	Measure oxide thickness	Gox Dummy	sopra		Thickness| 2.3nm	10/25/2011
6.06	Poly Deposition	AMAT, CON ox7.1-5	tystar 19	Nucleation: 100sccm Si2H6, 300mT, 425C Depo: 170sccm SiH4, 15sccm GeH4, 15sccm BCL3, 425C, 400mT	Time: 00:05:00 Time: 01:30:00	10/25/2011
6.07	LTO hardmask deposition	TEL, CONT ox7.1-3, d7.1-2	tystar11	11SULTOA, 00:12:00	Thickness ~145 nm	10/25/2011
7	Gate Patterning					
7.01	Coat BARC	AMAT, CON	svgcoat6	9, 4, 9	AR3-600 Rohm Haas BARC 3750RPM, 30sec	10/29/2011
7.02	BARC Bake	AMAT, CON	svgcoat6	9, 9, 1	213C, 60sec	10/29/2011
7.03	Coat PR	AMAT, CON ox7.1-3	svgcoat6	9, 2, 1		10/29/2011
7.04	Expose PR	AMAT, CON ox7.1-3	asml	DEVGRPCLR - POLY (Image 1)		10/29/2011
7.05	Develop PR	AMAT, CON ox7.1-3	svgdev6	1, 1, 9		10/29/2011

7.06	Hard Bake	AMAT, CON ox7.1-3	uvbake	Process U		10/29/2011
7.07	Gate CD Measurement	AMAT, CON	leo		Linewidth ~ 200nm for 250nm drawn	10/29/2011
7.08	Resist Trim	AMAT, CON	matrix	280W, 125C ER ~2nm/sec	CONT: Time = 00:01:10 TEL: Time = 00:01:20	10/29/2011
7.09	Gate CD Measurement	TEL, CONT	leo			10/29/2011
7.1	LTO hardmask etch	AMAT, CON	centura-mxp	MXP-OXIDE-ETCH ER ~75A/sec, 15% OE	Time: 15 sec	10/29/2011
7.11	Strip PR	AMAT, CON	matrix	2.5mins, 400W, 200C		10/29/2011
7.12	Polymer Removal	AMAT, CON	sink7	100:1 HF	Time: 15sec	10/29/2011
7.13	Gate CD Measurement	DEV	leo		Linewidth ~ 100-120 nm	10/29/2011
7.14	Oxide Trimming	AMAT, CON	msink7	100:1 HF LTO ER: 2 A/sec	AMAT: 360 sec CON: 180 sec	11/2/2011
7.15	Gate CD Measurement	AMAT, CON	leo		Linewidth ~ 40-60 nm	11/2/2011
7.16	Poly ER Test	ox7.4-5	lam8	8003 OB/ME/OE - 3s/10s/0s 8003 OB/ME/OE - 3s/10s/10s	ME ER ~ 48 A/sec OE ER ~ 21 A/sec	11/7/2011
7.17	Poly gate Etch	ox7.1-3 AMAT, CON	lam8	8003 OB/ME/OE - 3s/20s/15s	50% ME, 50% OE * No thickness OE, selectivity issue	11/7/2011
7.18	Preclean	AMAT, CON Gox Dummy	msink6	120C Pirahna 100:1 HF	Time: 10min Time: 20sec	11/8/2011
7.19	Poly Reoxidation	AMAT, CON Gox Dummy	tystar1	1GATEOXA, 750C, 00:05:00 Ramp to 750C, 00:00:10 750C anneal, 00:10:00	Thickness ~2.3 nm	11/8/2011
8	SDE/Halo Implant					
8.01	P-type S/D extension	AMAT, CON	CORE	BF_2 / 12keV / 1e13 / 7deg tilt		11/9/2011
8.02	N-type halo doping	AMAT, CON	CORE	P+ / 60keV / 1e12 x 4 / 30deg tilt	0, 90, 180, 270deg wafer rotation 4 implant total	11/9/2011
9	Spacer Formation					
9.01	msink6 Clean	AMAT, CON ox9.1-3, d9.1-2	msink6	120C Pirahna 100:1 HF	Time: 10min Time: 20sec @ 0.4A/s (2nm)	11/18/2011
9.02	LTO Deposition	AMAT, CON	tystar11	11THIN: 450C, 300mT, 02=90sccm, SiH4=1sccm, 00:50:00	~31nm	11/18//2011

		ox9.1-3, d9.1-2				
9.03	LTO ER Test	d9.1-2	centura-mxp	MXP-OXSP-ETCH	ER: 45.5 A/sec	11/18/2011
9.04	LTO Spacer Etch	AMAT, CON	centura-mxp	MXP-OXSP-ETCH	Time: 00:00:07	11/18/2011
10	LTO Implant Screen					
10.01	Polymer Removal	TEL, CONT	msink8 sink7	Piranha, 10min 100:1 HF, 15 sec		11/18/2011
10.02	Preclean	AMAT, CON d10.1-4	msink6	Piranha, 10min 100:1 HF, 10 sec		11/18/2011
10.03	LTO Deposition	AMAT, CON d10.1-4	tystar11	11THIN: 450C, 300mT, 02=90sccm, SiH4=1sccm, 00:16:00		11/18/2011
11	DSD Implant					
11.01	P-type DSD implant	AMAT, CON	CORE	BF_2 / 15keV / 1e15 / 7deg tilt		11/19/2011
12	SPER + LTO Passivation					
12.01	Preclean	AMAT, CON d10.1-4	msink6	Pirahna, 120C 100:1 HF, 20 sec		11/22/2011
12.02	SPER	AMAT, CON	tystar2	2LTANNLA 500C	Time: 01:00:00	11/22/2011
12.03	LTO Passivation Depo	AMAT, CON d12.1-4	tystar11	11SULTOA, 00:24:00		11/22/2011
12.04	Activation anneal	AMAT, CON	heatpulse4	900C, 10sec		11/22/2011
13	Contact Definition					
13.01	Coat PR	AMAT, CON d12.1-4	svgcoat6	1, 2, 1		11/29/2011
13.02	Expose PR	AMAT, CON d12.1-4	asml	DEVGRPDARK - CONT (Image 1)		11/29/2011
13.03	Develop PR	AMAT, CON d12.1-4	svgdev6	1, 1, 9		11/29/2011
13.04	Hard Bake	AMAT, CON d12.1-4	uvbake	Process U		11/29/2011
13.05	LTO ER Test	d12.1-4	centura-mxp	MXP-OXIDE-ETCH	ER: 60 A/sec	11/29/2011
13.06	LTO Dry Etch	AMAT, CON	centura-mxp	MXP-OXIDE-ETCH	Etch LTO passivation thickness, Time: 45s Check contact area over large Poly pad	1129/2011
13.07	LTO Wet Etch	AMAT,	msink7	50:1 HF		11/29/2011

		CON				
14	Metal Deposition					
14.01	TiN/Al2%Si	AMAT, CON	UHV Sputtering	50A TiN 3000A Al/2%Si		12/1/2011
15	Metal Definition					
15.01	Coat PR	AMAT, CON d14.1-4	svgcoat6	1, 2, 1		12/13/2011
15.02	Expose PR	AMAT, CON d14.1-4	asml	DEVGRPDARK - CONT (Image 1)		12/13/2011
15.03	Develop PR	AMAT, CON d14.1-4	svgdev6	1, 1, 9		12/13/2011
15.04	Hard Bake	AMAT, CON d14.1-4	uvbake	Process U		12/13/2011
15.05	Al ER Test	d14.1-4	centura-met	MET-AL-ME		12/15/2011
15.06	Al Etch	AMAT, CON	Centura-met	MET-AL-ME	Time: 40sec Finish with wet Al etch	12/15/2011
15.07	Strip PR, Metal Clean	AMAT, CON	matrix msink5	2.5min, 400W, 250C metal Clean bath		12/15/2011
16	Sintering					
16.01	Al Sintering	AMAT, CON	tystar18	400C, 00:30:00		12/15/2011