Planar Bulk CMOS Scaling to the End of the Road

Prof. Tsu-Jae King Liu

Electrical Engineering and Computer Sciences Department
University of California at Berkeley

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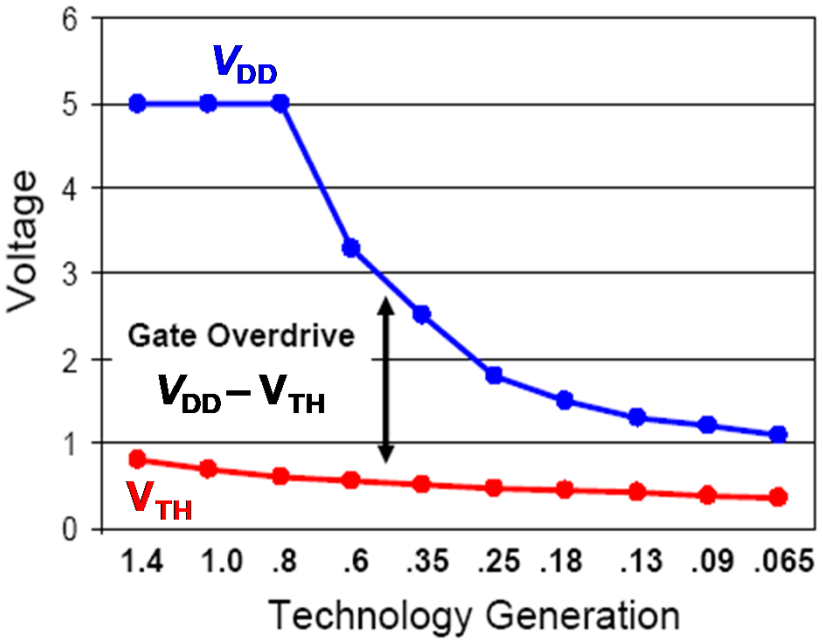
Outline

- **Where We Are Now**
  - **The CMOS Power Crisis**
- **The Road to Now**
  - **Recent Advancements in CMOS Technology**
- **The Road Not (yet) Taken**
  - **Evolution of the Planar Bulk MOSFET**
- **Summary**

The CMOS Power Crisis

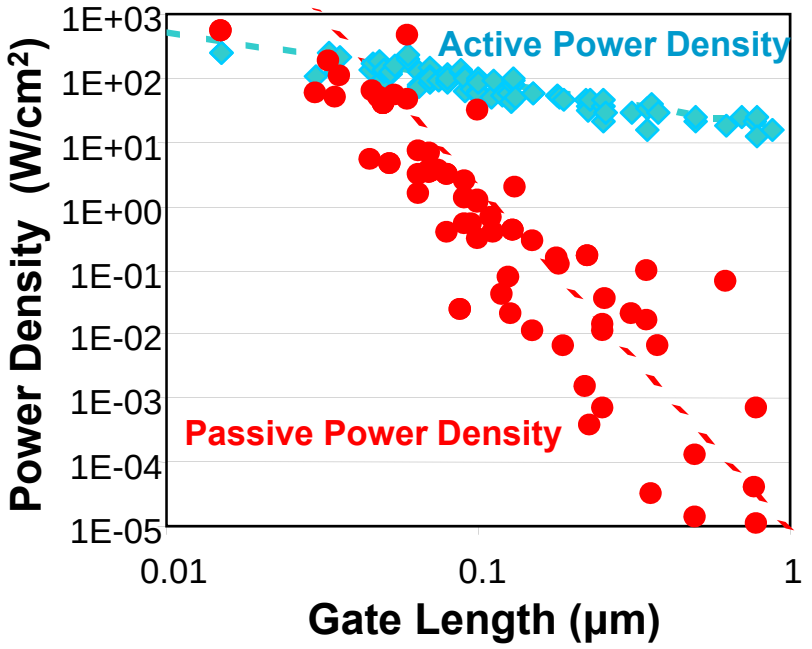
- **As transistor density has increased, the supply voltage (V_{DD}) has not decreased proportionately.**
  - **→ Power density now constrains CMOS chip design!**

CMOS Voltage Scaling



Source: P. Packan (Intel), 2007 IEDM Short Course

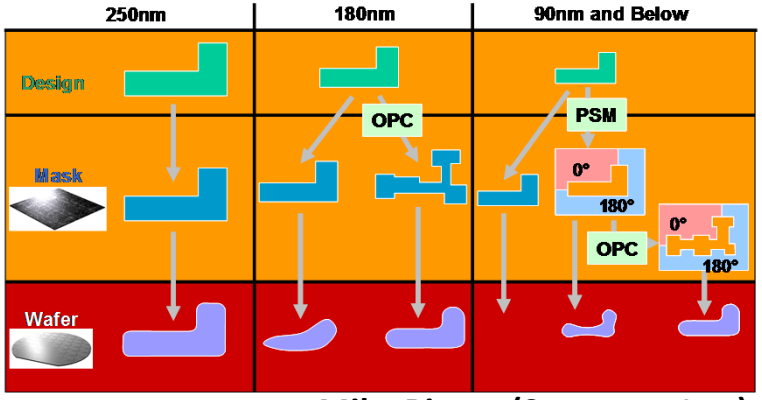
Power Density vs. Gate Length



Source: B. Meyerson (IBM) Semico Conf., January 2004

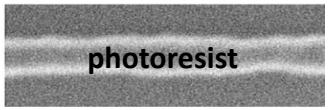
Process-Induced Variations

- **Sub-wavelength lithography:**
  - **Resolution enhancement techniques are costly and increase process sensitivity**

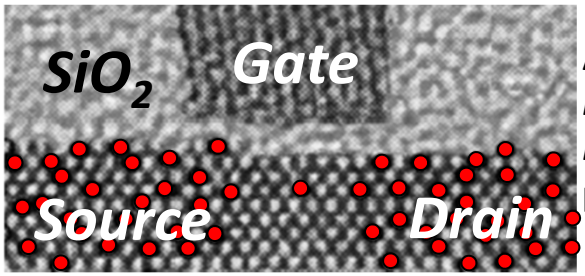


courtesy Mike Rieger (Synopsys, Inc.)

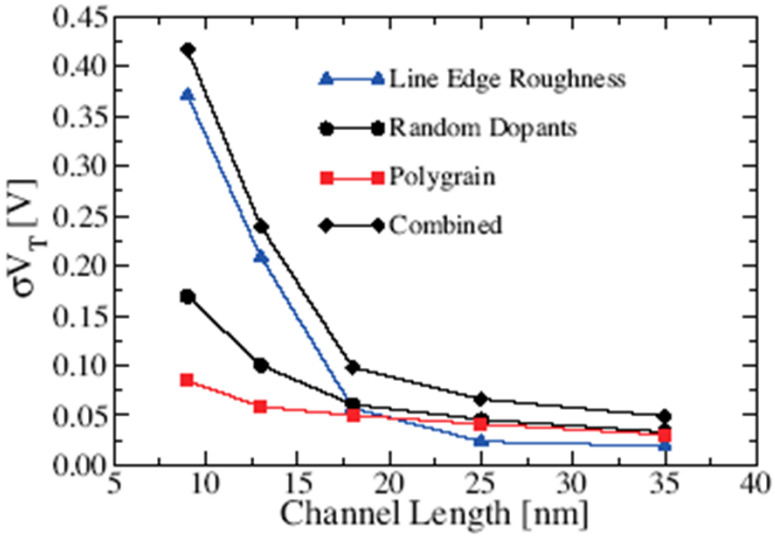
- **Gate line-edge roughness:**



- **Random dopant fluctuations (RDF):**
  - **Atomistic effects become significant in nanoscale FETs**



A. Brown *et al.*, *IEEE Trans. Nanotechnology*, p. 195, 2002



A. Asenov, *Symp. VLSI Tech. Dig.*, p. 86, 2007

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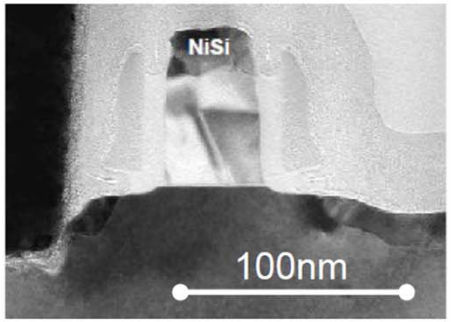
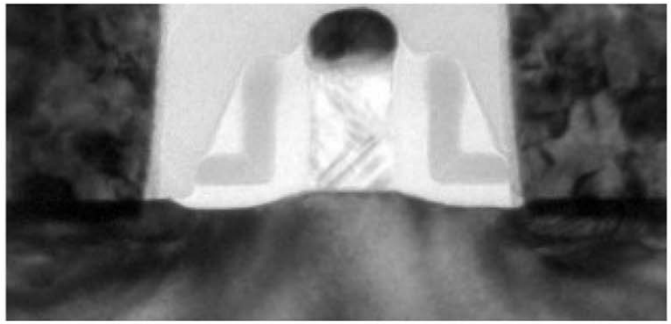
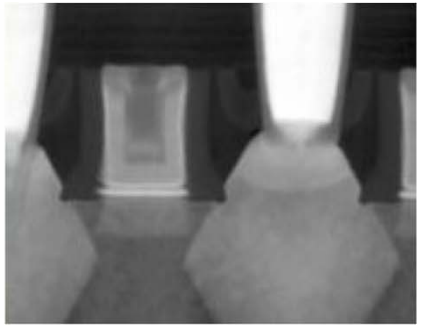
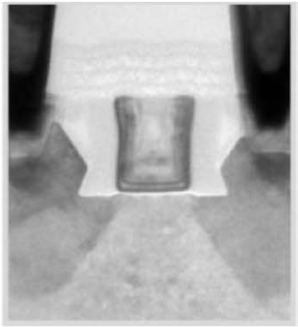
CMOS Technology Advancement

XTEM images with the same scale

courtesy V. Moroz (Synopsys, Inc.)

90 nm node	65 nm node	45 nm node	32 nm node
			
T. Ghani *et al.*, *IEDM* 2003	(after S. Tyagi *et al.*, *IEDM* 2005)	K. Mistry *et al.*, *IEDM* 2007	P. Packan *et al.*, *IEDM* 2009

strained Si →

high-k/metal gate stack →

- **The transistor gate length (L_g) has not scaled proportionately with device pitch in recent generations.**
  - **Transistor performance has been boosted by other means.**

Bulk MOSFET Design Optimization

R.-H. Yan *et al.*, *IEEE Trans. Electron Devices*, Vol. 39, pp. 1704-1710, 1992

- To maximize I_{ON} and minimize V_{TH} variation, heavy doping near the surface of the channel region should be avoided.

  → Use a steep retrograde channel doping profile to suppress I_{OFF}

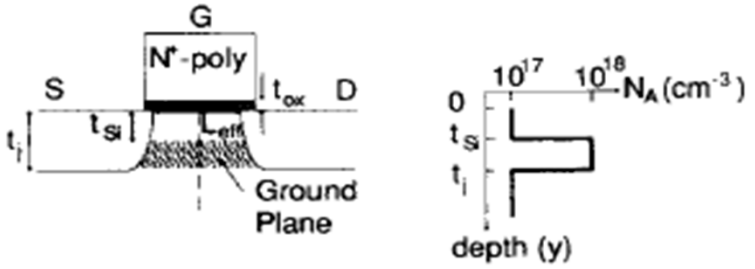
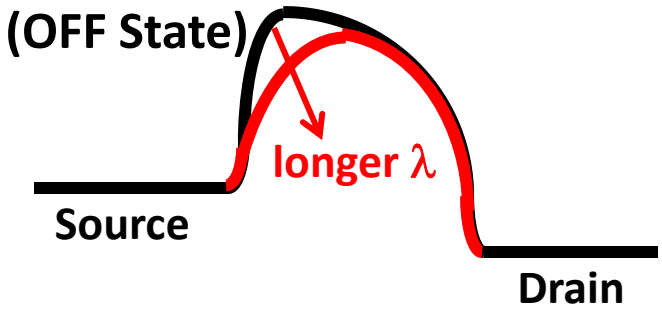


Fig. 6. The Pulse-Shaped Doped structure. (a) Cross-section view of the structure. (b) Vertical doping profile. The example used in Fig. 7 has L_{eff} = 0.1 μm, t_{ox} = 40 Å, t_{Si} = 250 Å, t_j = 500 Å, and the doping profile shown in Fig. 6(b).

- The thickness of the lightly doped channel region, t_{Si}, is a critical design parameter.

Energy Band Profile:



Structure:	Double-Gate FET	Ground-Plane FET
Scale length:	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{Si} t_{ox}}$	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} \frac{t_{Si} t_{ox}}{1+\left(\varepsilon_{Si} t_{ox} / \varepsilon_{ox} t_{Si}\right)}}$

Carrier Confinement w/o Doping

R. J. Mears *et al*. (Mears Technologies), *2012 Silicon Nanoelectronics Workshop*

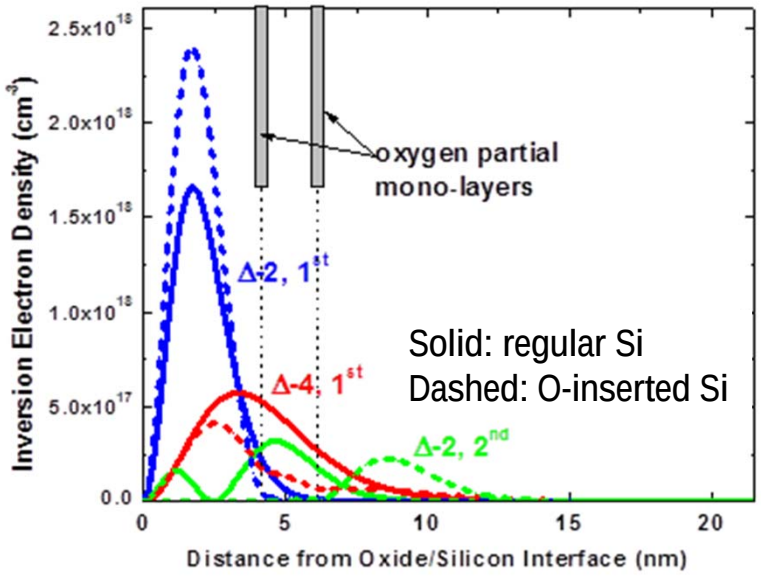
- **Inversion charge is confined to be near the surface, by inserting O partial mono-layers within the channel region**

  → relaxes requirement for thin t_{Si}

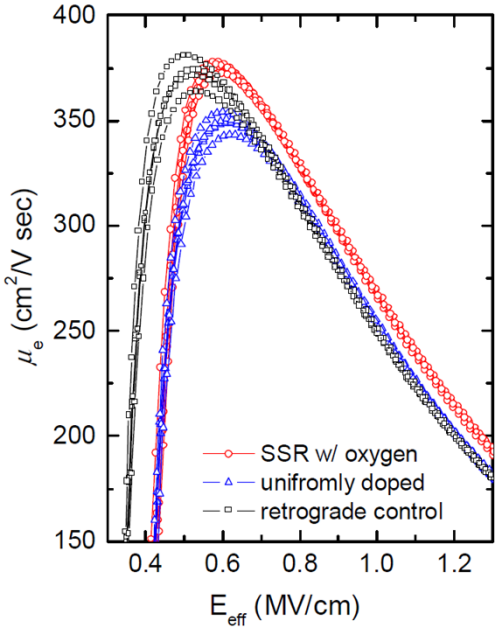
- **Separation of carrier sub-bands reduces inter-band scattering**

  → carrier mobility is enhanced

Inversion-charge density profile



Effective electron mobility



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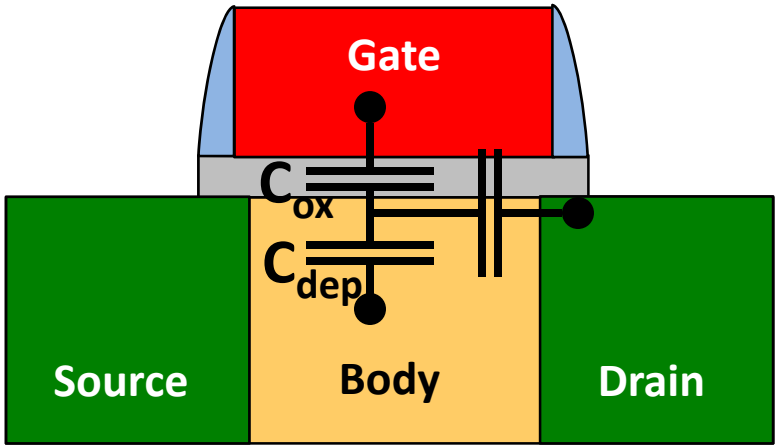
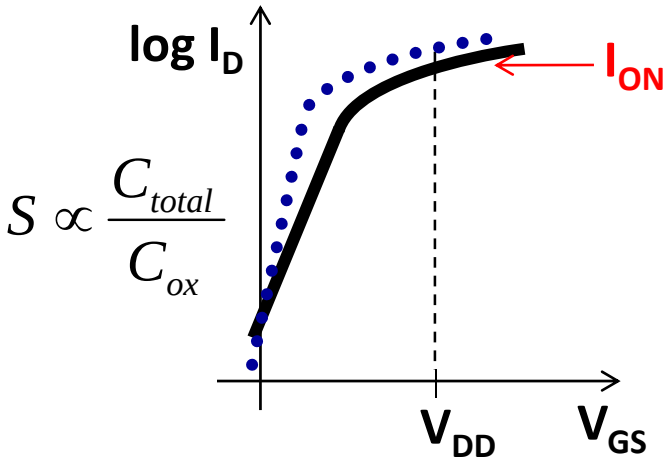
Key to L_g Scaling: Improved Gate Control

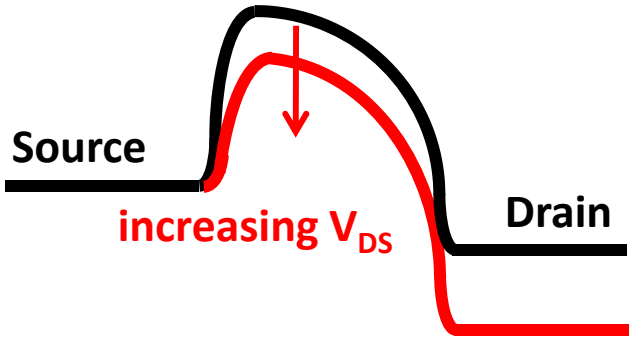


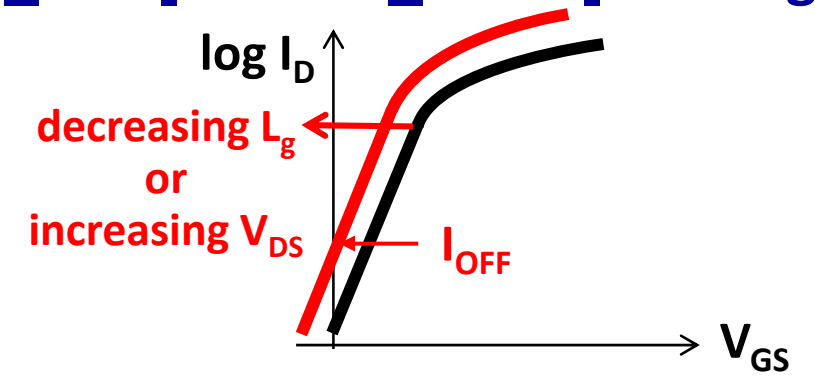


- **The greater the capacitive coupling between Gate and channel, the better control the Gate has over the channel potential.**

  →higher I_{ON}/I_{OFF} for fixed V_{DD}, or lower V_{DD} to achieve target I_{ON}/I_{OFF}

  →reduced short-channel effect and drain-induced barrier lowering:



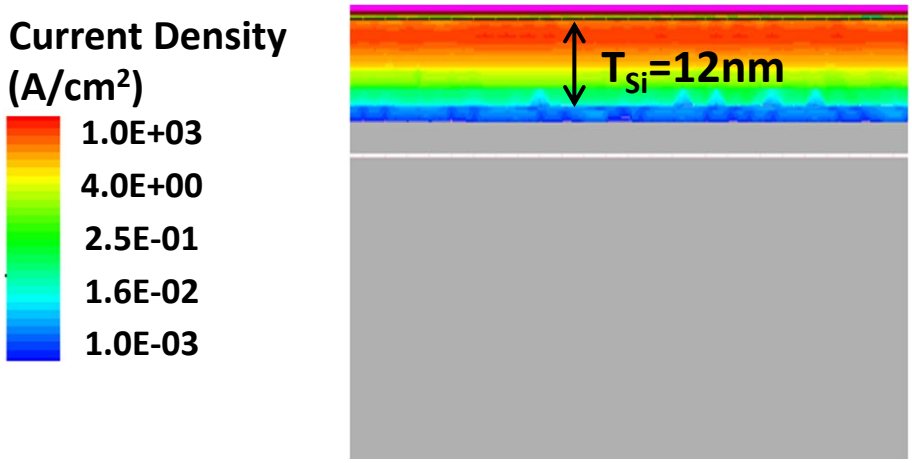


Off-State Leakage Contour Plots

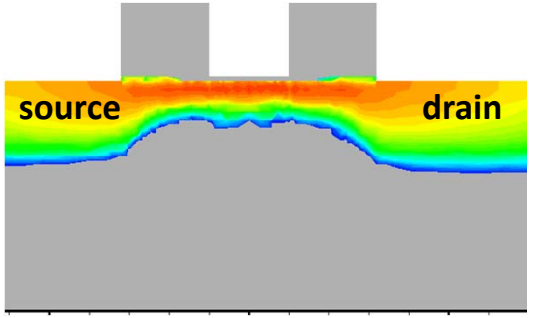
L_g=20nm, L_{eff}=18nm, EOT = 0.9nm, V_{ds}=0.7V

Wide MOSFET

Across the channel:



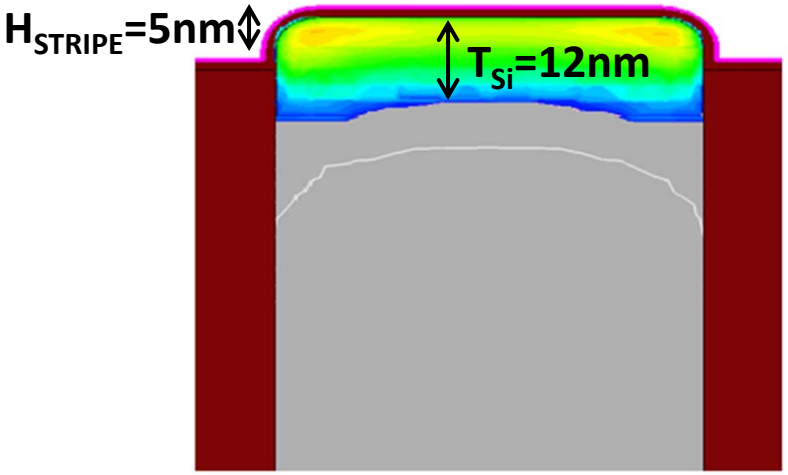
Along the channel:

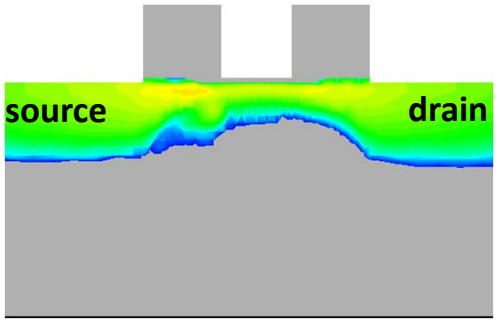


Retrograde channel doping (ground plane) is insufficient!

Narrow MOSFET

$W_{STRIPE} = 2L_g = 40$ nm





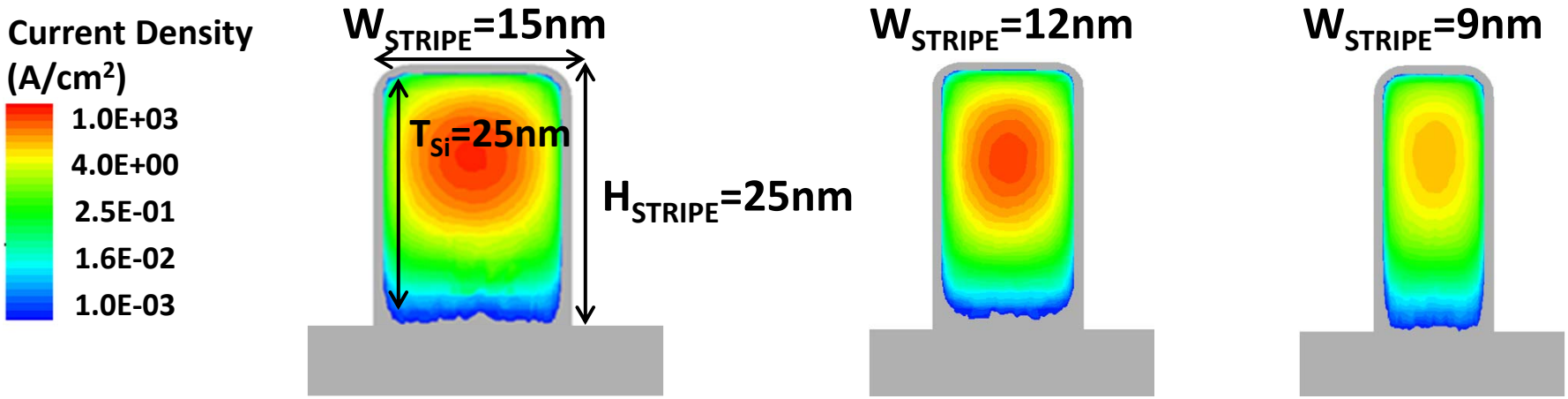
Fringing E-fields + ground plane → good gate control!

Bulk FinFET Off-State Leakage

L_g=20nm, L_{eff}=18nm, EOT = 0.9nm, V_{ds}=0.7V

Note that doping at the base of the fin is used to suppress sub-fin leakage between the source and drain regions, not to achieve good gate control.

Across the channel/fin:

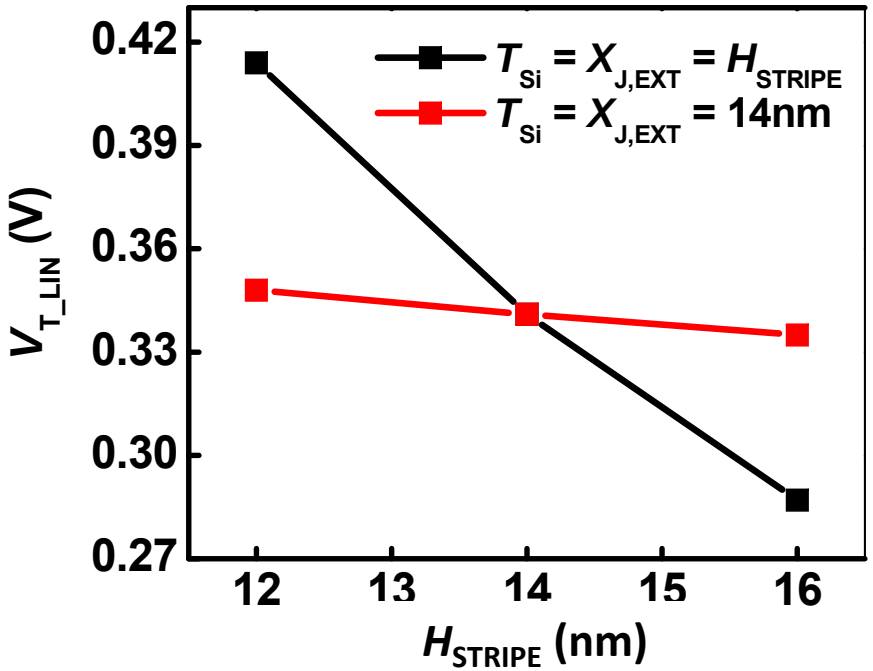


- **The FinFET requires a narrow channel region to achieve good gate control.**
  - → **Fin width must be less than 0.6×L_g to well suppress I_{OFF}**
- **Fin aspect ratio must be >1.5 for good area efficiency**
  - → **Challenging to manufacture!**

Impact of H_{STRIPE} Variation

X. Sun (UC Berkeley), Ph.D. thesis

L_g = 20nm, EOT = 0.9nm, W_{STRIPE} = 20nm



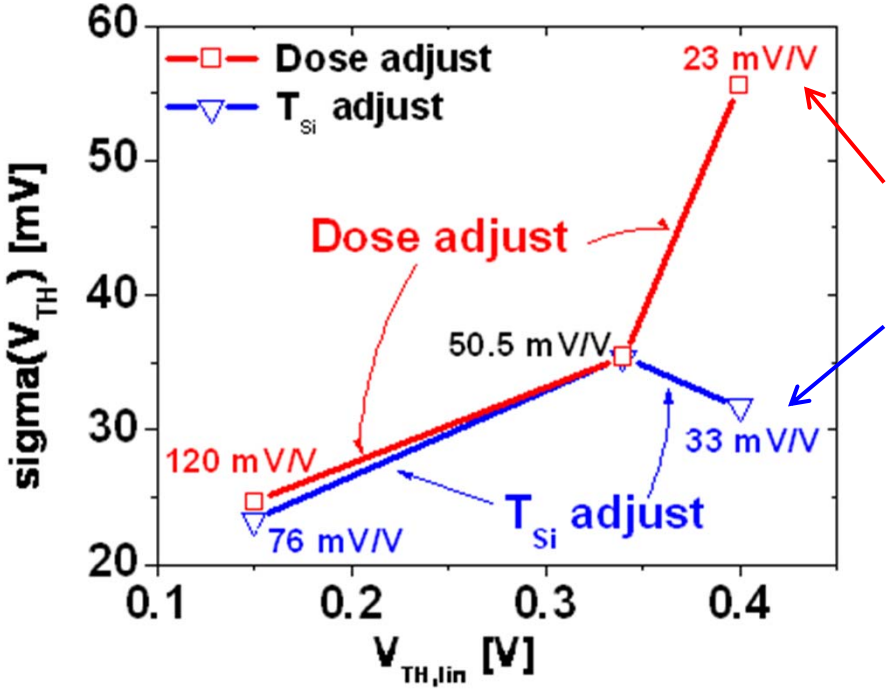
- If T_{Si} is fixed, V_{TH} is not sensitive to H_{STRIPE} variation.

V_{TH} Adjustment Approaches

C. Shin *et al.*, *IEEE 2008 Silicon Nanoelectronics Workshop*

- V_{TH} of a narrow MOSFET can be adjusted by tuning either the dose (N_{peak}) or the depth (T_{Si}) of the retrograde doping.
  - 200 atomistic simulations were run for each nominal design.
- V_{TH} adjustment via T_{Si} tuning provides for less variation, and eliminates the trade-off with short-channel control.

L_g = 20 nm
EOT = 0.9 nm
W_{STRIPE} = 20 nm
H_{STRIPE} = 14 nm
W_{eff} = 44 nm
t_{Si} = 14 nm
X_J = 14 nm



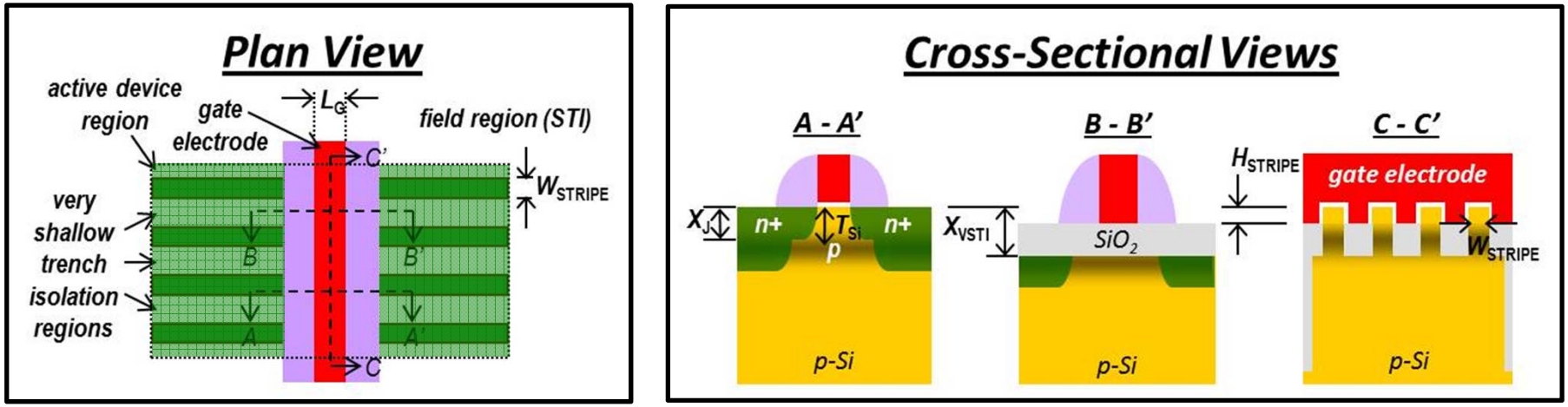
DIBL values for each design are indicated

Segmented Channel MOSFET (SegFET)

- Channel region comprises stripes of equal width ≥ L_g, isolated by very shallow trench isolation (vSTI).
  - vSTI is much shallower than the STI between transistors.

→ Deep source/drain regions and ground plane are not segmented!

- Gate control is enhanced by fringing electric fields!
  - The channel stripes can be elevated above the vSTI, or a high-k vSTI dielectric can be used, to further enhance gate control.

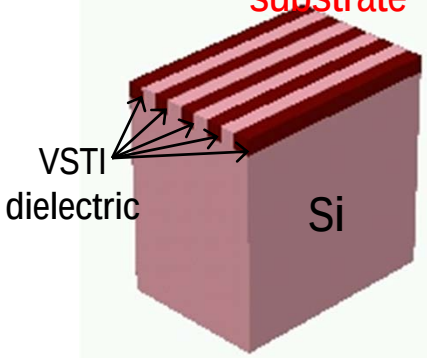


B. Ho *et al., International Semiconductor Device Research Symposium 2011*

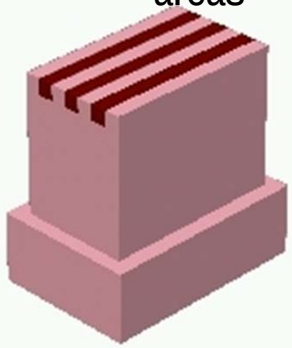
SegFET Fabrication Process

T.-J. King and V. Moroz, U.S. Patent 7,265,008

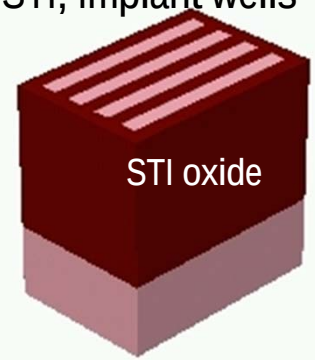
1. Start with corrugated substrate



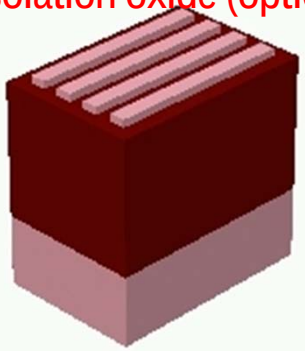
2. Define active areas



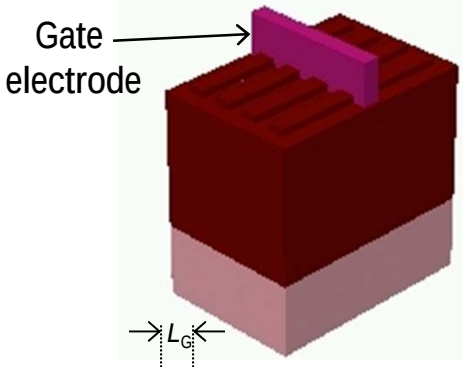
3. Fill trenches to form STI; Implant wells



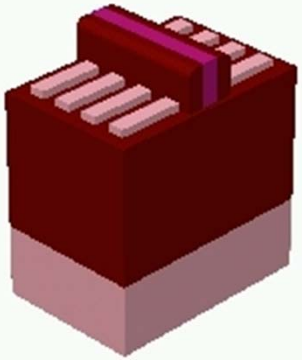
4. Slightly recess the isolation oxide (optional)



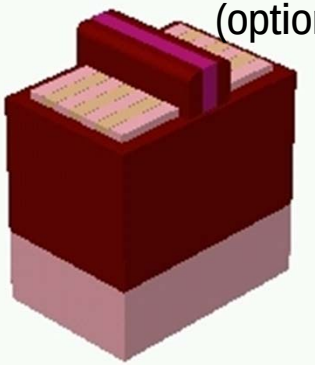
5. Implant channels; Form gate stack



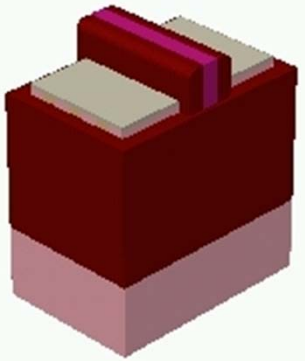
6. Form S/D extensions, then sidewall spacers

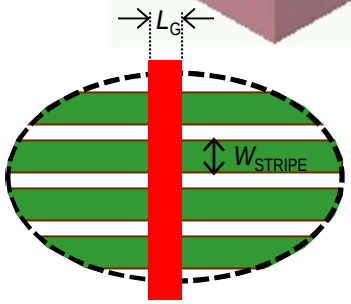


7. Embed/grow epitaxial material in S/D regions (optional)



8. Dope S/D regions; Form silicide





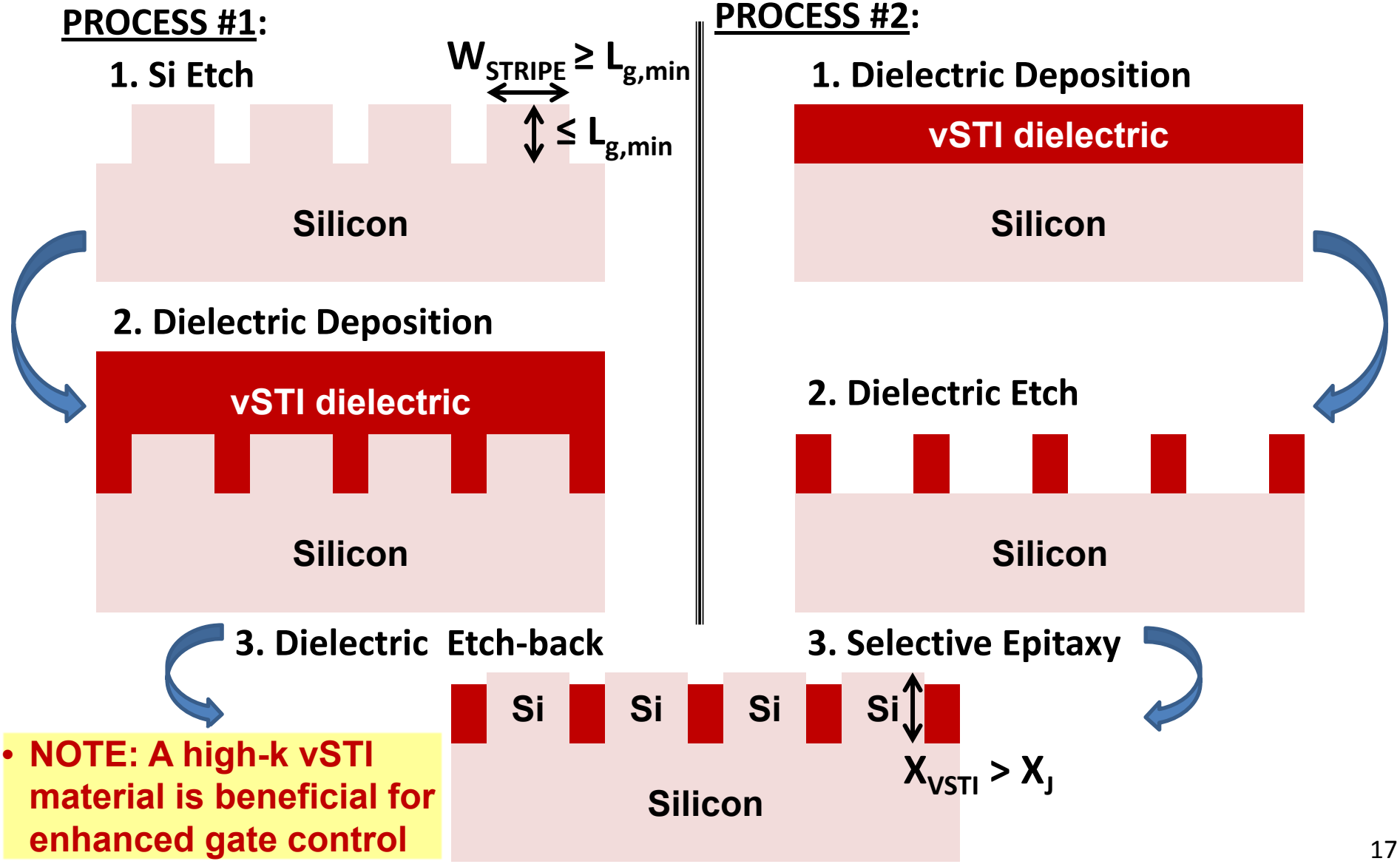
✓ **Precise control of channel width is achieved**

(Layout dependencies, sensitivity to misalignment are reduced)

→ **variation in MOSFET performance is reduced**

Corrugated Substrate Fabrication

(requires 1 mask, which can be used for multiple chip designs)



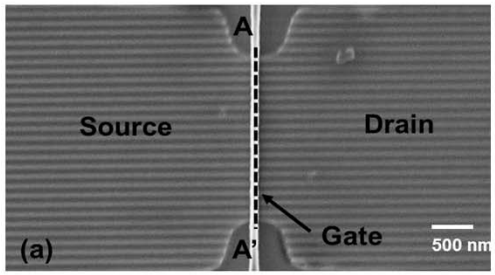
- **NOTE: A high-k vSTI material is beneficial for enhanced gate control**

1st Demonstration of (N-channel) SegFET

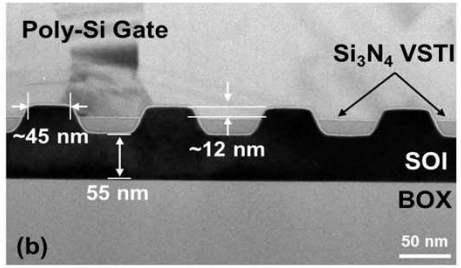
B. Ho *et al., International Semiconductor Device Research Conference* 2012

(Corrugated Substrate Process #1)

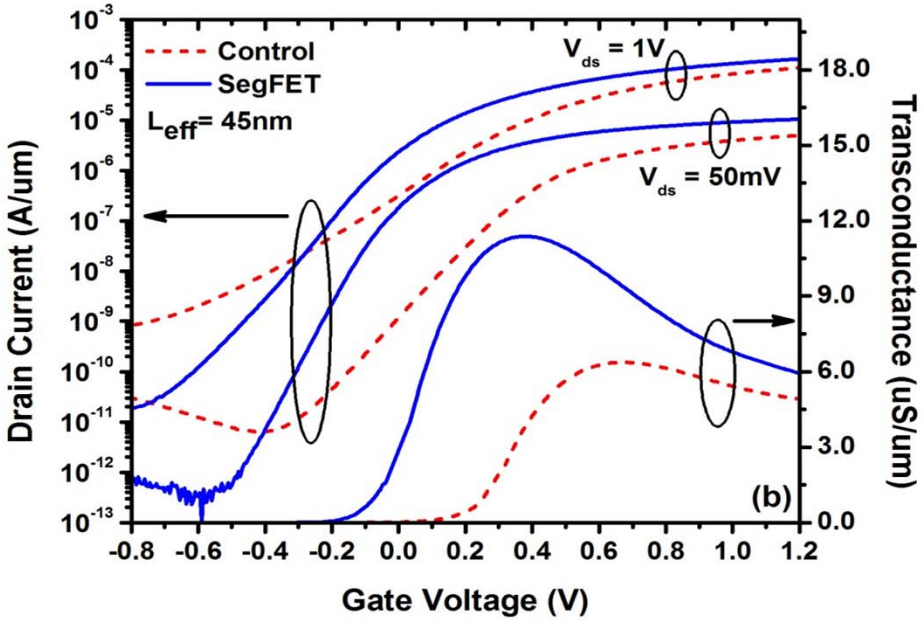
Plan-View SEM Image



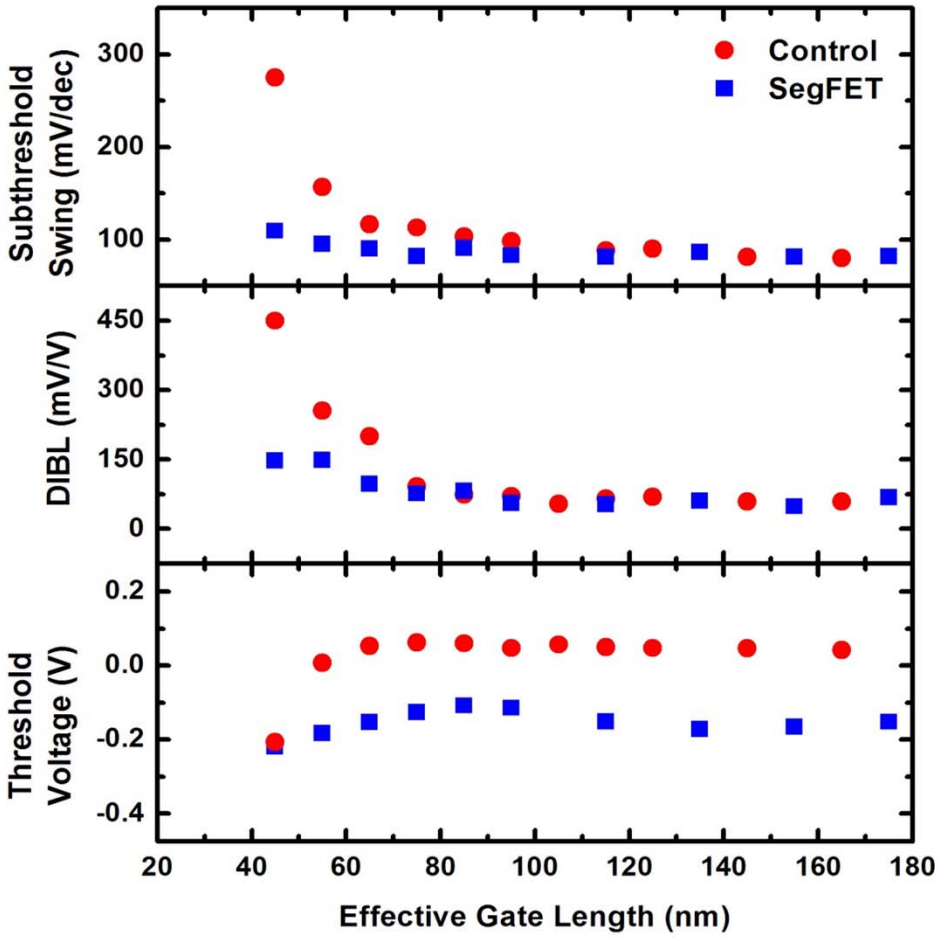
XTEM along A-A'



Measured I-V Characteristics



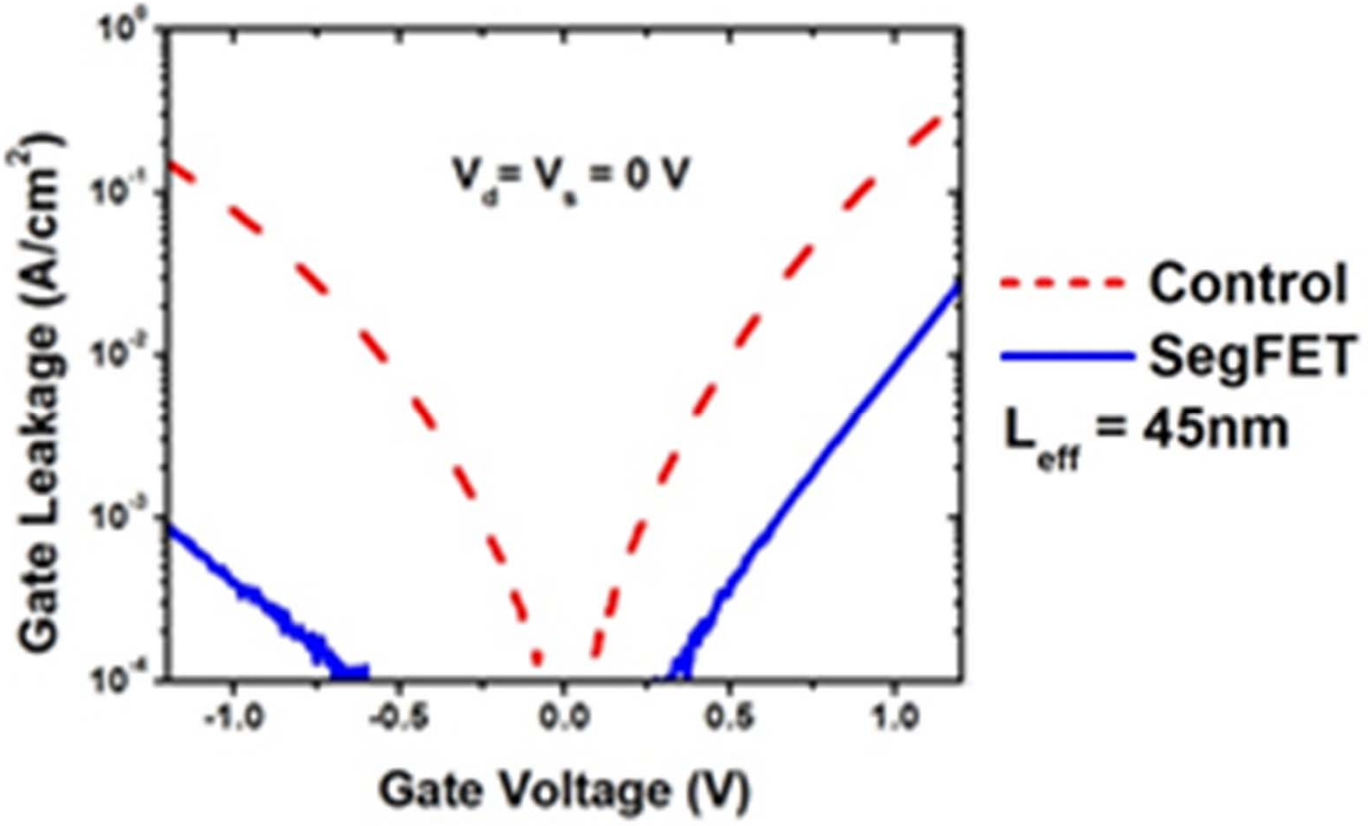
(Currents are normalized to layout width)



- **SegFETs have reduced SCE and comparable area efficiency as conventional planar MOSFETs.**

N-Channel FET Gate Leakage

B. Ho *et al., International Semiconductor Device Research Conference* 2012



- SegFET has lower gate leakage due to reduced transverse E-field

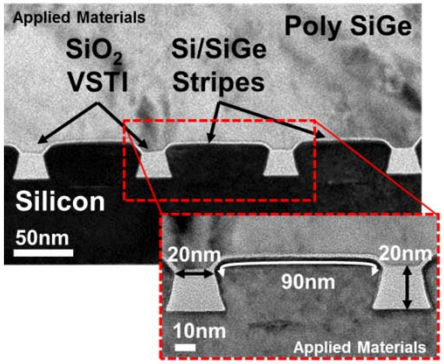
→ Allows for more aggressive EOT scaling for improved scalability

$Si_{1-x}Ge_x$ P-Channel SegFET

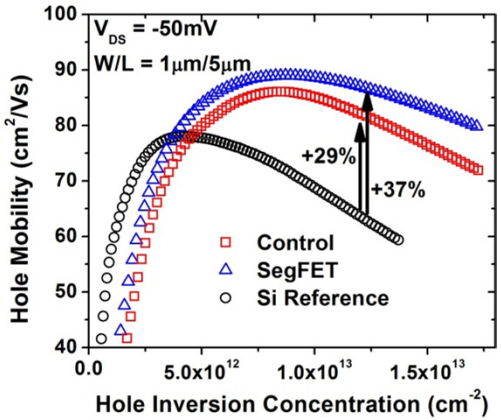
B. Ho *et al., Symp. VLSI Technology* 2012

(Corrugated Substrate Process #2)

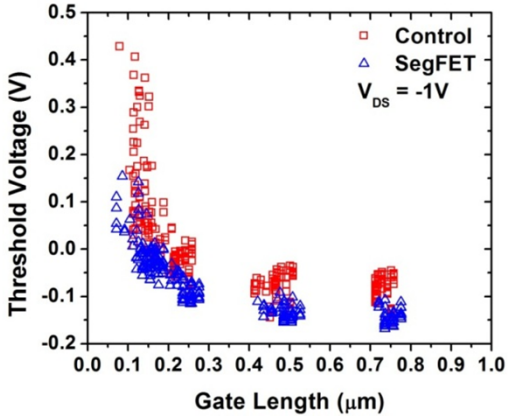
XTEM along Gate



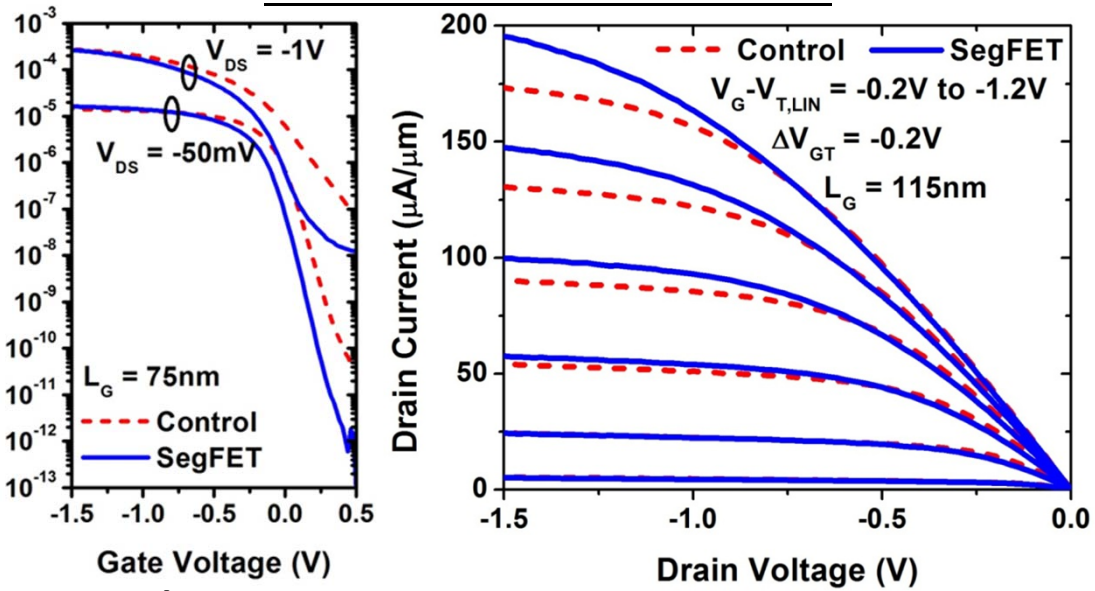
Hole Mobility



Short Channel Effect



Measured I-V Characteristics



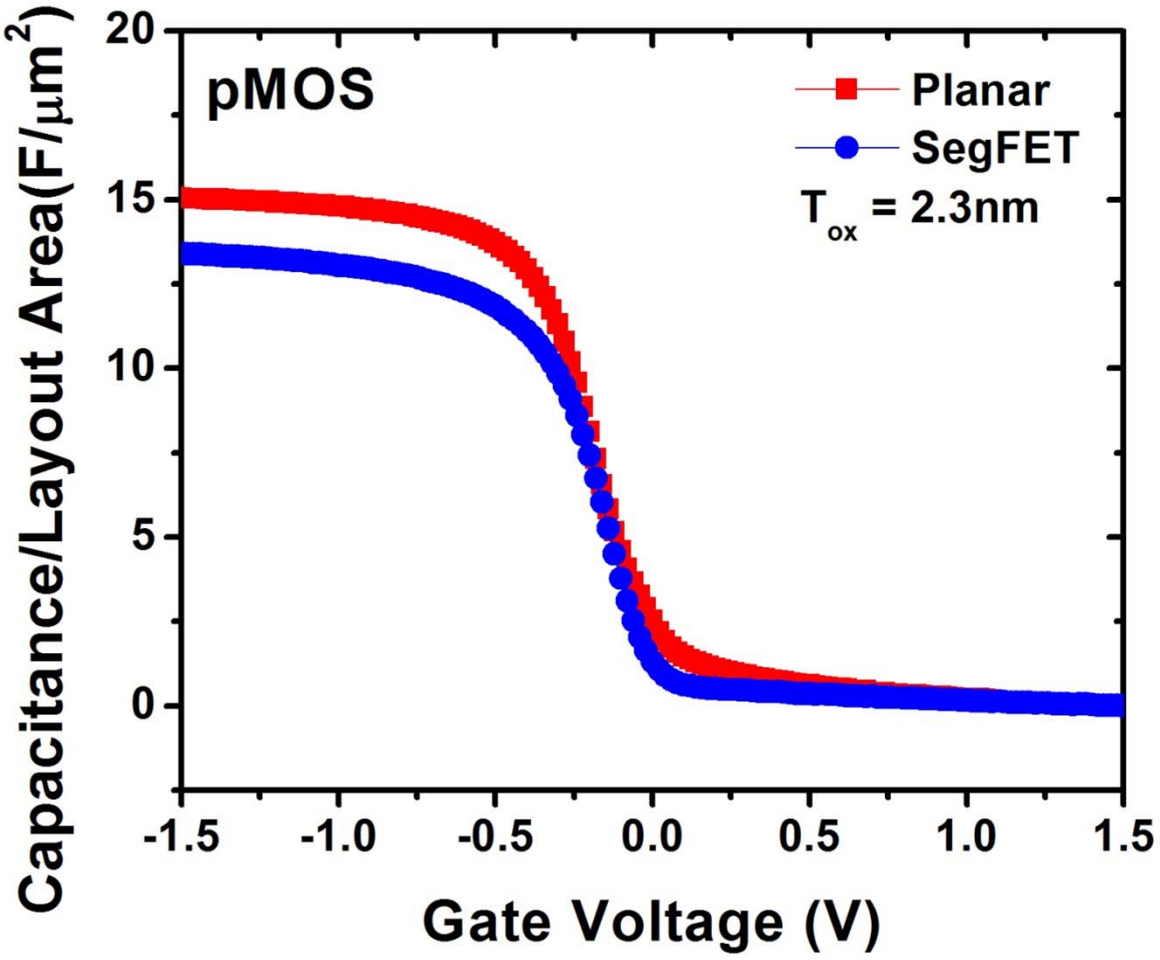
(Currents are normalized to layout width)

The SegFET exhibits

- **higher linear V_{TH}** (due to reduced biaxial strain)
- **larger drive current per unit layout width**

P-Channel FET Gate Capacitance

B. Ho *et al.,* to be published

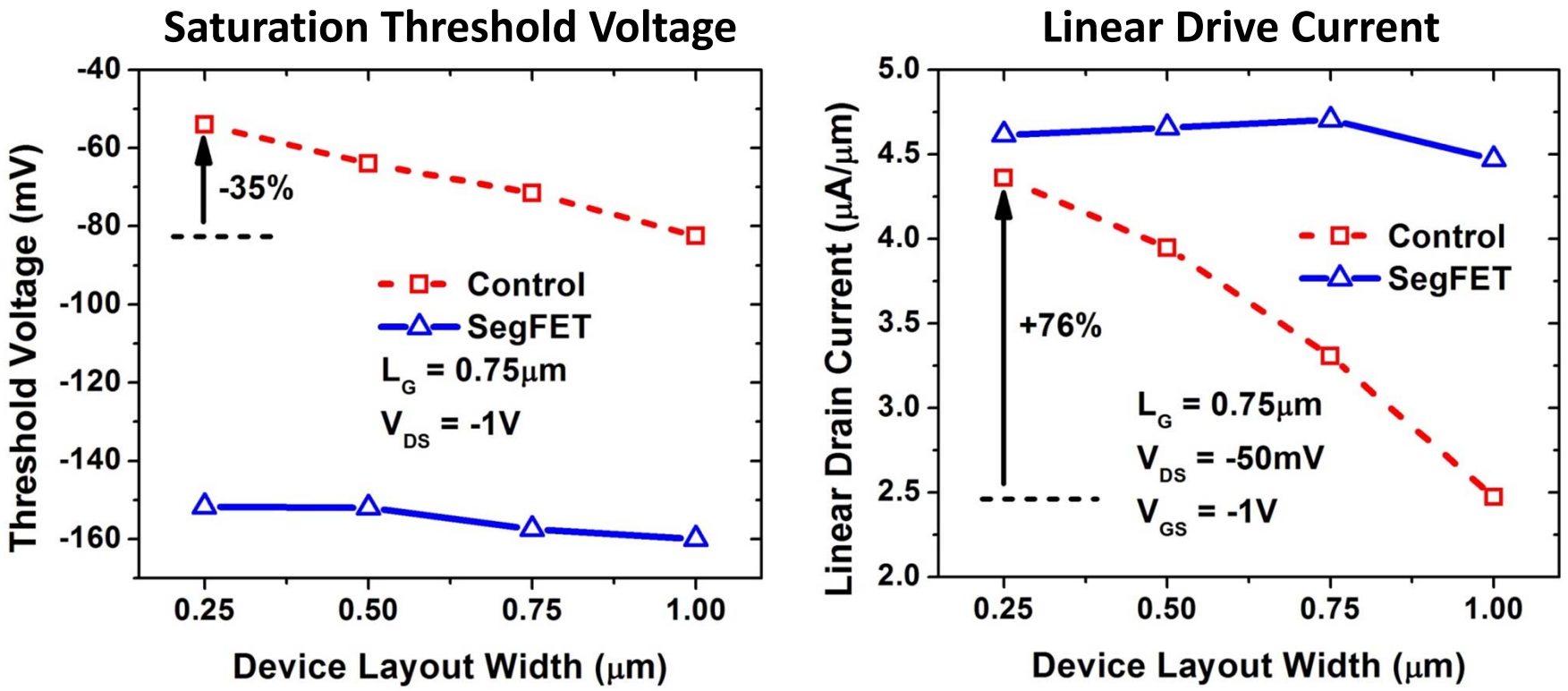


- **SegFET has lower gate capacitance per unit layout area**

→ beneficial for lower delay

P-channel FET Layout Width Dependence

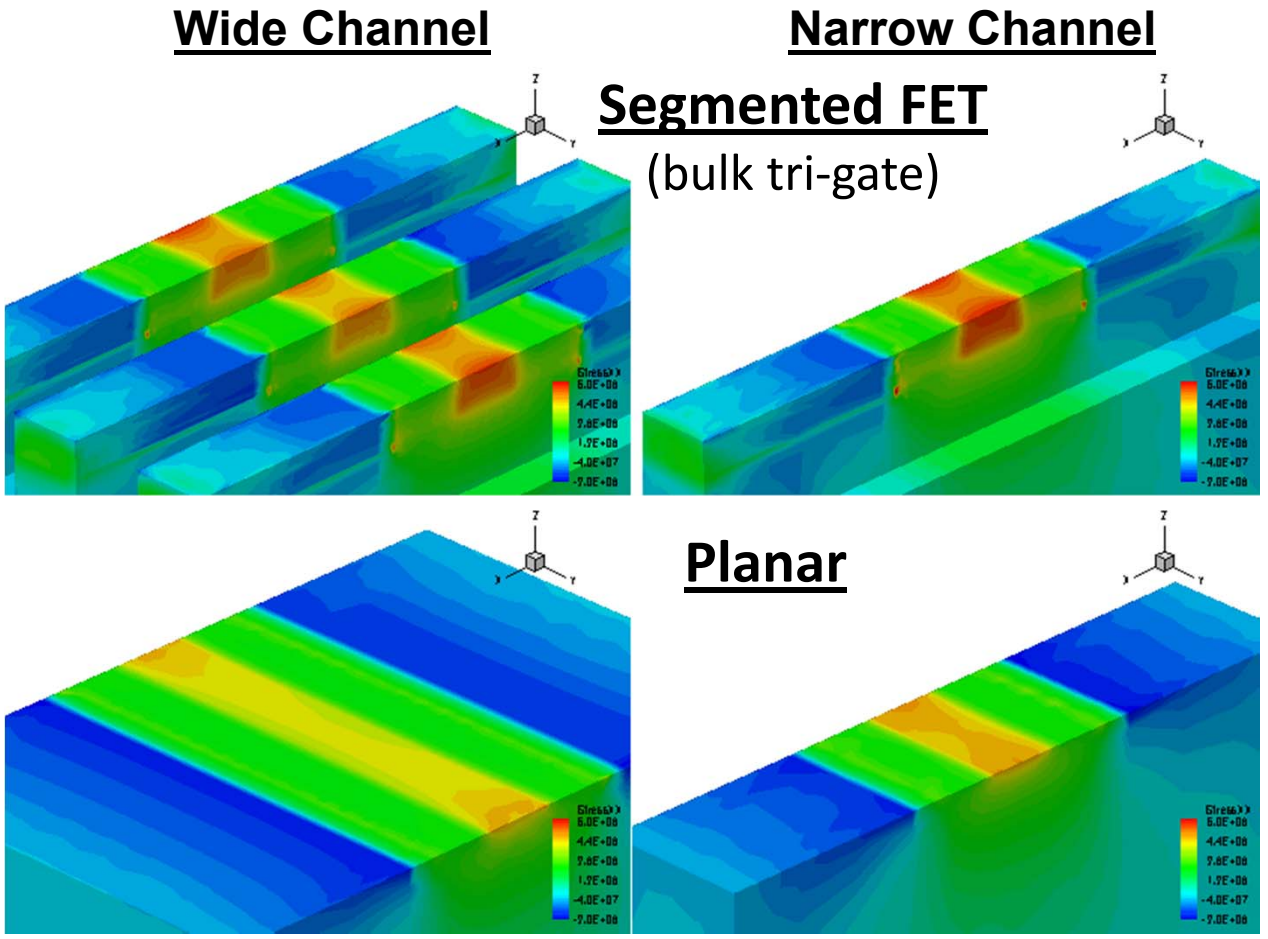
B. Ho *et al., Symp. VLSI Technology* 2012



- **SegFETs show dramatically reduced narrow width effects.**

Layout Width Dependence of Strained Si

Capping-layer-induced strain along the channel



Contact etch stop liner is assumed to be a 30nm-thick silicon nitride with 2GPa tensile stress

- SegFET parameters:
  W_{STRIPE} = 20nm
  $W_{SPACING}$ = 20nm
  H_{STRIPE} = 10nm
- L_g = 20nm
- EOT = 0.9nm
- T_{GATE} = 40nm
- L_{SPACER} = 20nm

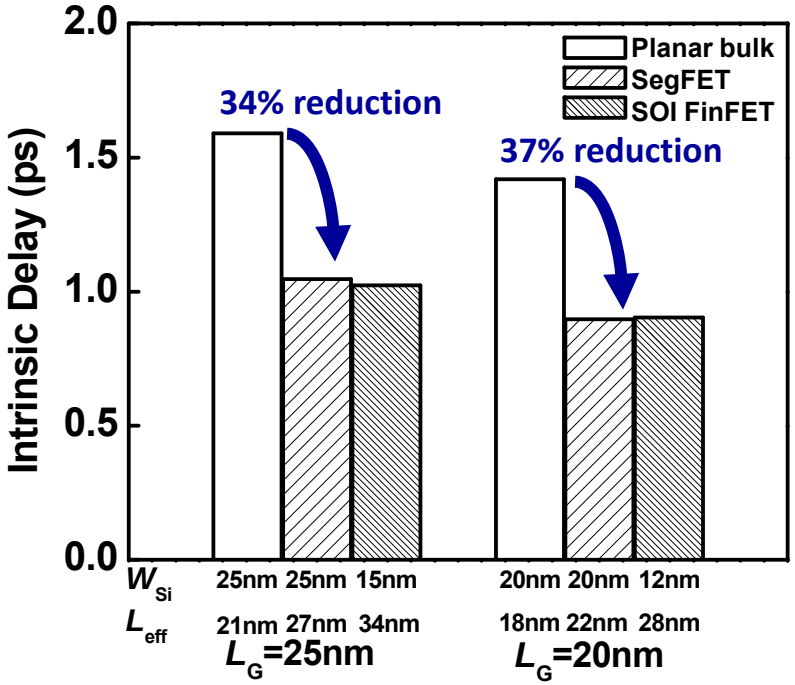
- **More stress is induced in SegFET → More mobility enhancement**
- **Reduced variation with W_{eff} for SegFET → Reduced μ_{eff} variation**

Xin Sun Ph.D. thesis, UC Berkeley, 2010

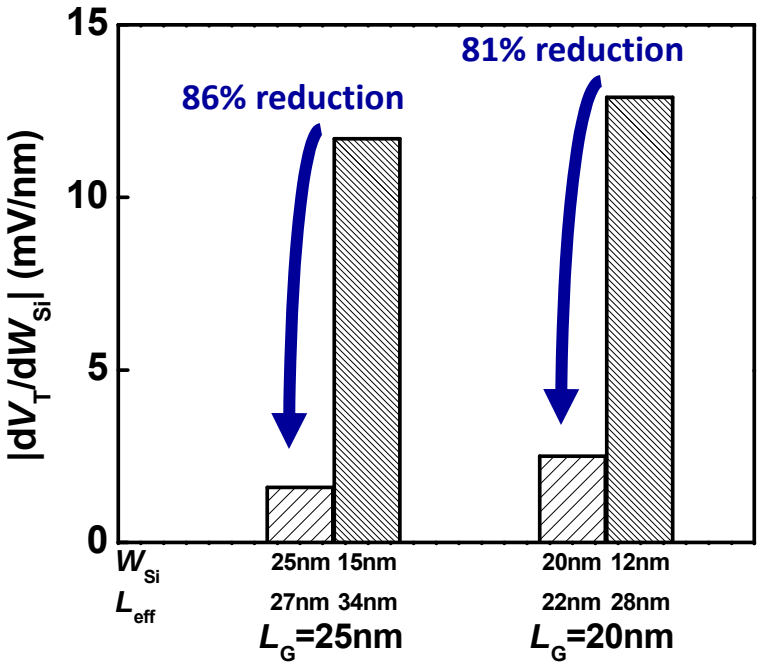
Performance Comparison with FinFET

- 3-D device simulations were performed for MOSFETs designed to achieve minimum intrinsic delay at a given I_{OFF} specification:
  - For L_G=25nm, I_{OFF}=8nA/μm
  - For L_G=20nm, I_{OFF}=18nA/μm

✓ The intrinsic delay advantage of the SegFET increases with scaling.



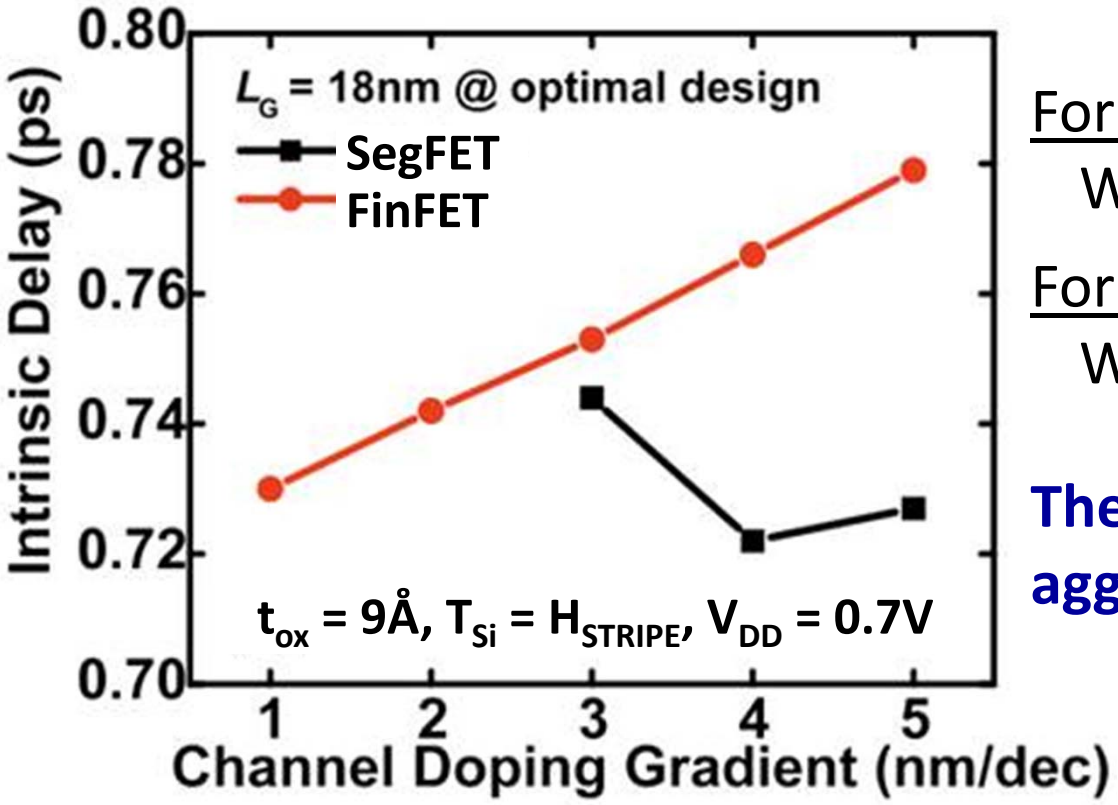
✓ The SegFET is less sensitive to W_{STRIPE} variation than the FinFET.



Xin Sun Ph.D. thesis, UC Berkeley, 2010

Impact of Retrograde Doping Steepness

X. Sun (UC Berkeley), Ph.D. thesis



For the SegFET:

$W_{STRIPE} = L_g$, $H_{STRIPE} = 0.8L_g$

For the FinFET:

$W_{STRIPE} = 0.6L_g$, $H_{STRIPE} = 1.3L_g$

The optimal steepness is less aggressive for the SegFET!

- **For the SegFET, there is a trade-off between improved average carrier mobility and improved short-channel-effect suppression.**
- **For the FinFET, the retrograde doping gradient should be as steep as possible to maximize the average carrier mobility.**

Summary

- **Power density and variability now limit transistor scaling**
  - **Thin-body MOSFET solutions are *revolutionary*, introducing new challenges for design and/or manufacturing**
- **The segmented-channel bulk MOSFET design offers an *evolutionary* (low-cost) pathway to lower σ_{VTH} and V_{DD}**
  - **utilizes conventional (established) IC fabrication techniques**
  - **is compatible with all technologies** (strained-Si, high-k/metal gate stack, advanced doping/anneal) **developed for bulk CMOS**
  - **is easily implemented alongside conventional bulk MOSFETs**
- **The benefits of SegFET technology**
  - **lower power / higher performance; improved yield / lower cost**

will only increase with CMOS technology scaling.

Corrugated Substrate Technology

Process steps required to form a (partially) corrugated substrate:

- **Masked etch** (of Si or vSTI dielectric)
  - **Regular line/space pattern + low-aspect-ratio features**
    → **amenable to spacer lithography to achieve very fine pitch**
  - **Mask can generic, *i.e.* used for multiple chip designs**
- **vSTI dielectric deposition**

  which can be high-k material (different than STI) for improved gate control
- **Etchback** (of VSTI dielectric) **or selective epitaxy** (of channel)
  - **Epitaxial growth of Ge or III-V directly on Si is facilitated by confinement**

Benefits of Corrugated Substrate approach *vs*. STI-only approach:

- ✓**Superior CD control**
- ✓**Lower parasitic resistance** (due to non-segmented source/drain)
- ✓**Higher stress transfer from embedded source/drain stressors**

→ Superior performance and yield!

Broadening the Roadmap

B. Ho (UC Berkeley), Ph.D. thesis

	Manufacturable solutions exist		Manufacturable solutions are known		Manufacturable solutions are NOT known

High Performance (HP) Logic Technology Requirements

Year	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
Physical L_G (nm)	18	17	15.3	14	12.8	11.7	10.6	9.7	8.9	8.1	7.4	6.6	5.9
V_{DD} (V)	0.82	0.8	0.77	0.75	0.73	0.71	0.68	0.66	0.64	0.62	0.61	0.59	0.57
Equivalent Oxide Thickness (nm)													
Planar	0.73												
SegFET	0.86	0.8	0.76	0.72	0.68	0.65	0.62	0.59	0.56	0.53	0.5	0.47	0.45
FinFET		0.8	0.76	0.72	0.68	0.65	0.62	0.59	0.56	0.53	0.5	0.47	0.45
Stripe width (nm)													
SegFET	18	17	15.3	14	12.8	11.7							
FinFET		11.3	10.3	9.4	8.5	7.7	7	6.3	5.7	5.2	4.7	4.2	3.7
Junction Depth (nm)													
Planar	7.2												
SegFET	12.6	11.9	10.7	9.8	9.3	8.8	8.2	7.76	7.1	6.5	5.9	5.3	4.7

Extend known solutions by 4 yrs

Extend known solutions by >7 years

Extend known solutions by 8 years

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  - **Soitec** (B.-Y. Nguyen, O. Bonnin, C. Mazure)

Additional Information

SegFET at a Glance

- **SegFET is a proven transistor design in which the channel region of a planar bulk MOSFET is segmented to improve gate control.**
  - **Conventional CMOS fabrication process, w/ corrugated starting substrate**

  Not a FinFET: nearly planar, *i.e.* no high-aspect-ratio features
  - **Leverages retrograde channel doping to suppress leakage**
  - **V_T can be tuned via body biasing**
- **The combination of retrograde channel doping and a "tri-gate" structure provides for superior electrostatic integrity.**
  - **More scalable than FinFET, Intel's tri-gate FET, and gate-all-around FET**

→ **Easiest approach to extend transistor scaling to sub-10 nm L_g and/or to adopt new channel materials**
  - **Requires no process-tool changes or new materials**
  - **Requires one additional mask – which can be reused**
  - **Uses standard bulk MOSFET compact model and EDA tools**

Proof of Concept: Recessed Isolation Oxide

C. Shin *et al., 2010 ESSDERC*

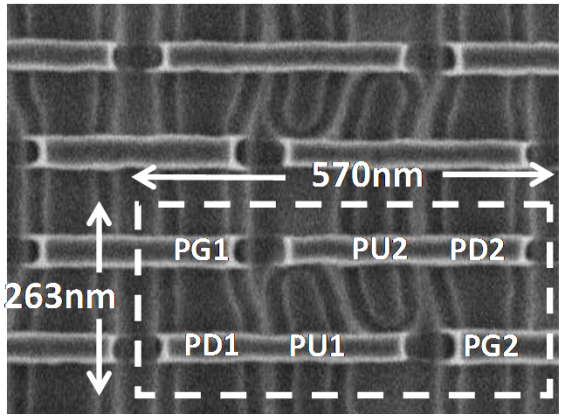
Experiment performed at UMC in early 28nm CMOS technology

- **Individual logic transistors and 6T-SRAM arrays fabricated**
  - **~2500 cell per device-under-test (DUT)**
  - **Dual-stress liners for performance enhancement**

CMOS front-end-of-line steps

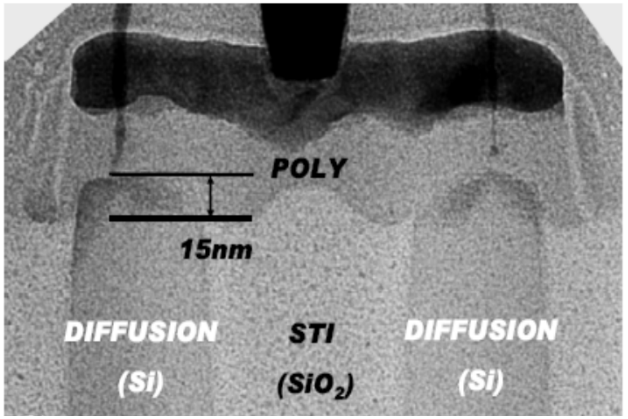
- STI Formation
- Well & V_T Implants
- ***STI Oxide Recess*** **0 or 15nm**
- Gate Ox./Poly Deposition
- Gate Patterning
- LDD & Pocket Implants
- Spacer & S/D Formation
- Activation Process
- Salicidation

SRAM cell plan-view SEM



cell-area = 0.149 um^2

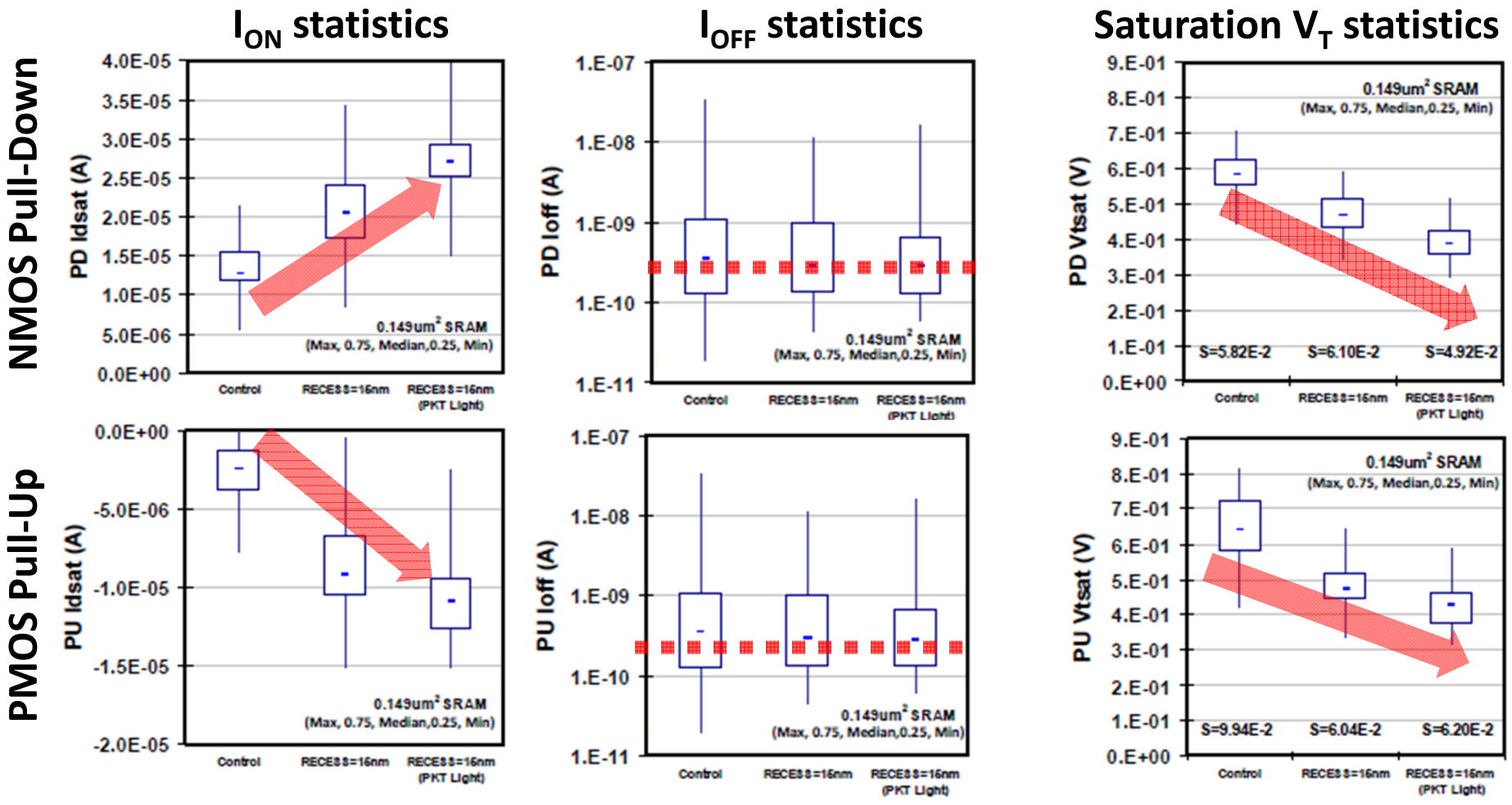
XTEM along gate electrode



PKT dose split: Standard or Light

Measured Quasi-Planar CMOS Results

C. Shin *et al.*, *2010 ESSDERC*



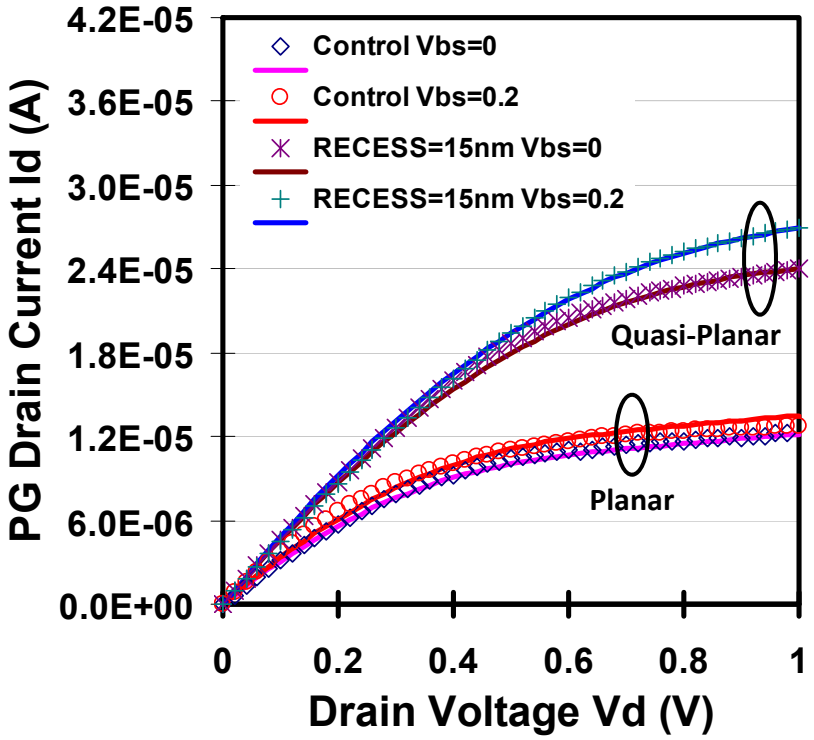
- Quasi-planar I_{ON} is higher, for comparable I_{OFF}
  - 2x increase for NMOS, 4x increase for PMOS
- Quasi-planar V_{TH} variation is lower

Body Bias Effect and Compact Model

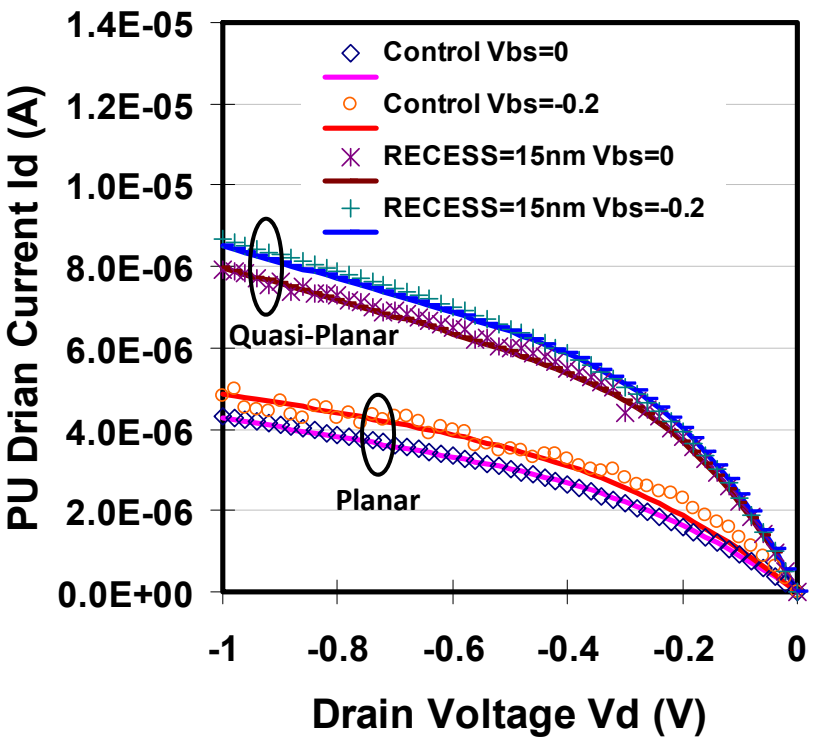
C. Shin *et al.*, *2010 ESSDERC*

- **The standard bulk MOSFET compact model can well predict quasi-planar MOSFET performance, including the body effect.**

NMOS



PMOS



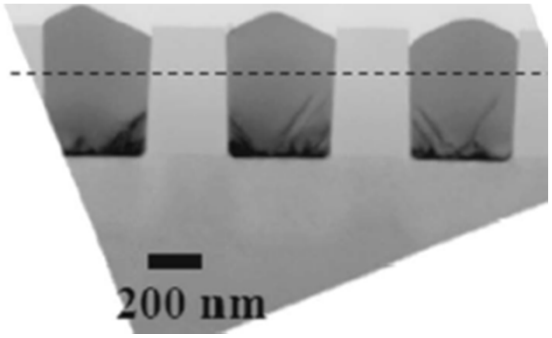
Advanced Channel Materials

- **High-mobility semiconductor materials potentially can provide for improved performance:**
  - **Ge for PMOS**
  - **(In)GaAs for NMOS**

	Si	Ge	GaAs
Electron mobility (cm^2/Vs)	1500	3900	8500
Hole mobility (cm^2/Vs)	450	1900	400
Lattice constant (Å)	5.431	5.646	5.653
Band gap (eV)	1.12	0.66	1.424
Dielectric constant	12	16	13

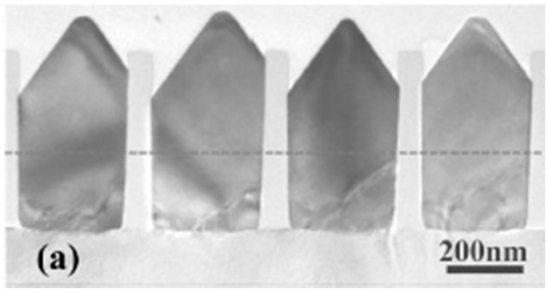
- **Selective epitaxial growth directly on Si is facilitated by the use of a corrugated substrate:**

Ge on Si



J.-S. Park *et al.*, *Appl. Phys. Lett.* 90 052113, 2007

GaAs on Si



J. Z. Li *et al.*, *Appl. Phys. Lett.* 91 021114, 2007