14 nm chip X-SEM from www.intel.com/content/dam/www/public/us/en/documents/pdf/foundry/mark-bohr-2014-idf-presentation.pdf

Extending the Era of Moore's Law

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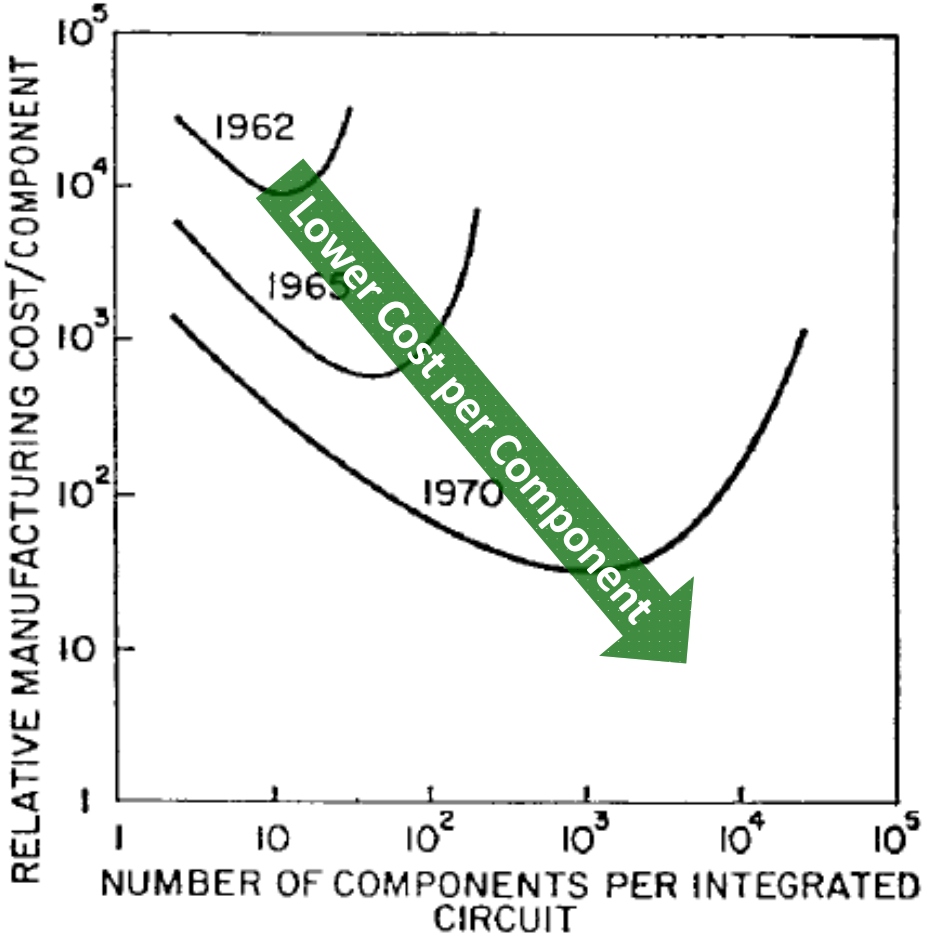
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley

September 11, 2017

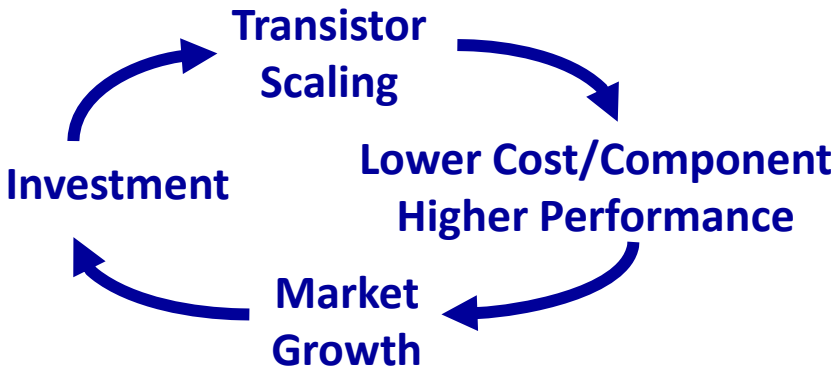
SPIE Photomask Technology + EUV Lithography Conference

IC Technology Advancement

Gordon E. Moore, "Cramming more Components onto Integrated Circuits," *Electronics*, pp. 114-117, April 1965



- **The minimum cost point moves to a larger number of components per IC over time, with advancements in manufacturing technology.**

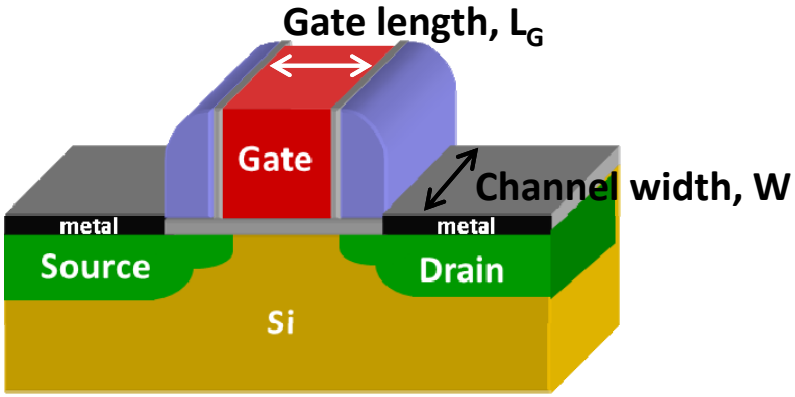


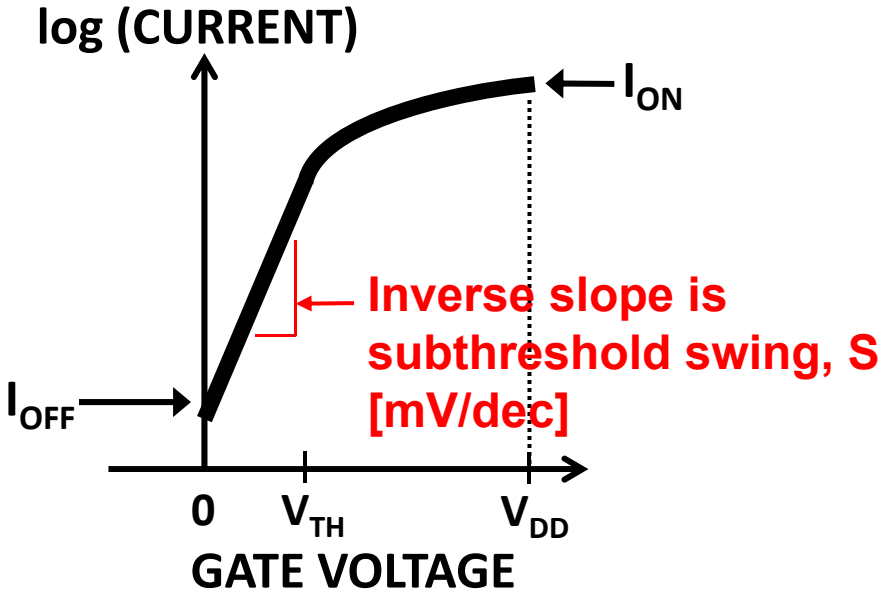
Outline

- **Transistor Scaling to the Limit**
- **Extending the Era of Moore's Law**
- **Summary**

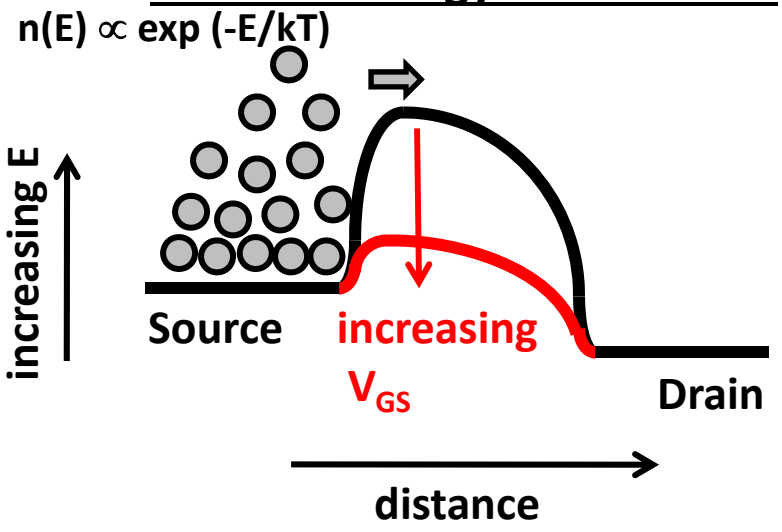
Transistor Basics

Metal-Oxide-Semiconductor (MOS) Field-Effect Transistor (FET)





Electron Energy Band Profile



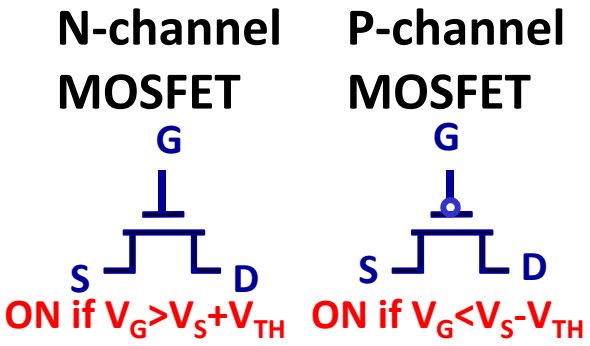
$$\nu \propto \mu_{eff}$$

$$I_D = W \cdot \nu \cdot Q_{inv}$$

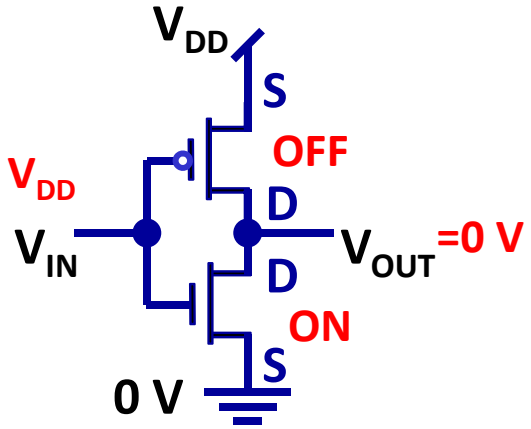
$$Q_{inv} \propto C_{ox}(V_{GS} - V_{TH})^{\eta}$$

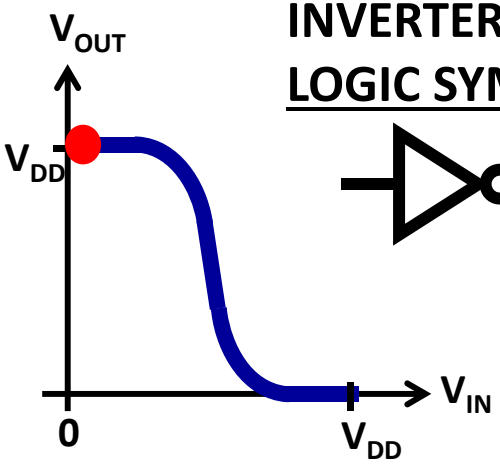
Complementary MOS Devices & Circuits

CIRCUIT SYMBOLS



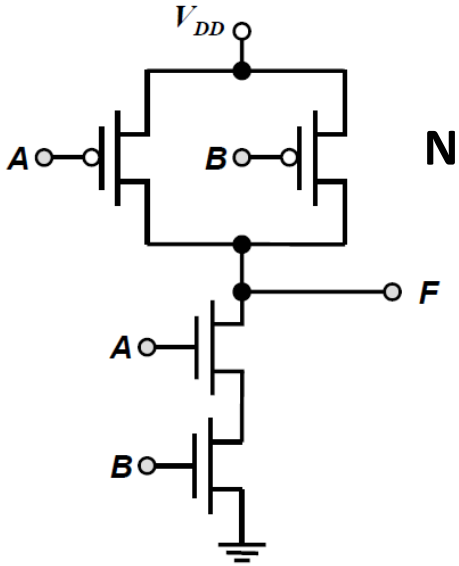
CMOS INVERTER CIRCUIT





INVERTER LOGIC SYMBOL

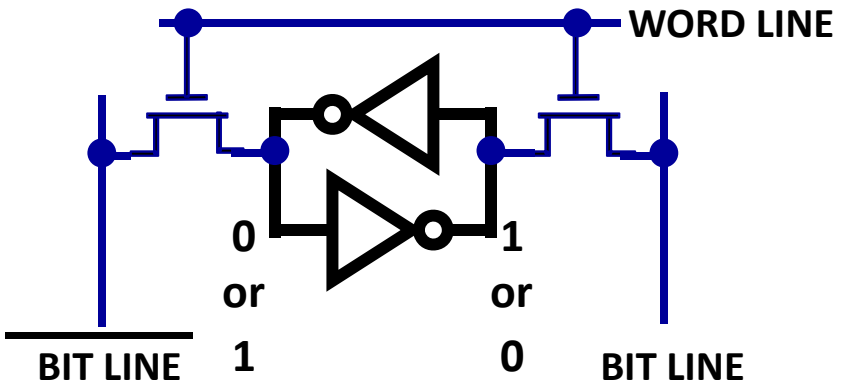
CMOS NAND GATE



NOT AND (NAND) TRUTH TABLE

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

STATIC MEMORY (SRAM) CELL

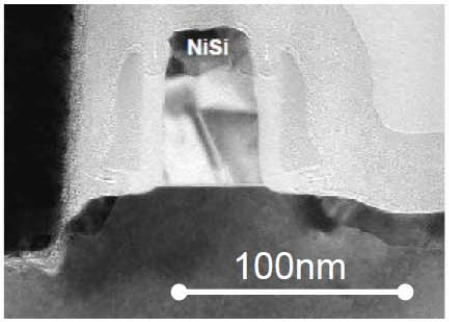


CMOS Technology Scaling

XTEM images with the same scale

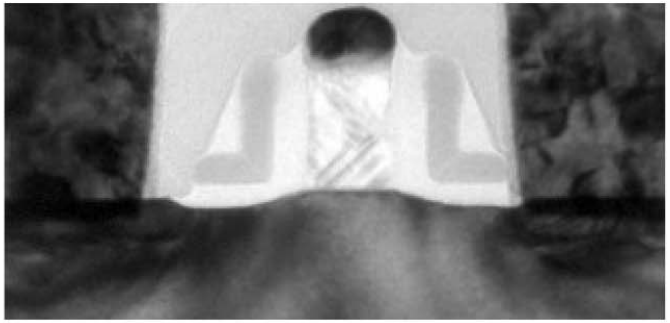
courtesy V. Moroz (Synopsys, Inc.)

90 nm node



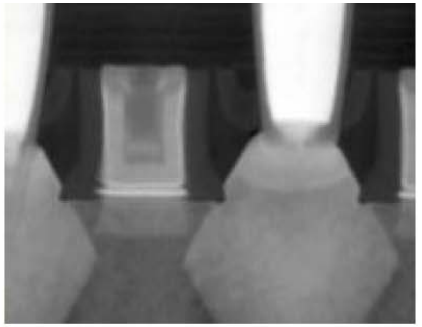
T. Ghani *et al.*, *IEDM* 2003

65 nm node



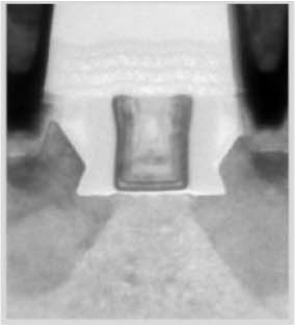
(after S. Tyagi *et al.*, *IEDM* 2005)

45 nm node



K. Mistry *et al.*, *IEDM* 2007

32 nm node

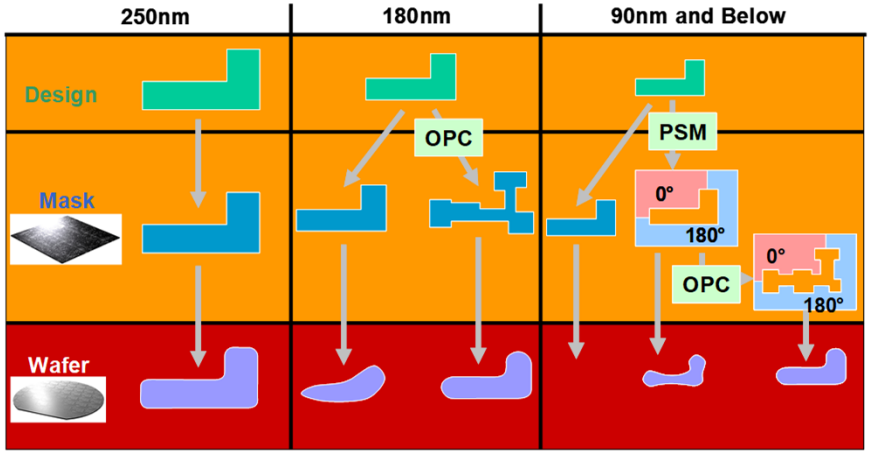


P. Packan *et al.*, *IEDM* 2009

strained Si → μ_{eff}↑

high-k/metal gate → C_{ox}↑

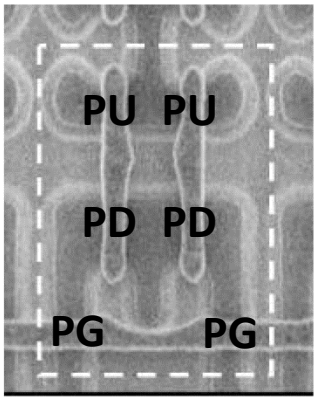
Design for Manufacturing



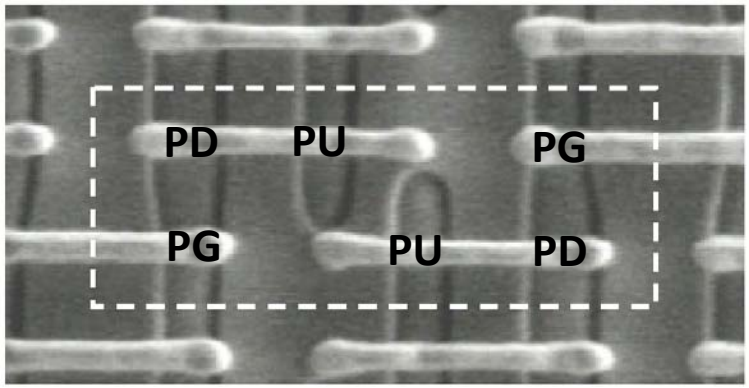
courtesy Mike Rieger (Synopsys, Inc.)

SRAM bit-cell layouts

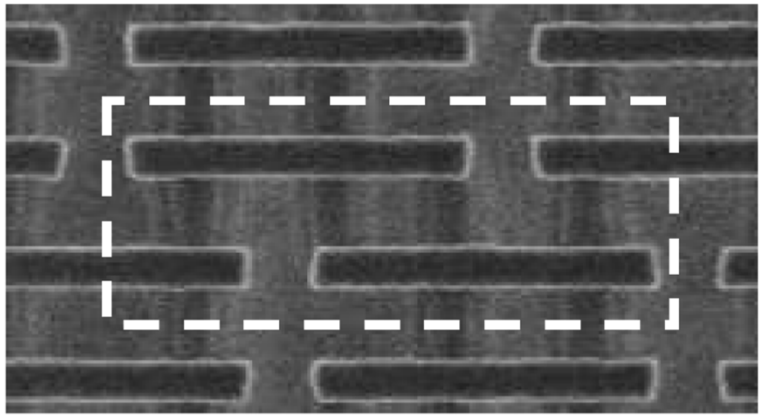
C. Webb, *Intel Technology Journal*, vol. 12, No. 2, pp. 121-130, 2008



90 nm

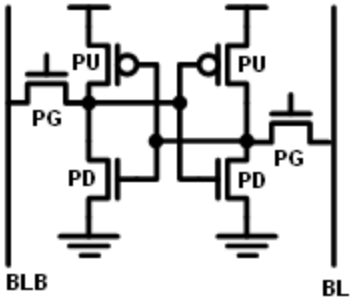


65 nm



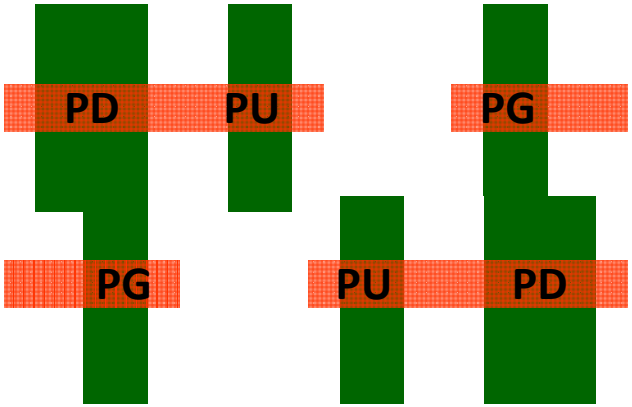
45 nm

6-T SRAM Cell

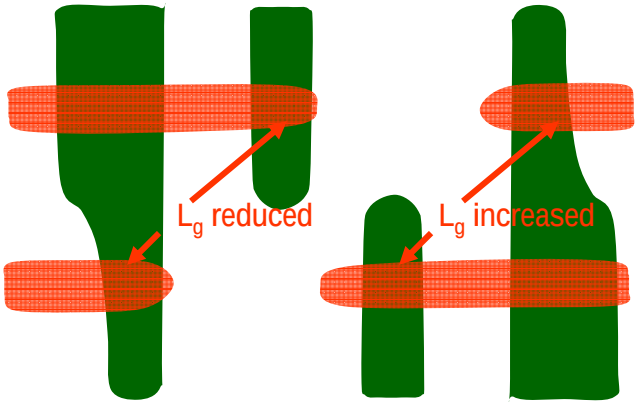


Impact of Misalignment

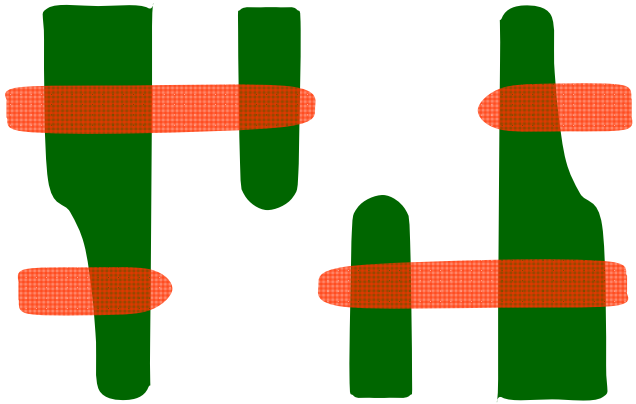
Desired layout
(6-T SRAM cell)



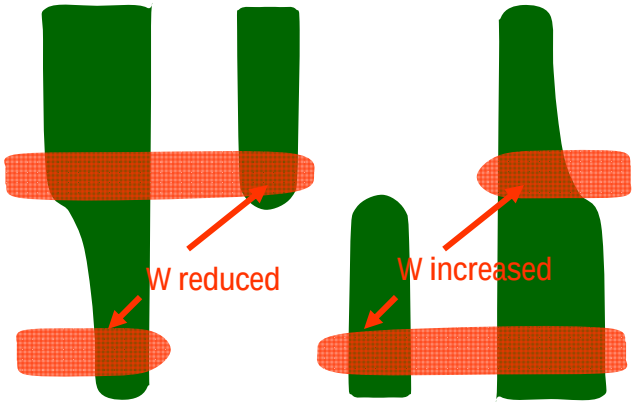
Actual layout w/ lateral misalignment
(gate length variations)



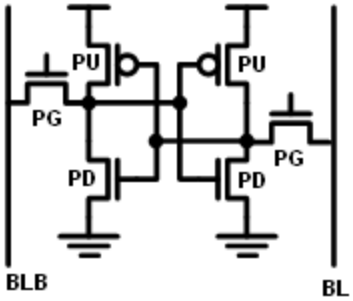
Actual layout
(corner rounding)



Actual layout w/ vertical misalignment
(channel width variations due to active jogs)

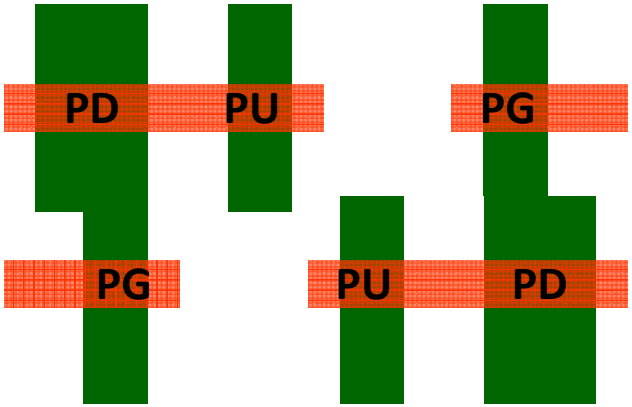


6-T SRAM Cell

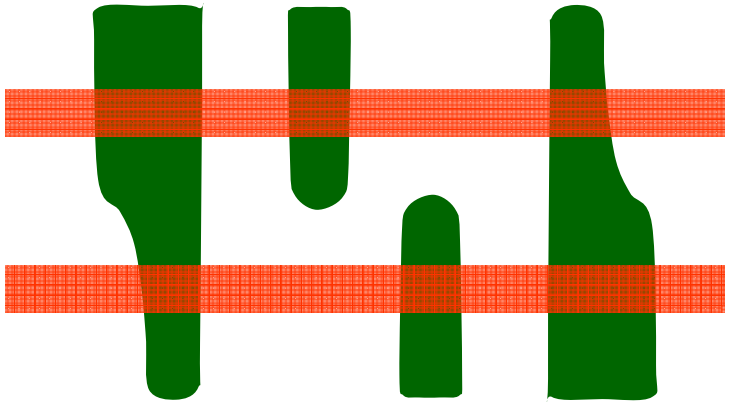


Double Patterning of Gate

Desired layout
(6-T SRAM cell)

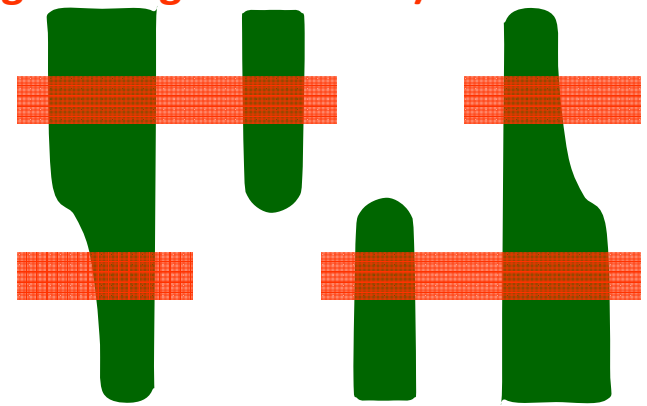


Actual layout after 1st gate patterning



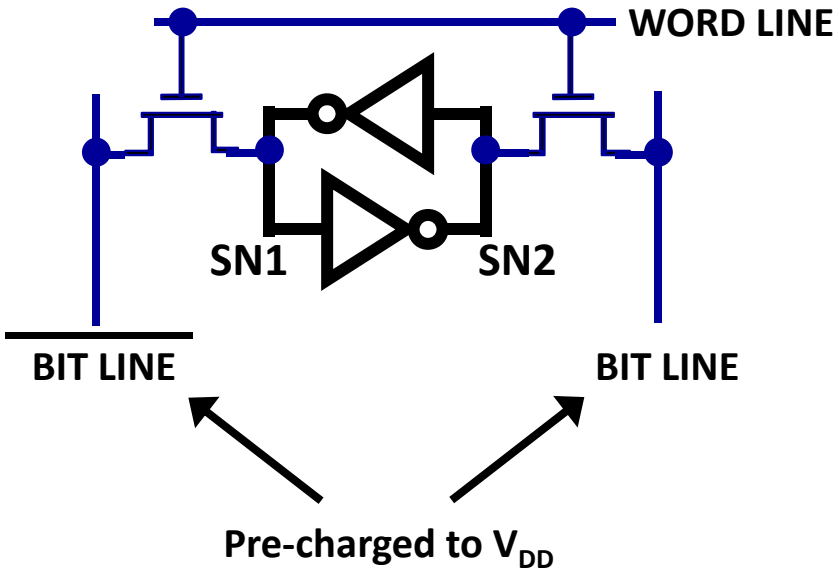
Actual layout after active patterning

Actual layout after 2nd gate patterning
(no gate length variation)

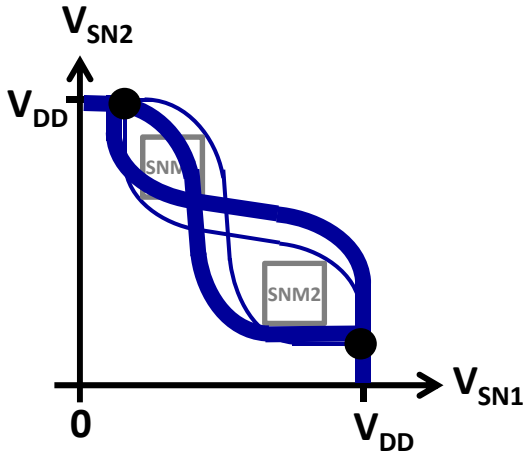


Impact of Variability on SRAM

STATIC MEMORY (SRAM) CELL



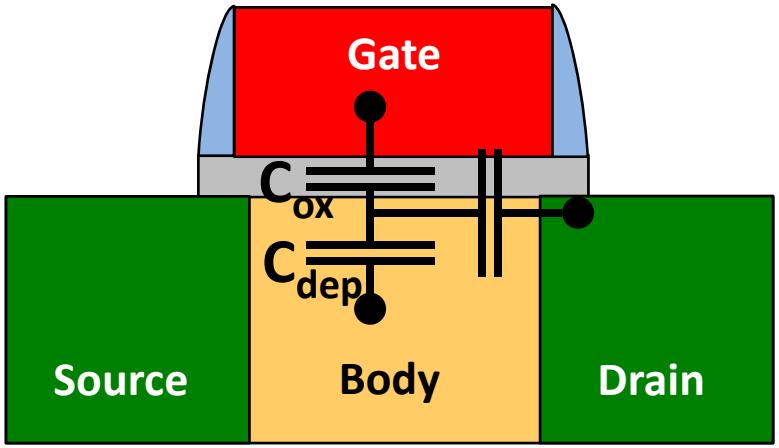
BUTTERFLY CURVES



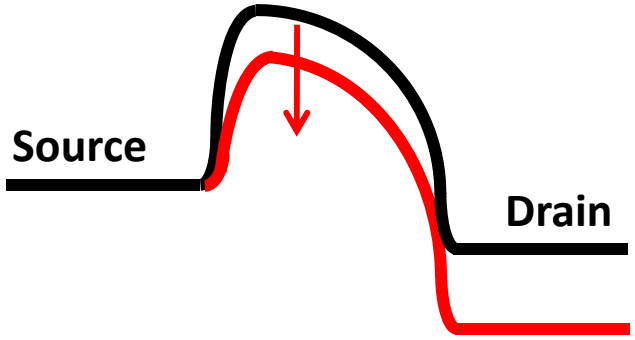
- V_{TH} mismatch results in reduced static noise margin.
  → lowers cell yield and/or limits V_{DD} scaling

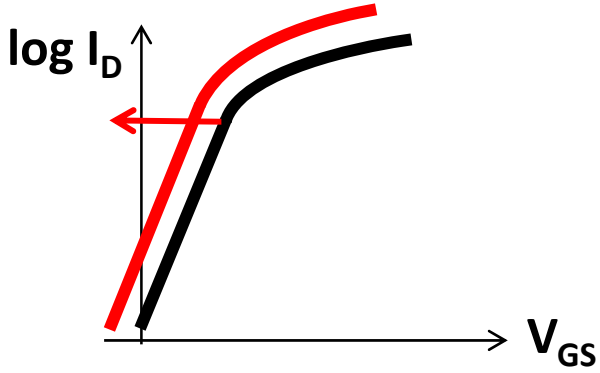
→ Immunity to short-channel effects needed!

Short-Channel Effects



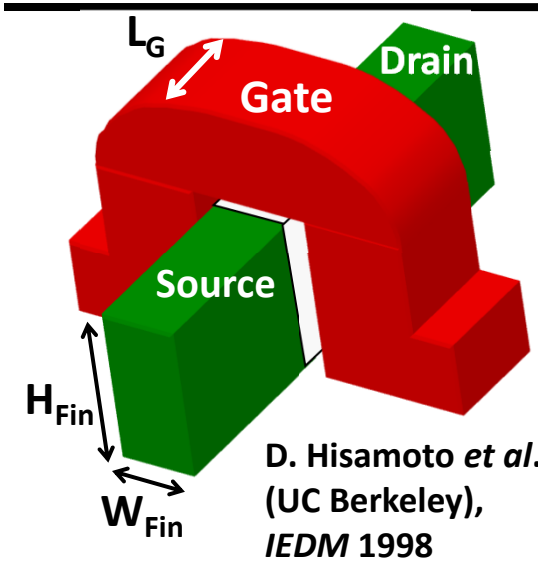
- V_{TH} decreases with decreasing L_g and with increasing V_{DS}:



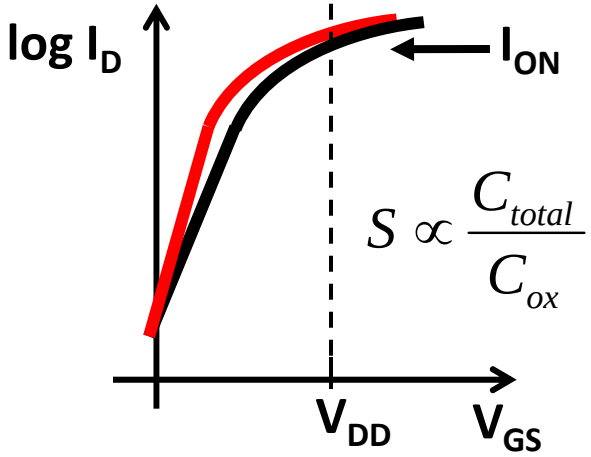


- **Increased capacitive coupling between Gate and channel provides for better Gate control, hence reduced SCE**

FinFET/Tri-Gate Transistor



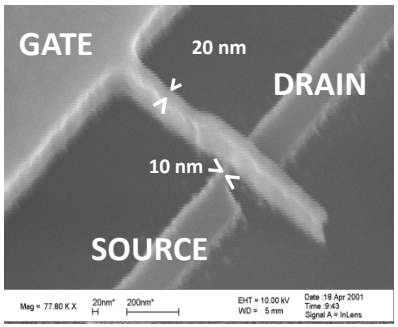
D. Hisamoto *et al.* (UC Berkeley), *IEDM* 1998



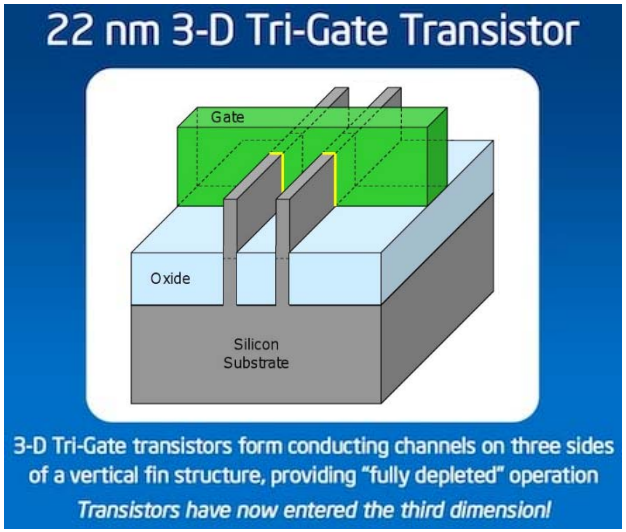
- **Superior gate control**

→higher I_{ON}/I_{OFF} or lower V_{DD}

15nm L_g FinFET



Y.-K. Choi *et al.*, (UC Berkeley) *IEDM* 2001



Intel Corp., May 2011

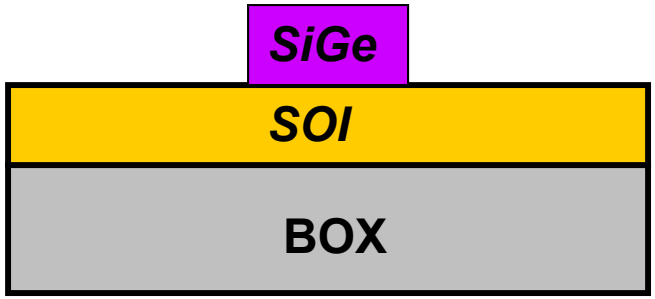
- **Multiple fins can be connected in parallel to achieve higher ON-state drive current.**

Spacer Lithography

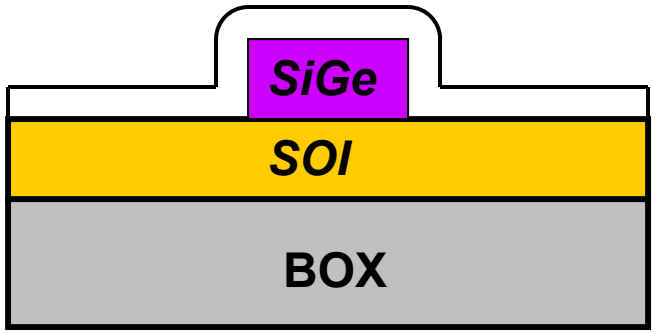
Y.-K. Choi, T.-J. King, and C. Hu, *IEEE Trans. Electron Devices*, Vol. 49, No. 3, pp. 436-441, 2002

a.k.a. Sidewall Image Transfer (SIT) and Self-Aligned Double Patterning (SADP)

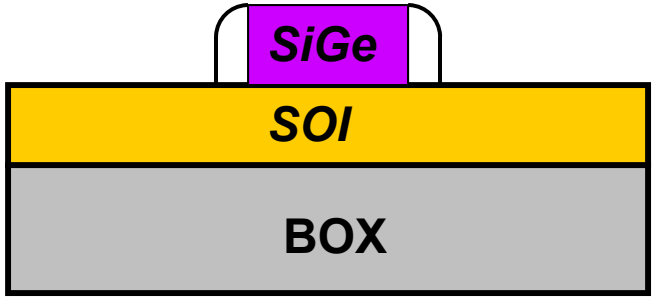
1. Deposit & pattern sacrificial layer



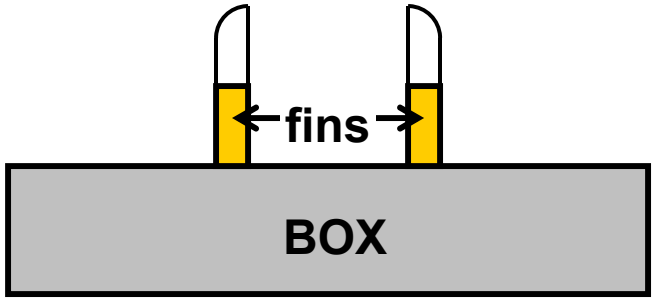
2. Deposit mask layer (SiO_2 or Si_3N_4)



3. Etch back mask layer to form "spacers"



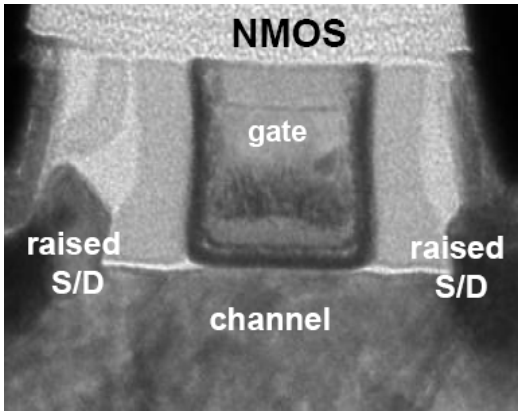
4. Remove sacrificial layer; etch SOI layer to form fins

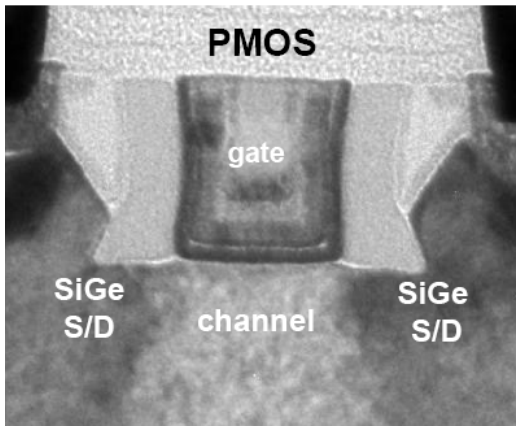


Note that fin pitch is 1/2× that of patterned layer

MOSFET Evolution

32 nm
planar

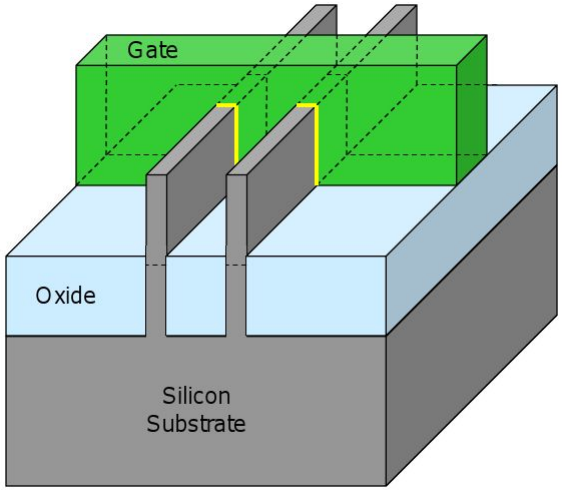




P. Packan *et al*. (Intel), *IEDM* 2009

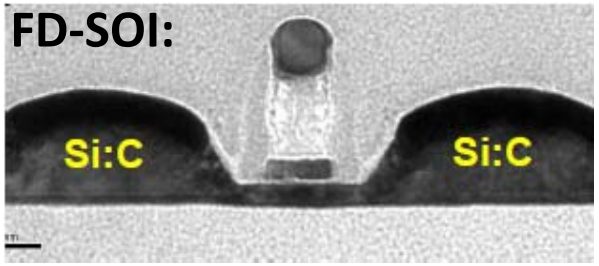
22 nm
thin body

FinFET:



Intel Corp.

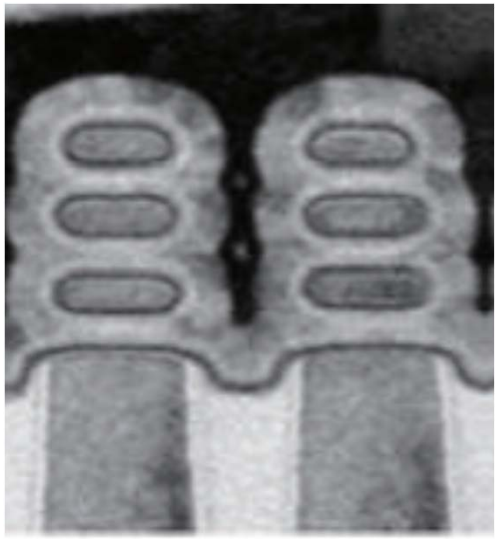
FD-SOI:



K. Cheng *et al.* (IBM), *VLSI Symp.* 2011

beyond 7 nm

Stacked nanosheets

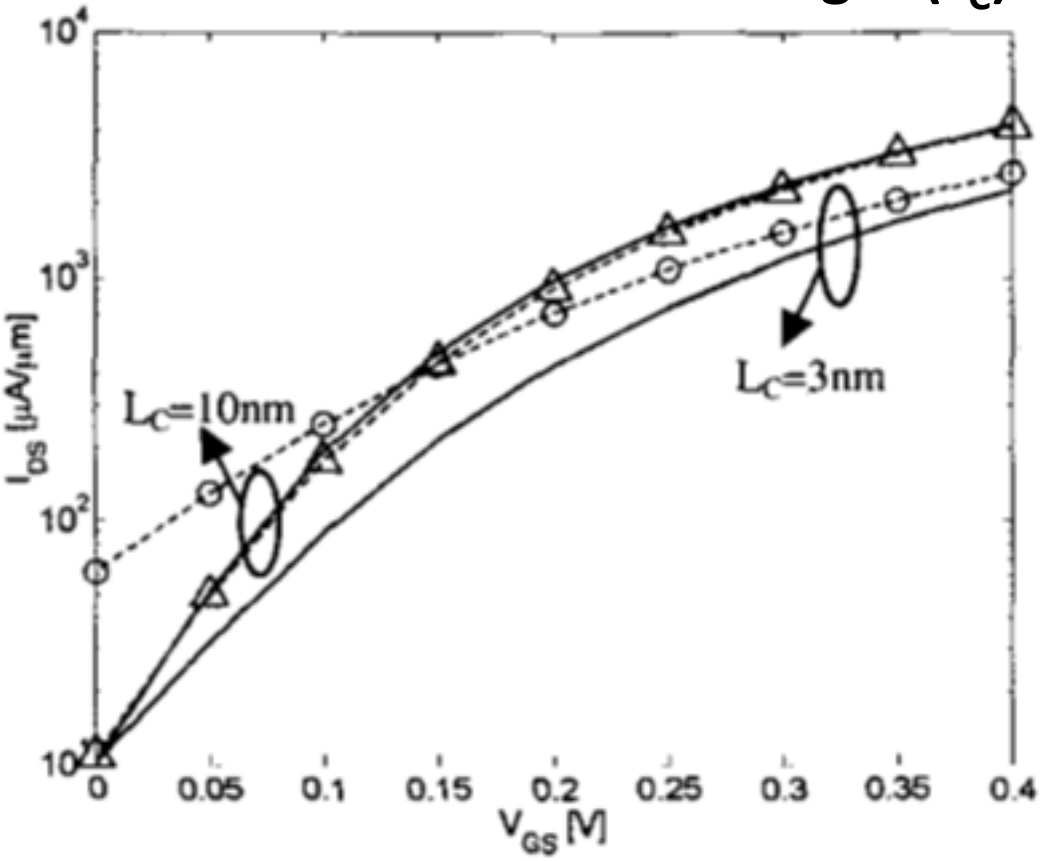


N. Loubet *et al*. (IBM, Samsung, GLOBALFOUNDRIES)
Symp. VLSI Tech 2017

Stacked gate-all-around (GAA) FETs achieve the highest layout efficiency.

Channel-Length Scaling Limit

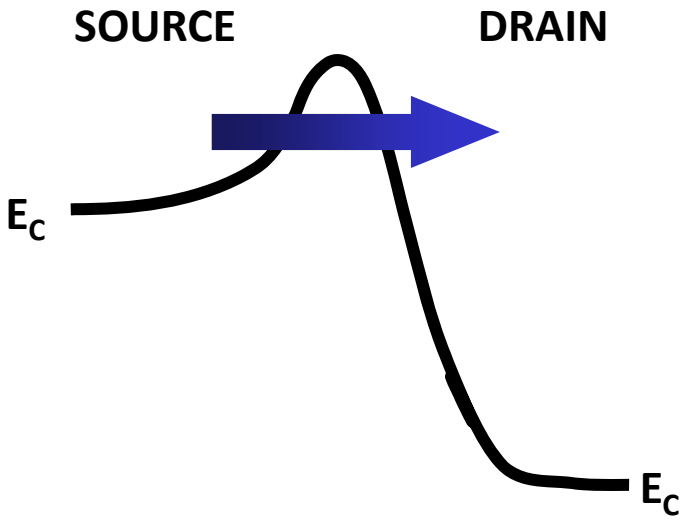
- **Quantum mechanical tunneling sets a fundamental scaling limit for the channel length (L_C).**



J. Wang *et al.*, *IEDM Technical Digest*, pp. 707-710, 2002

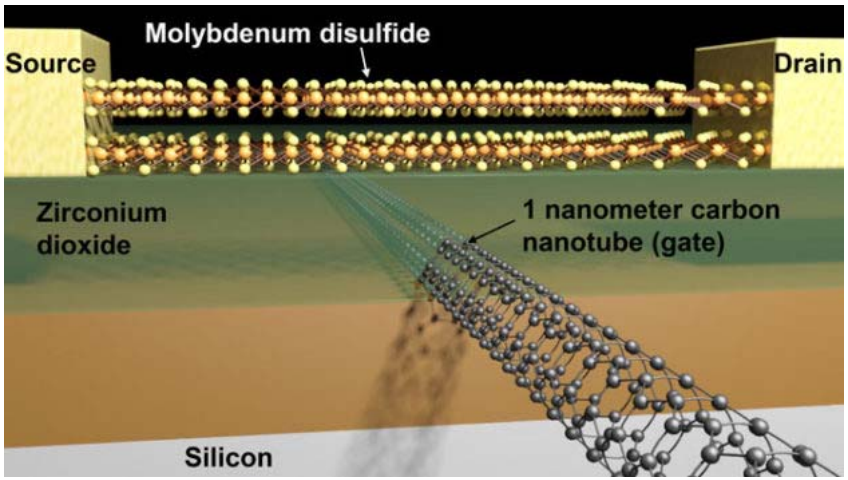
If electrons can easily tunnel through the source potential barrier, the gate cannot shut off the transistor.

nMOSFET Energy Band Diagram
(OFF state)

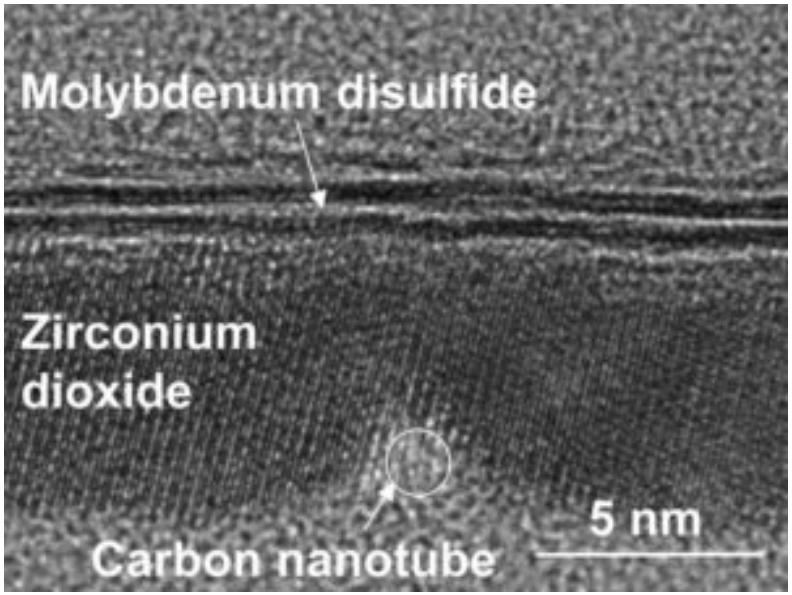


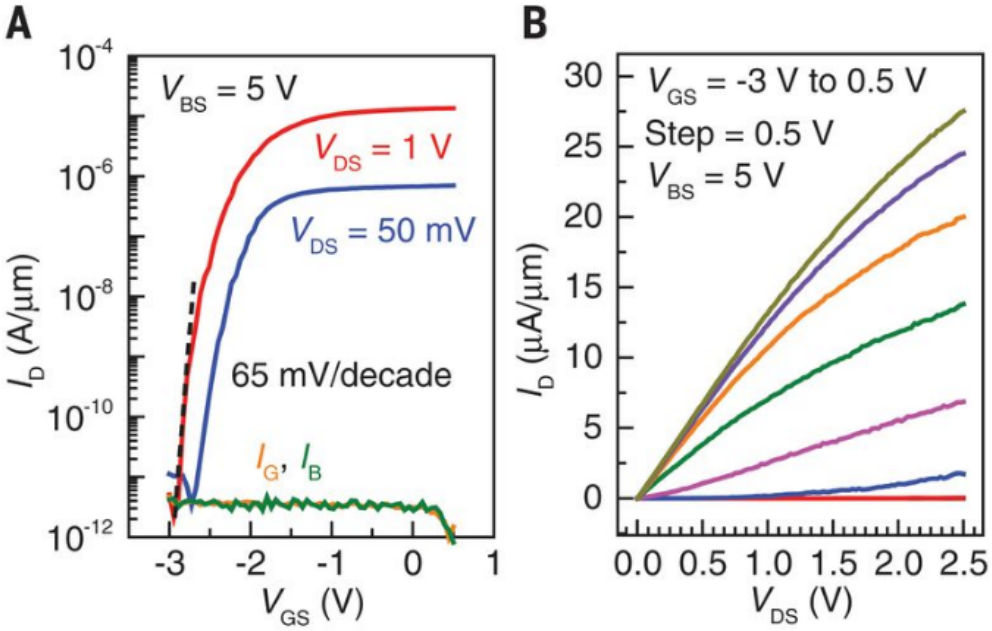
1-nm Gate Length MOSFET

S. B. Desai *et al.*, *Science*, Vol. 354, No. 6308, pp. 99-102, 2016

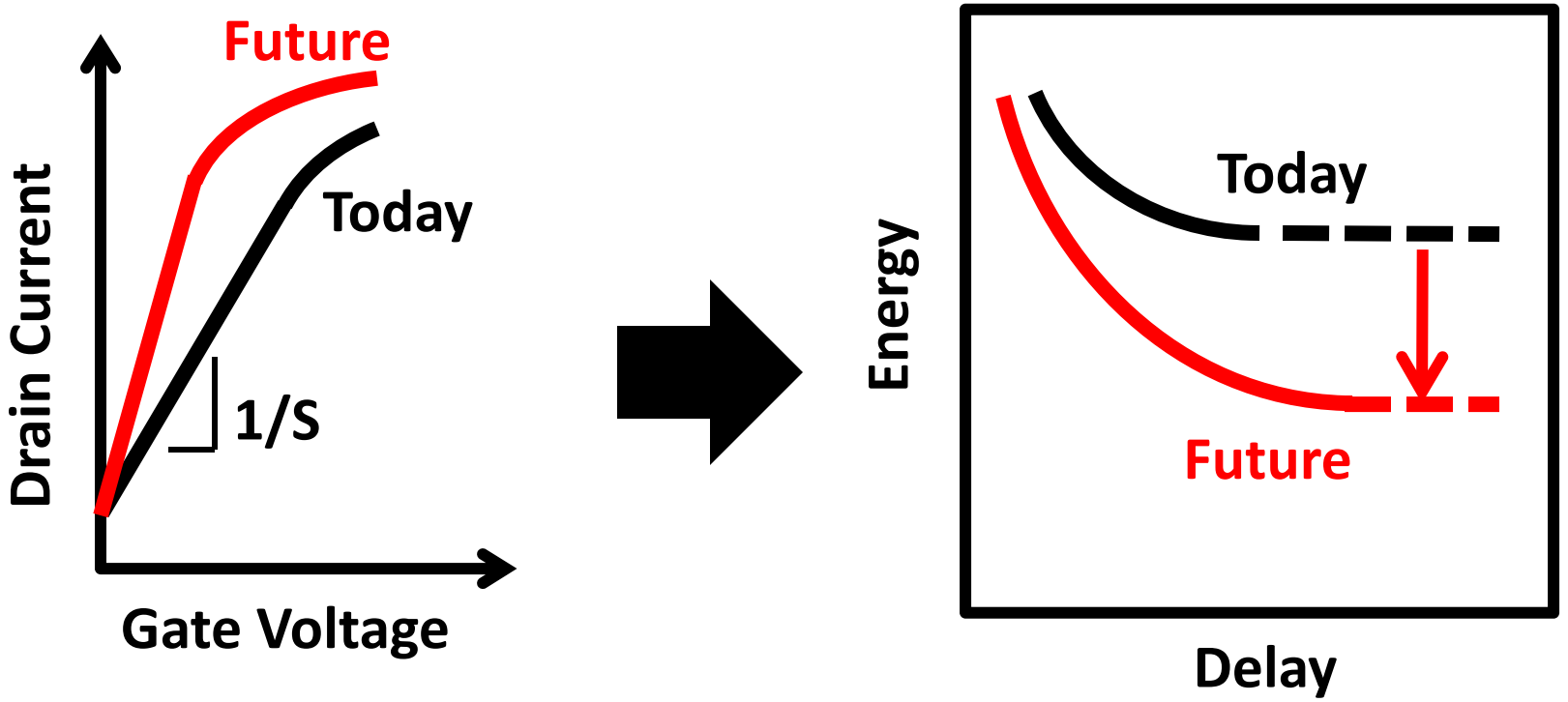


- **A 1-nm-diameter CNT-gated MoS_2 MOSFET is demonstrated with ON/OFF current ratio ~10^6 (V_{DD} ~1 V)**
  - ✓ **Heavier m_{eff} ($0.45m_0$ *vs.* $0.26m_0$ in Si)**
  - ✓ **Bandgap energy ~1.3 eV**





Future Logic Switches



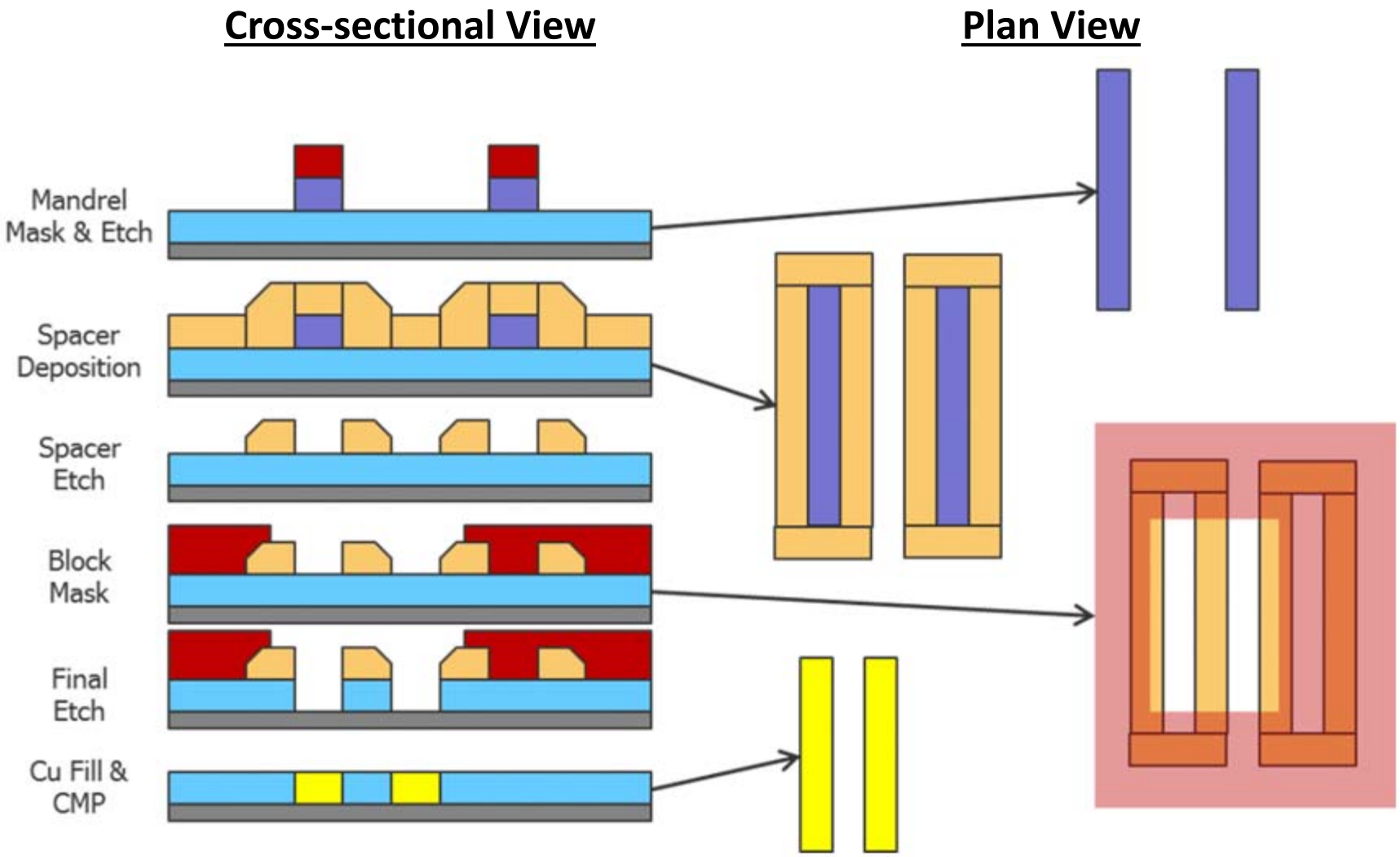
- Higher I_{ON}/I_{OFF} ratio → lower minimum Energy/op

→ Steeper switching behavior needed (S < 60mV/dec)

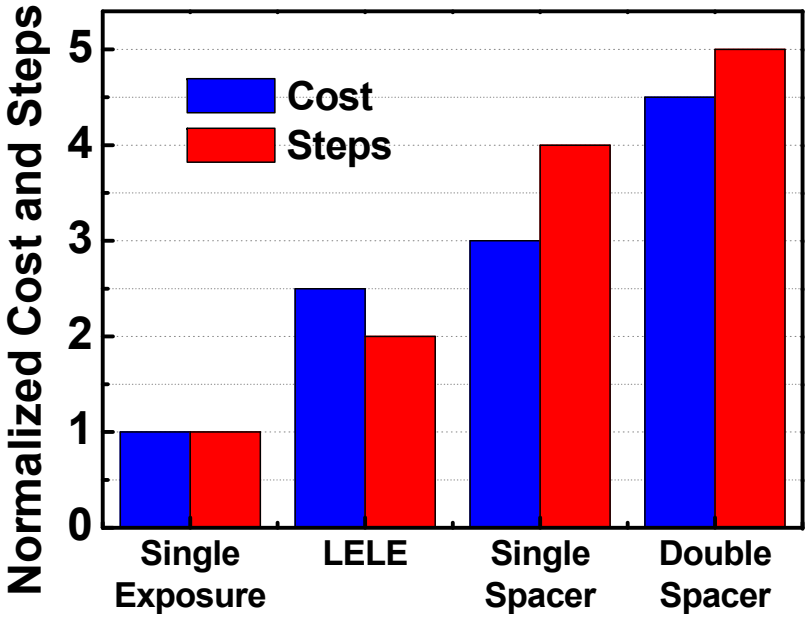
Outline

- Transistor Scaling to the Limit
- **Extending the Era of Moore's Law**
- Summary

Self-Aligned Double Patterning



Multiple-patterning techniques have extended Moore's Law beyond the lithographic resolution limit – at increasing cost



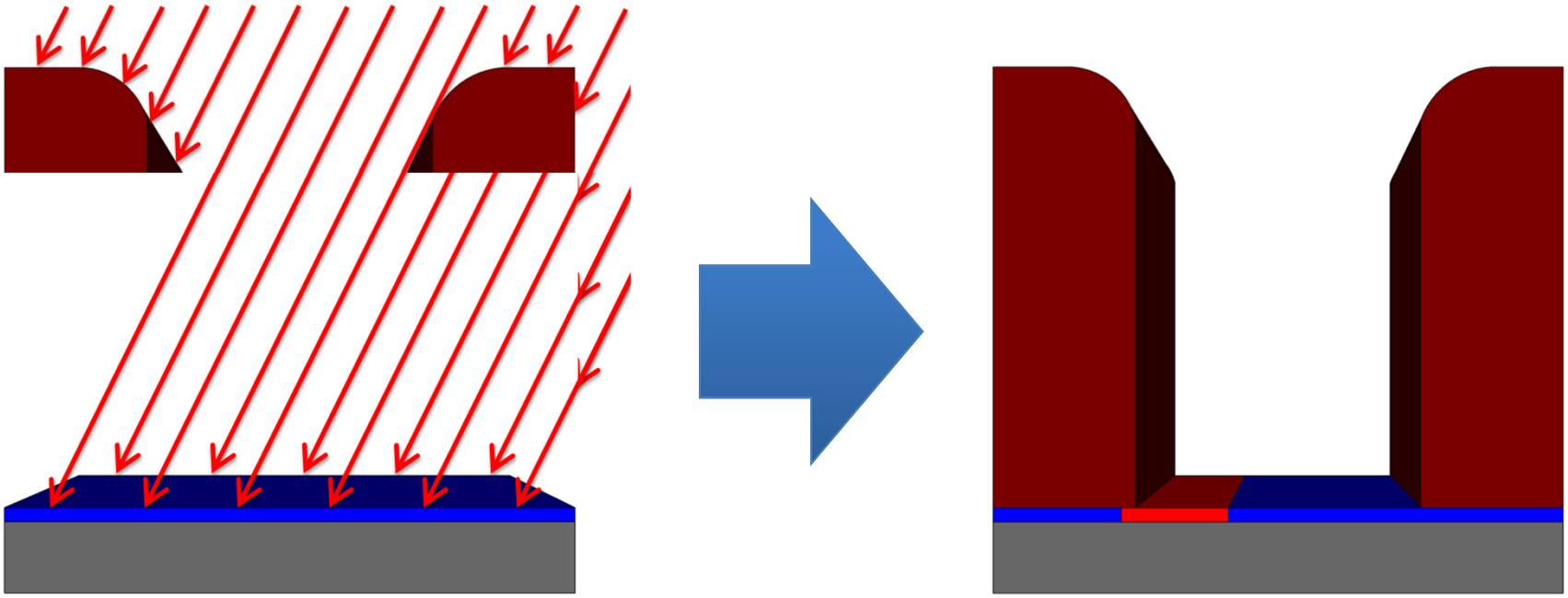
Samsung, EUVL Symposium 2009
ASML, SPIE Advanced Lithography 2012

"The sheer cost and complexity of this lithographic solution could dissuade chipmakers from jumping to future nodes, thereby stunting the growth rates of the IC industry."

- *Semiconductor Engineering*, April 17th, 2014

Tilted ion implantation (TII) Approach

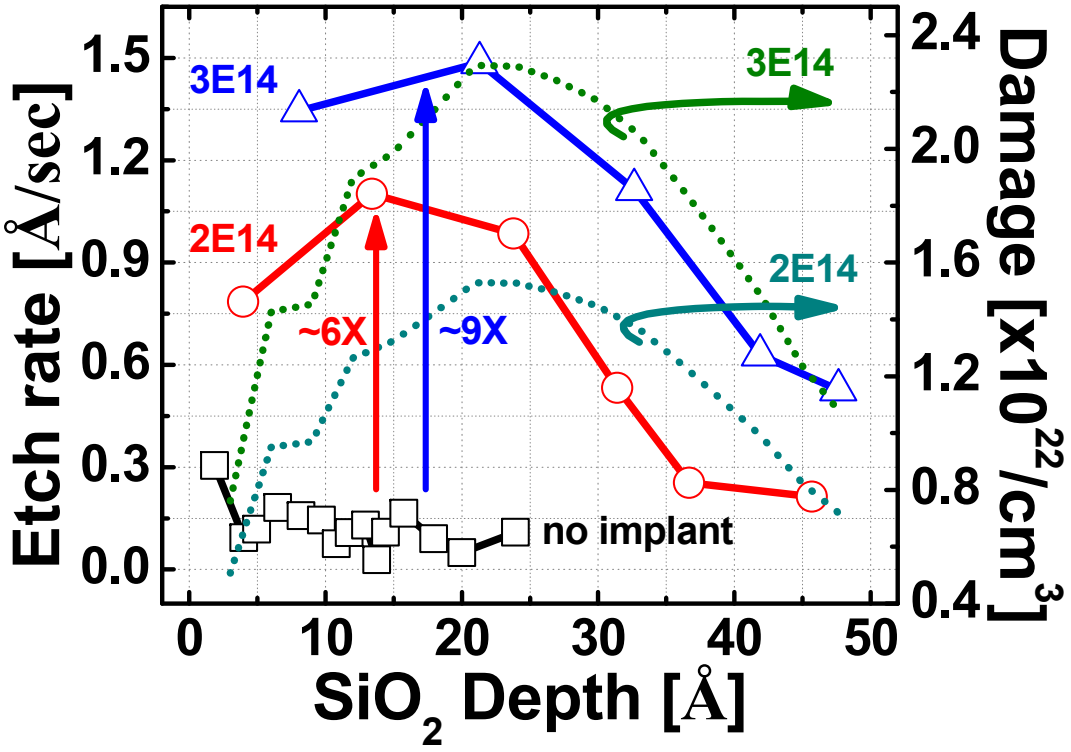
- **A sub-lithographic damage region can be achieved by tilted ion implantation (TII) + photoresist/hard mask**
  - **self-aligned to pre-existing mask features on surface**



Impact of TII on SiO_2 Etch Rate

S. W. Kim *et al.*, SPIE Advanced Lithography 2016

Ar^+ implant conditions: 15° tilt; 1.5 keV; dose = 0, 2 or 3 x $10^{14}/cm^2$



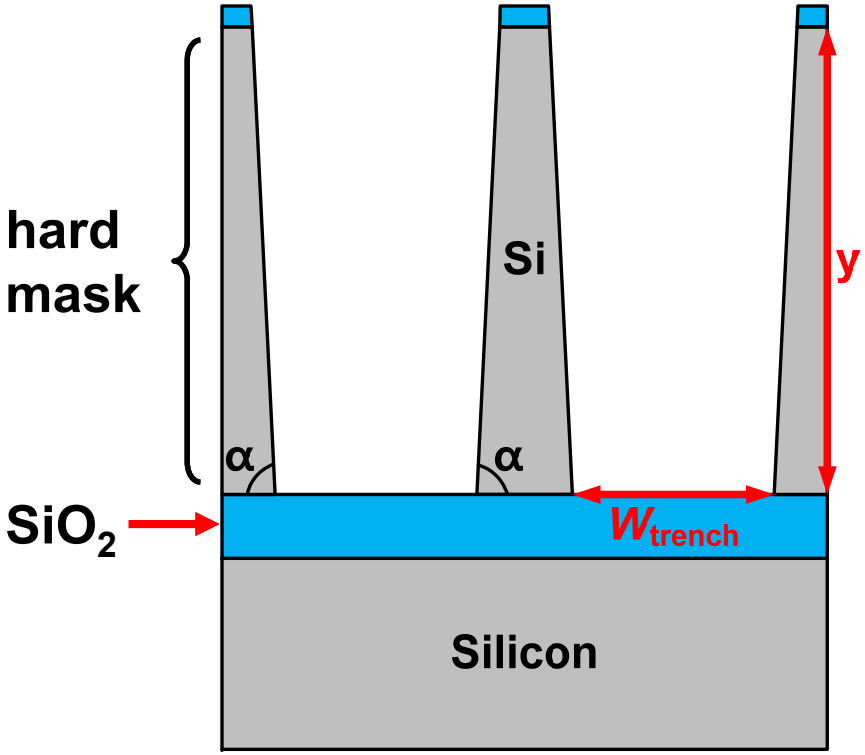
<u>Symbols & solid lines</u>:

etch rate in 200:1 DHF

<u>Dotted lines</u>:

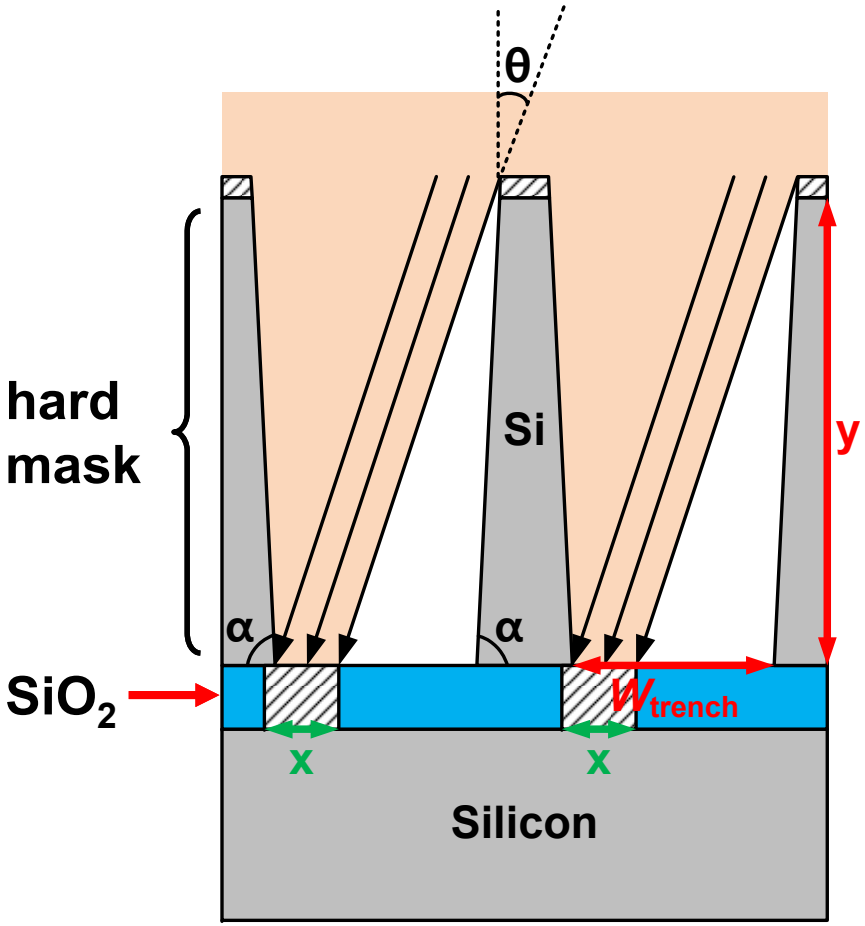
damage profile (SRIM)

Double-Patterning by TII



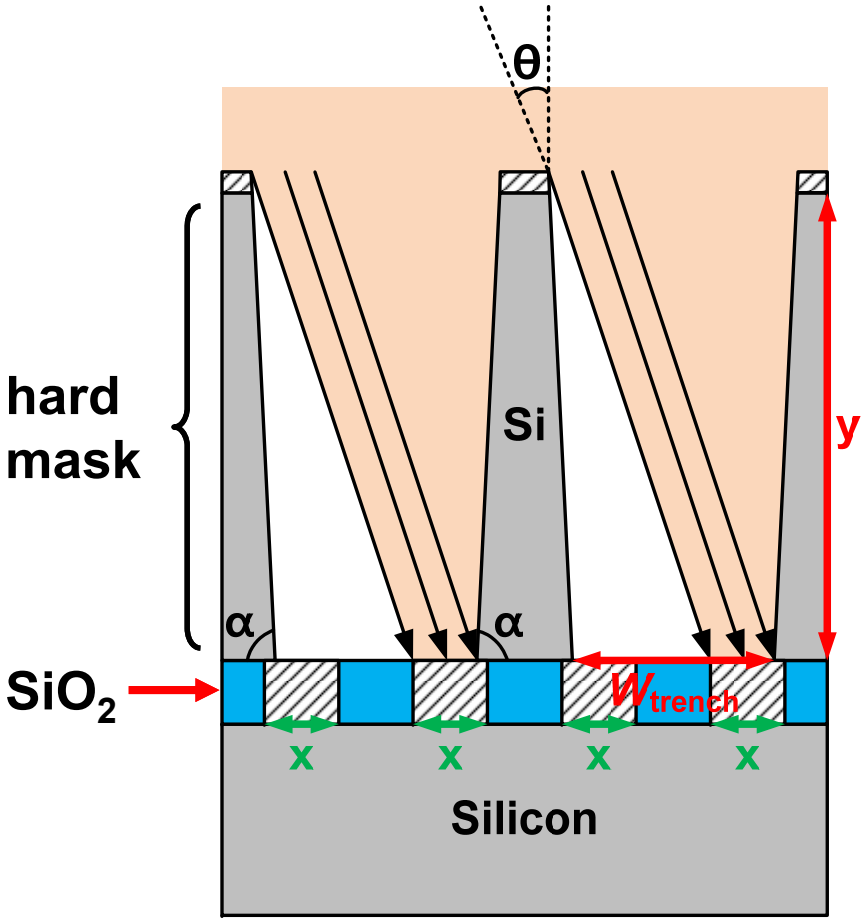
- Thermal SiO_2: masking layer
- Formation of linear a-Si hard-mask features by spacer patterning

Double-Patterning by TII



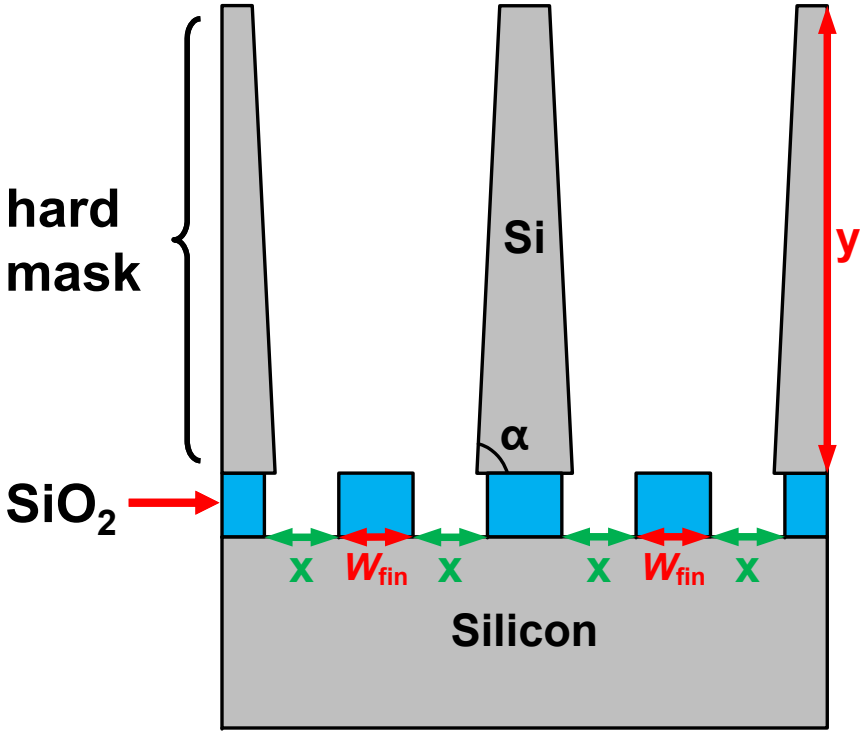
- Thermal SiO_2: masking layer
- Formation of linear a-Si hard-mask features by spacer patterning
- **First implant: positive tilt angle**
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$

Double-Patterning by TII



- Thermal SiO_2: masking layer
- Formation of linear a-Si hard-mask features by spacer patterning
- First implant: positive tilt angle
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$
- **Second implant: negative tilt angle**
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$

Double-Patterning by TII

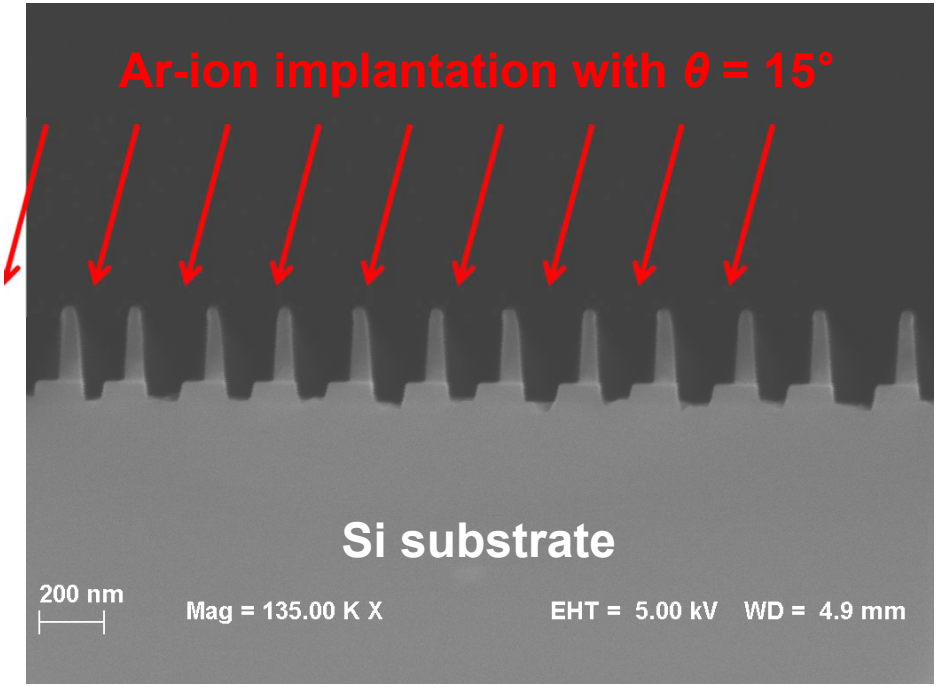


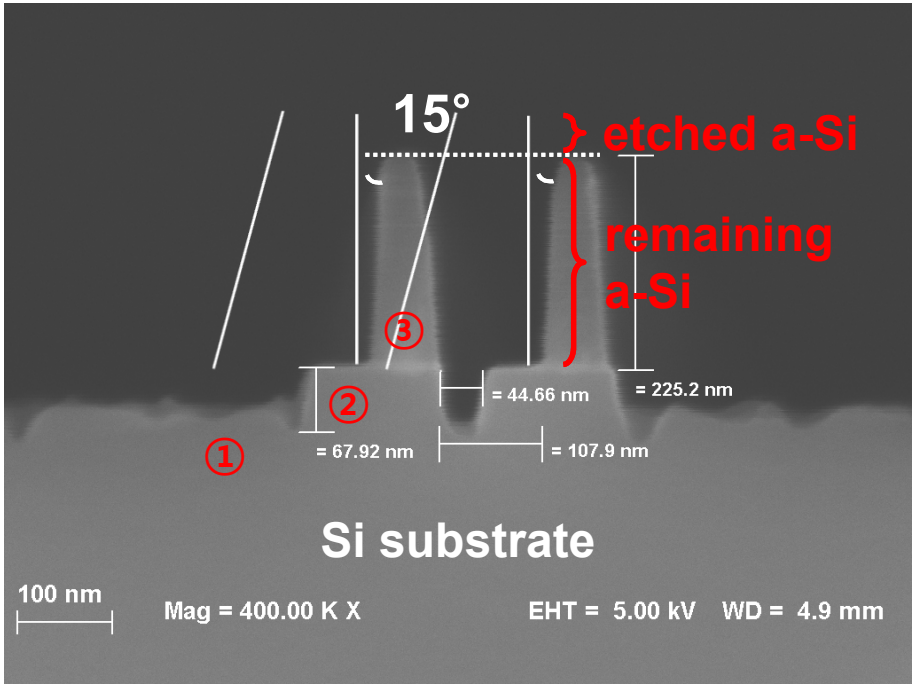
- Thermal SiO_2: masking layer
- Formation of linear a-Si hard-mask features by spacer patterning
- First implant: positive tilt angle
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$
- Second implant: negative tilt angle
  $x \cong W_{trench} - y(\tan(\theta) - \cot(\alpha))$
- **Selective removal of damaged SiO_2**
- **Si substrate dry etch**
  $W_{fin} \cong 2y(\tan(\theta) - \cot(\alpha)) - W_{trench}$

Proof of Concept: Single Implant

S. W. Kim *et al.* (UC Berkeley), SPIE Advanced Lithography 2016

Cross-sectional Scanning Electron Micrographs

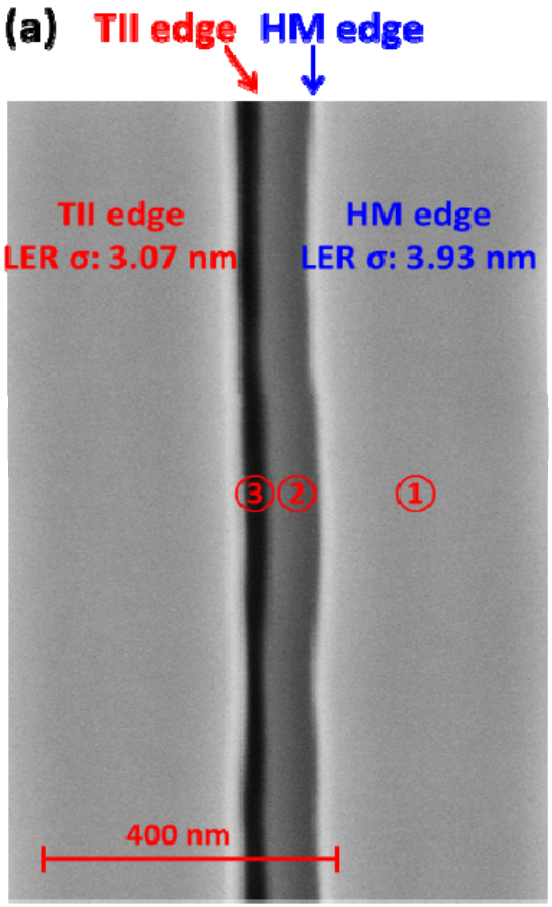




- **Sub-lithographic features (~45 nm) achieved by 15° tilt, 3.0 keV Ar^+ implant into 10 nm-thick SiO_2 hard mask**
  - **→ dilute HF etch**
  - **→ Si dry etch**

Self-Aligned Nature of TII Patterning

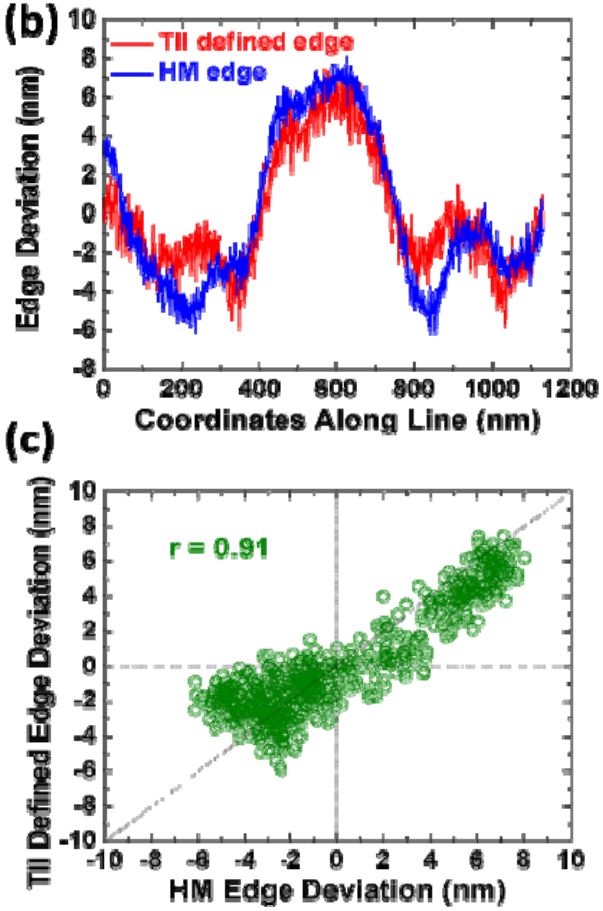
P. Zheng *et al.* (UC Berkeley), *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 231-236, 2017



① = a-Si hard mask

② = un-etched c-Si

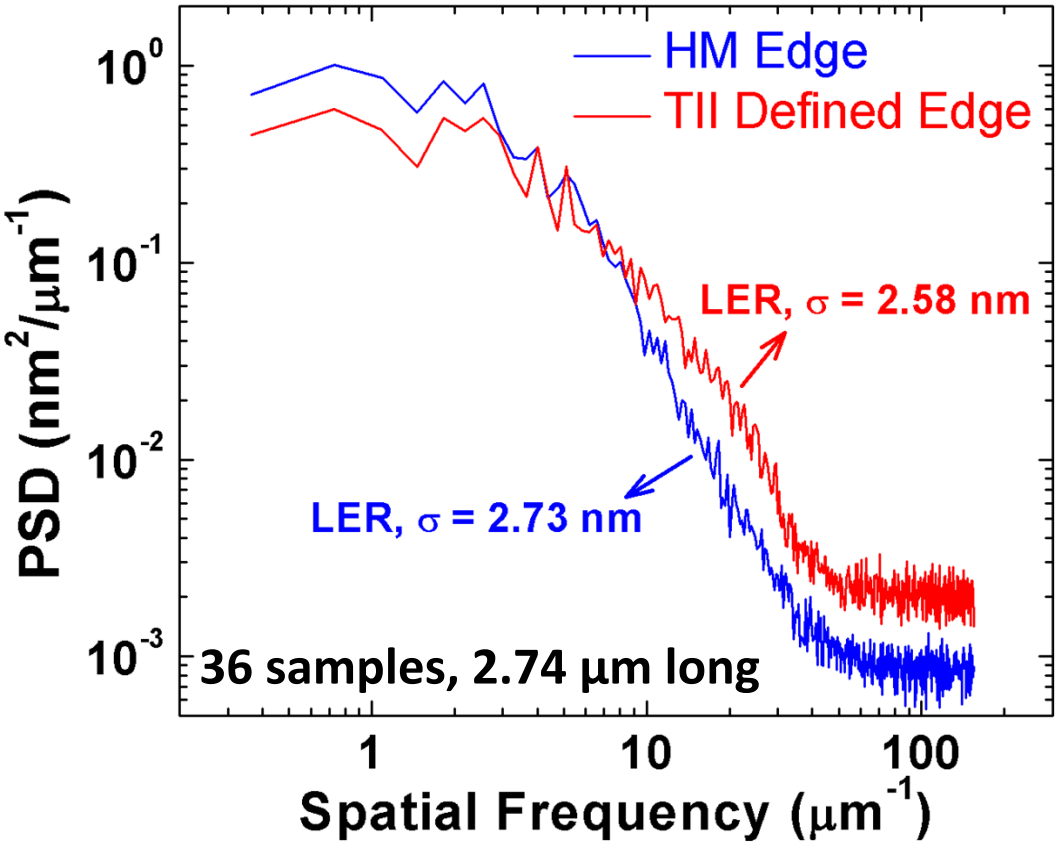
③ = etched c-Si



- **The TII-defined edge closely tracks the HM edge**

Line-Edge Roughness Comparison

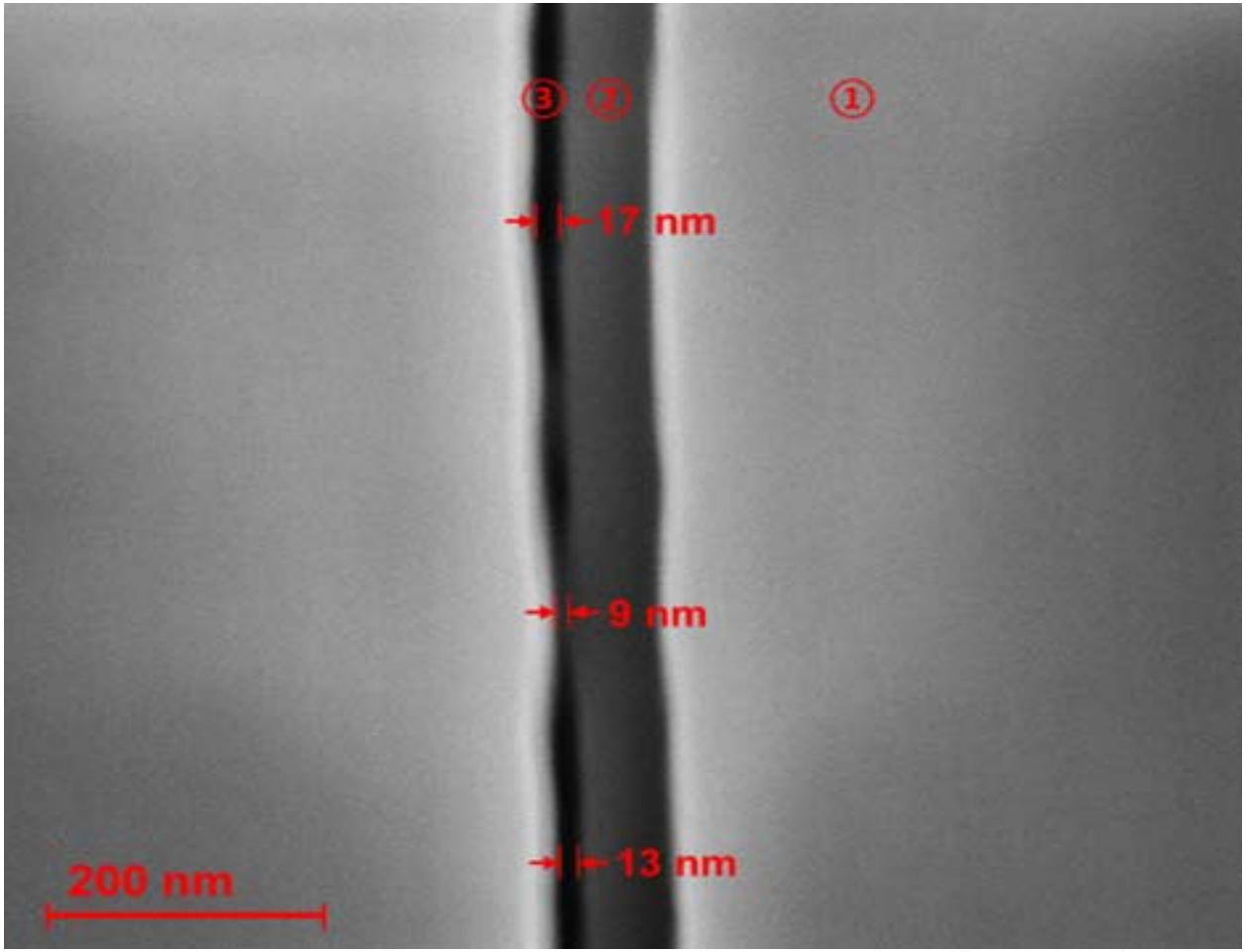
P. Zheng *et al.* (UC Berkeley), *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 231-236, 2017



- **TII improves low- and mid-frequency line-edge roughness**

TII Patterning Resolution Limit

P. Zheng *et al.* (UC Berkeley), *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 231-236, 2017

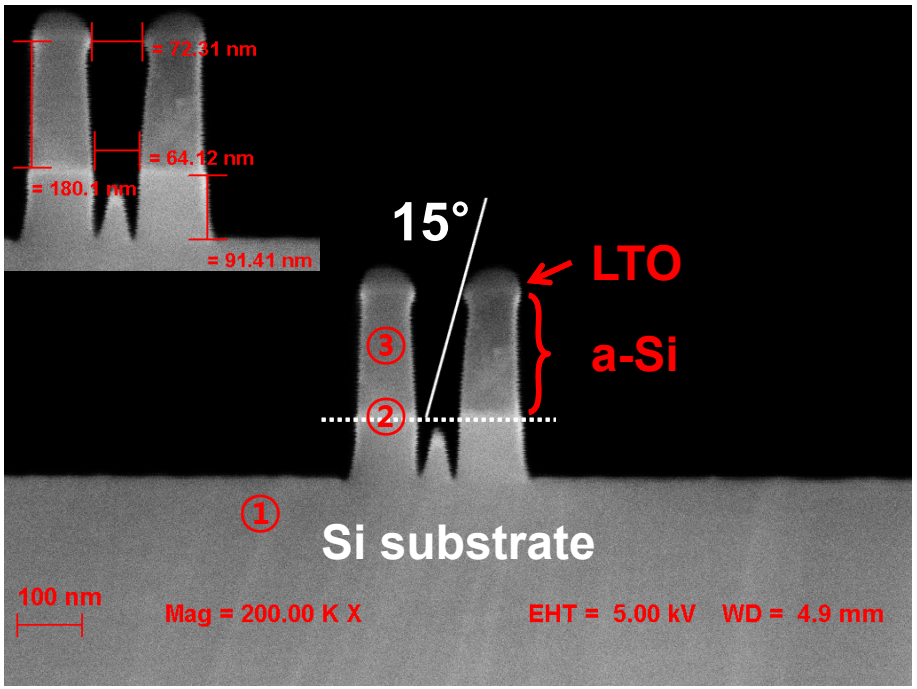


- **TII can be used to pattern features as small as 10 nm.**

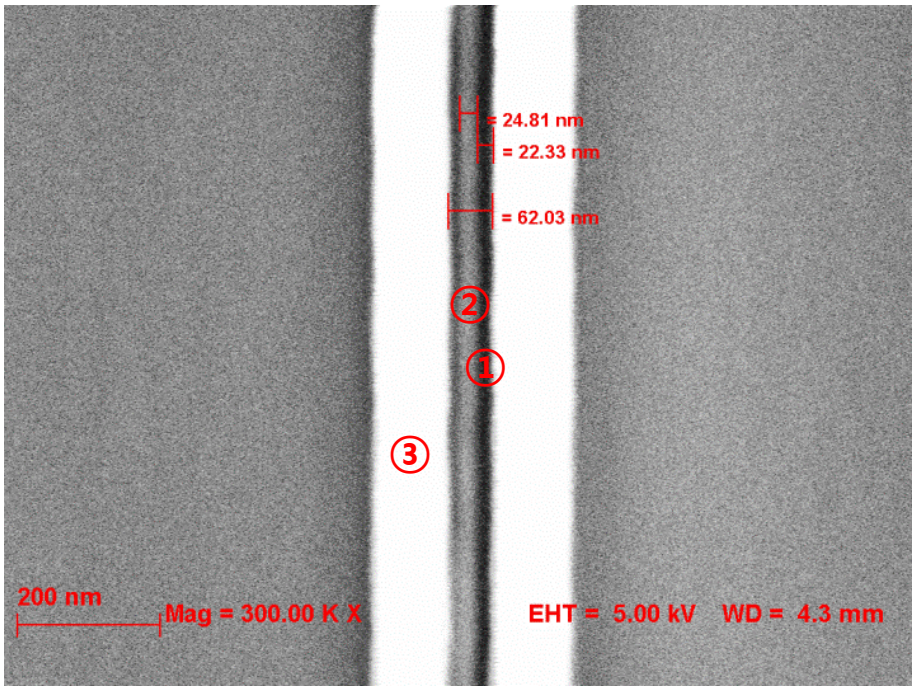
Double Tilted Implant Results

S. W. Kim *et al.* (UC Berkeley), SPIE Advanced Lithography 2016

Cross-sectional SEM



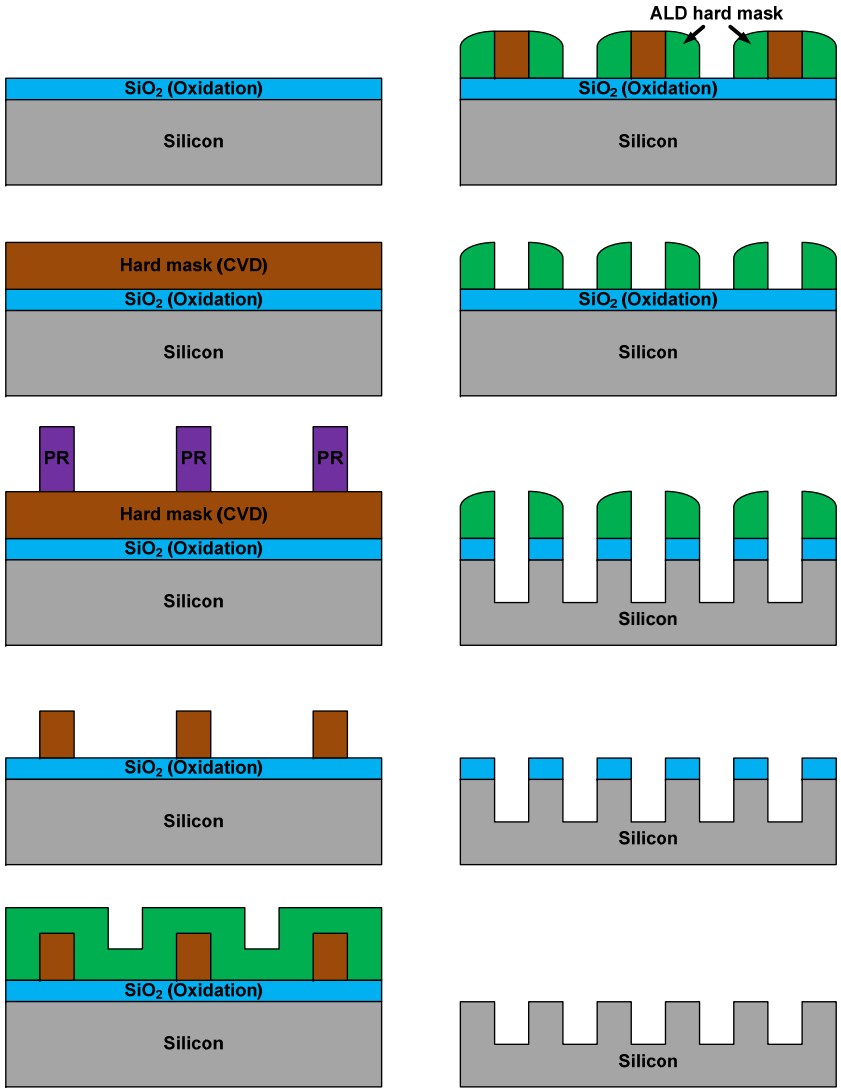
Plan-view SEM



- **Local pitch-halving achieved with ±15° tilt, 3.0 keV Ar^+ implants**
- **~21 nm half-pitch of the etched Si features**

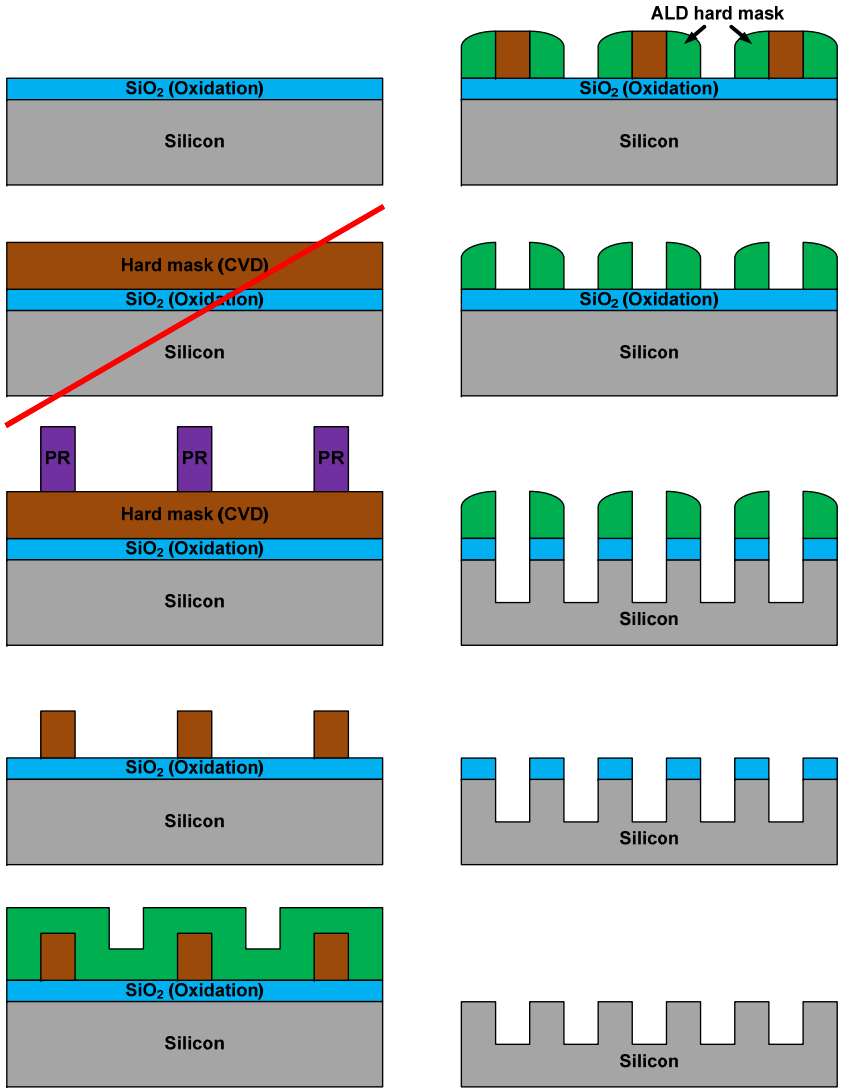
Double-Patterning Approaches

Spacer lithography (SADP)

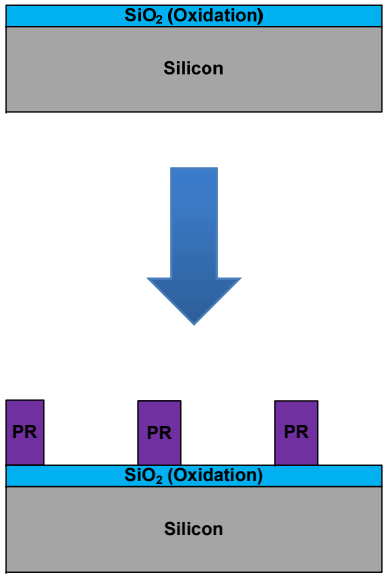


Double-Patterning Approaches

Spacer lithography (SADP)

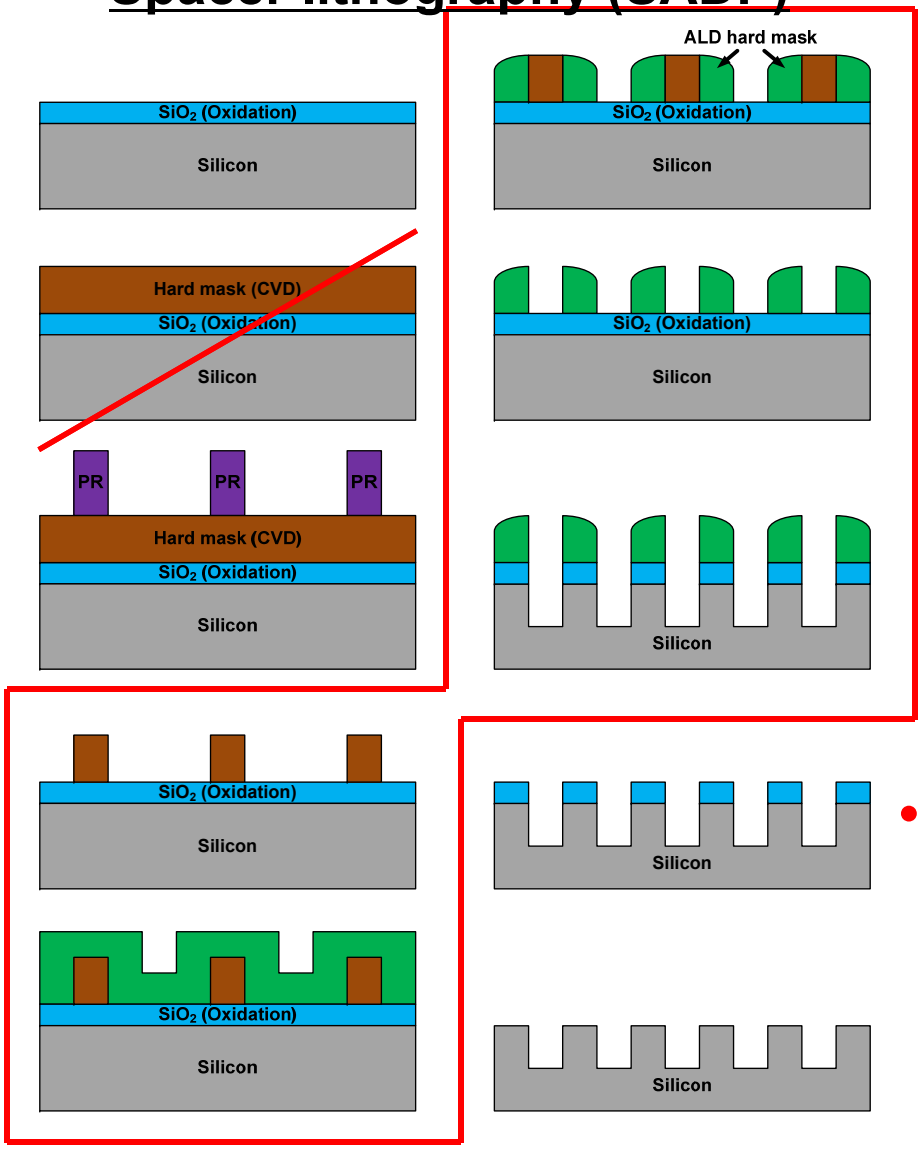


Tilted Ion Implantation (TII)

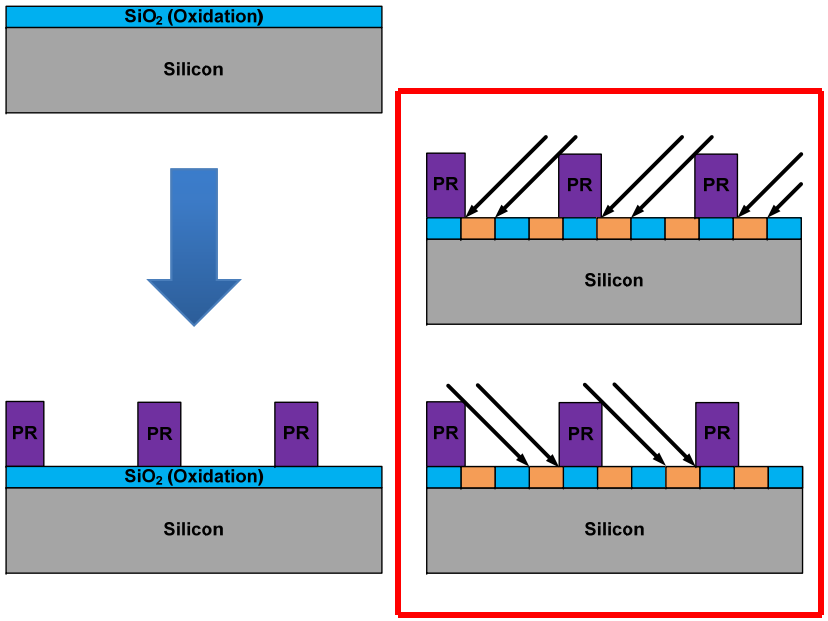


Double-Patterning Approaches

Spacer lithography (SADP)



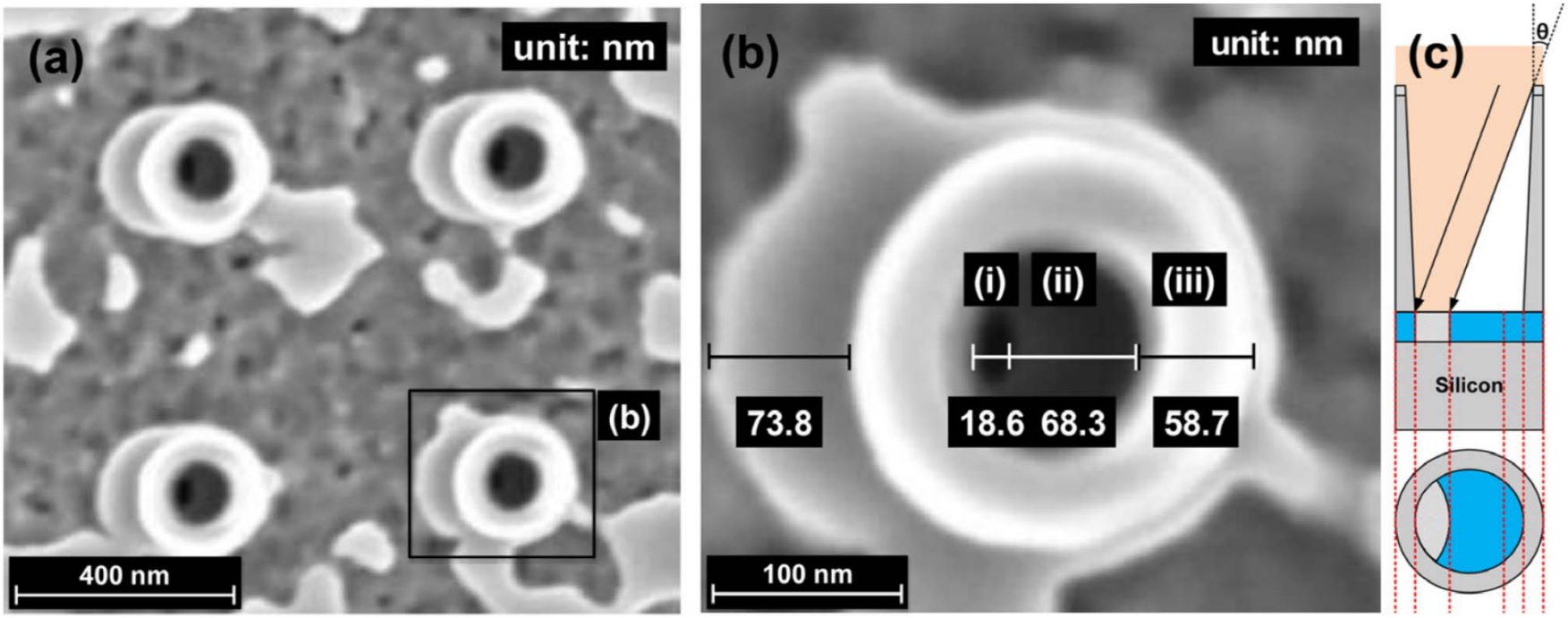
Tilted Ion Implantation (TII)



- **The cost of TII double-patterning can be only ~60% of the cost of SADP.**

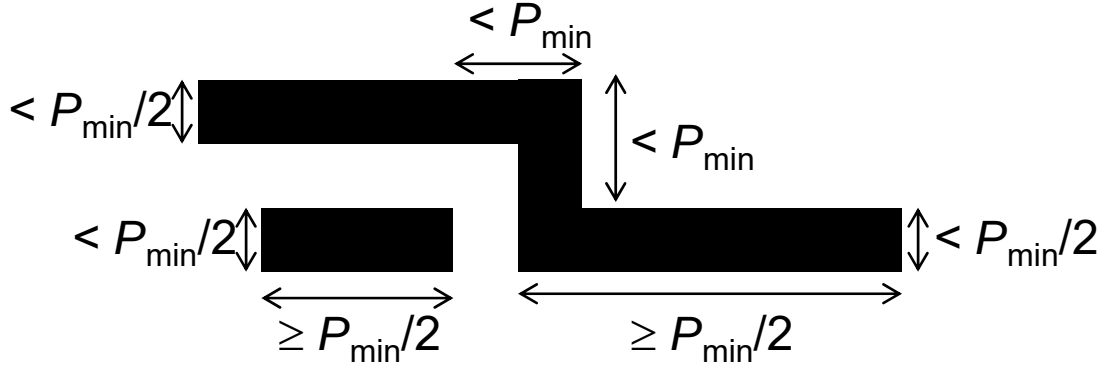
Sub-Lithographic Hole Formation

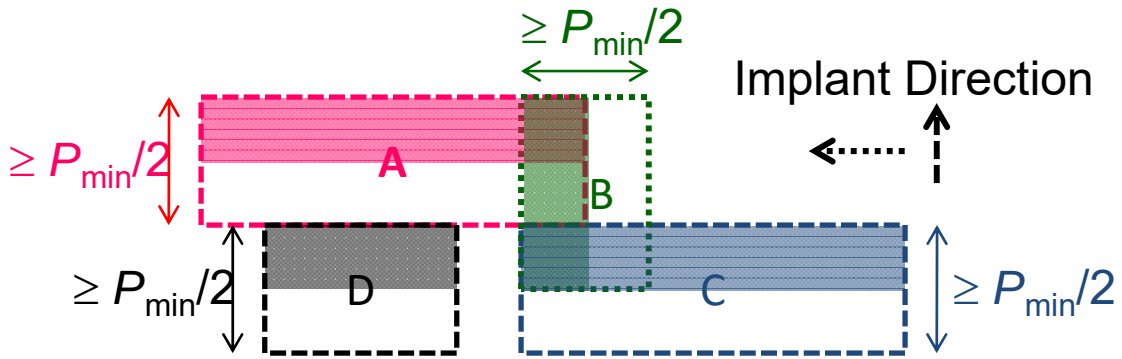
S. W. Kim *et al.* (UC Berkeley), *Journal of Vacuum Science & Technology B*, vol. 34, 040608, 2016



Future Work: 2D Patterning by TII

1. Coat IC layer with HM layer;
2. Perform multiple litho+TII processes in sequence, such that each litho+TII process forms a latent 1D pattern in the HM layer;





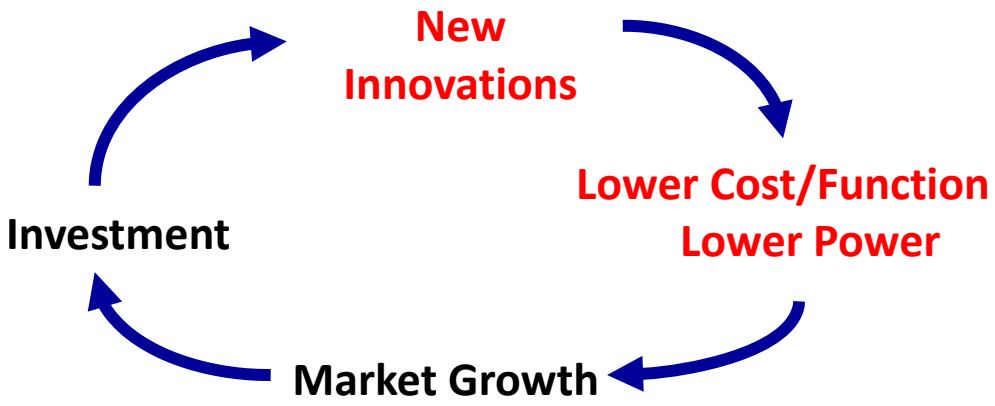
3. Selectively etch the HM layer to form the composite 2D pattern;
4. Transfer the 2D pattern to the IC layer by a selective etch process.

Outline

- Transistor Scaling to the Limit
- Extending the Era of Moore's Law
- **Summary**

Summary

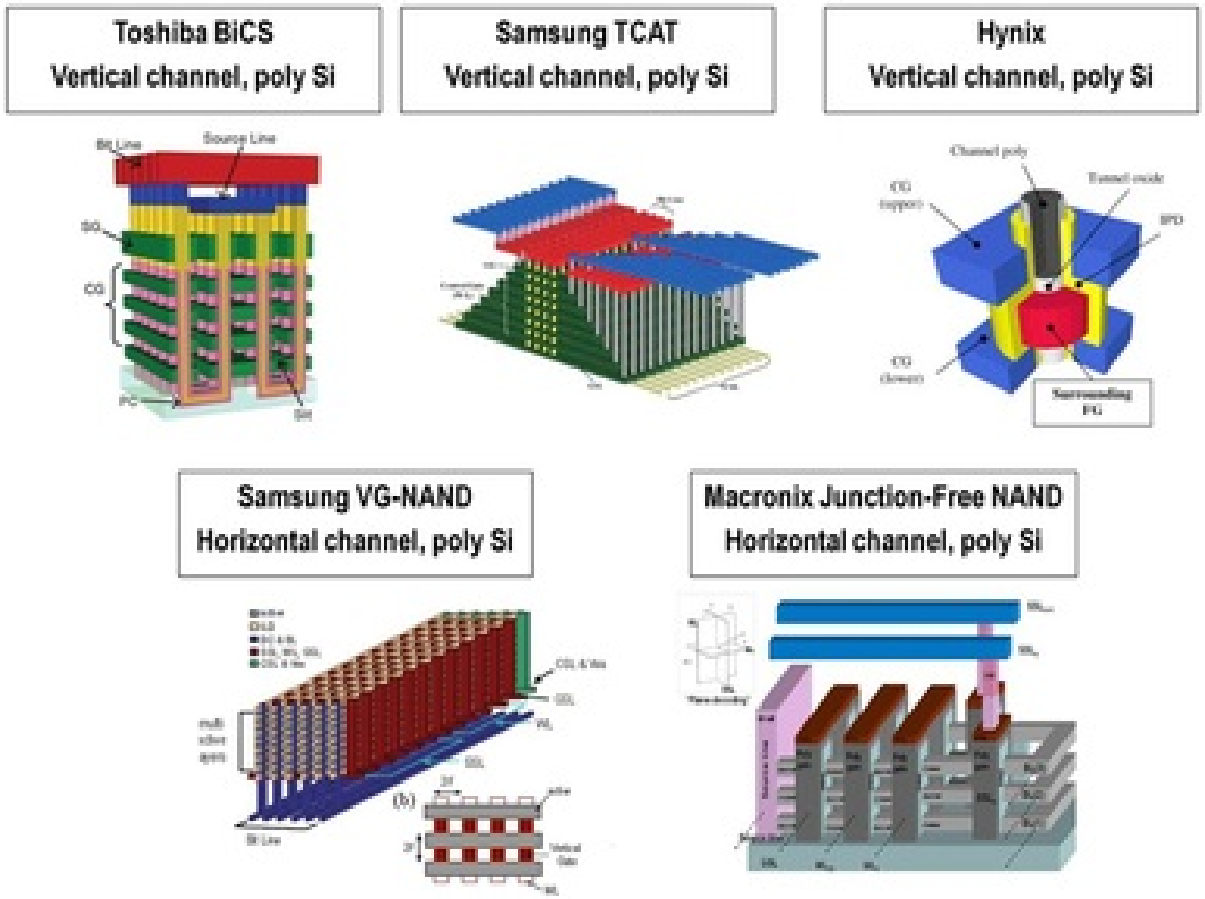
- **There's still plenty of room for CMOS technology scaling!**
  - **Advancements in transistor structures and materials will enable continued miniaturization and voltage scaling.**
- **Innovations to mitigate the challenge of growing cost of patterning are needed to extend the era of Moore's Law**



Acknowledgements

- **TII-Enhanced Lithography:**
  - Dr. Sang Wan Kim (now with Ajou University)
  - Dr. Peng Zheng (now with Intel Corporation)
  - Dr. Leonard Rubin (Axcelis Technologies)
  - UC Berkeley Marvell Nanofabrication Laboratory
  - Funding from Applied Materials, Lam Research, National Science Foundation

3-D NAND Flash Technology



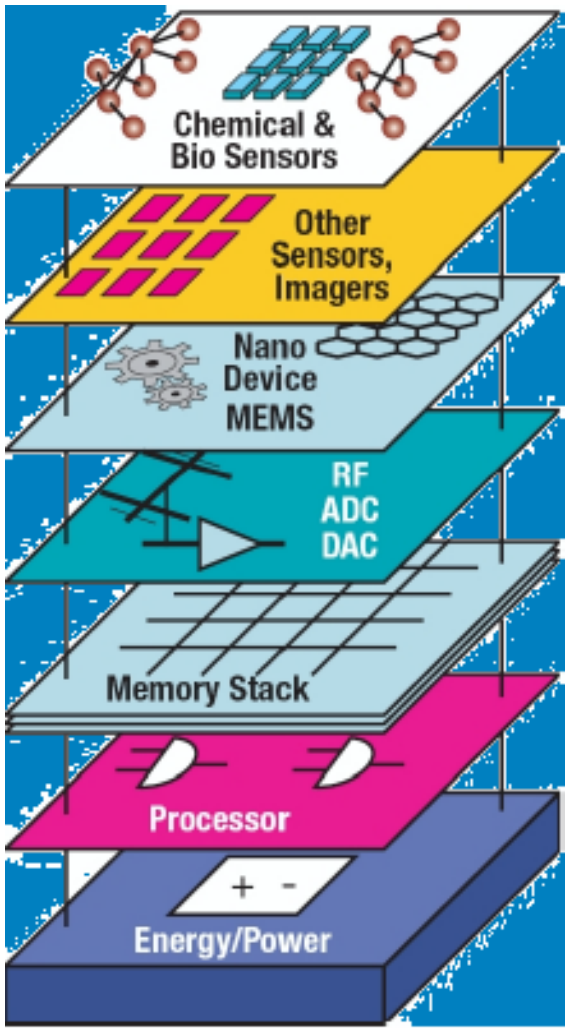
Vertical FETs (vFETs):

- **Poly-Si is used as the semiconductor material.**
- **Lithography steps for multiple memory layers are shared.**

- **Density scaling is not driven by lithography.**
- **Aspect ratios of etched and filled features are large (>40:1).**

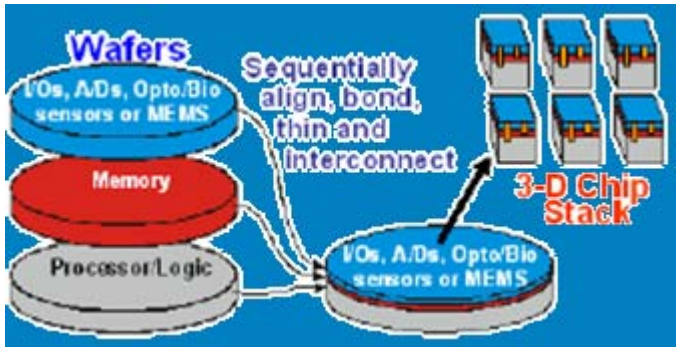
http://www.monolithic3d.com/uploads/6/0/5/5/6055488/695394.jpg?388

Heterogeneous Integration

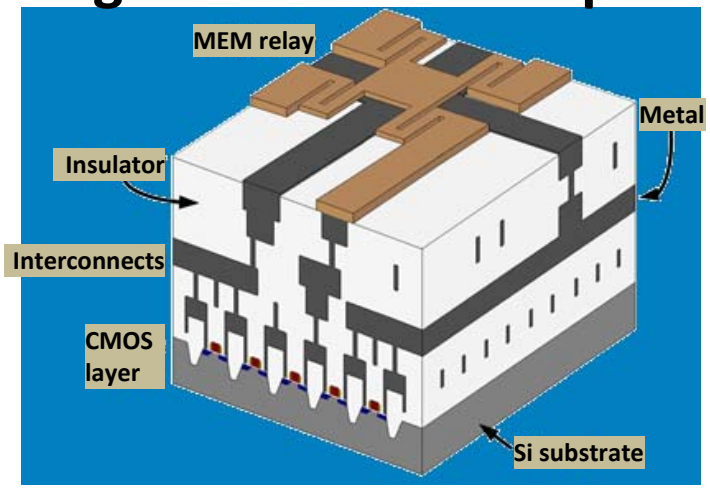


Enhanced performance & functionality in a compact form factor

- **Separate layer fabrication processes**



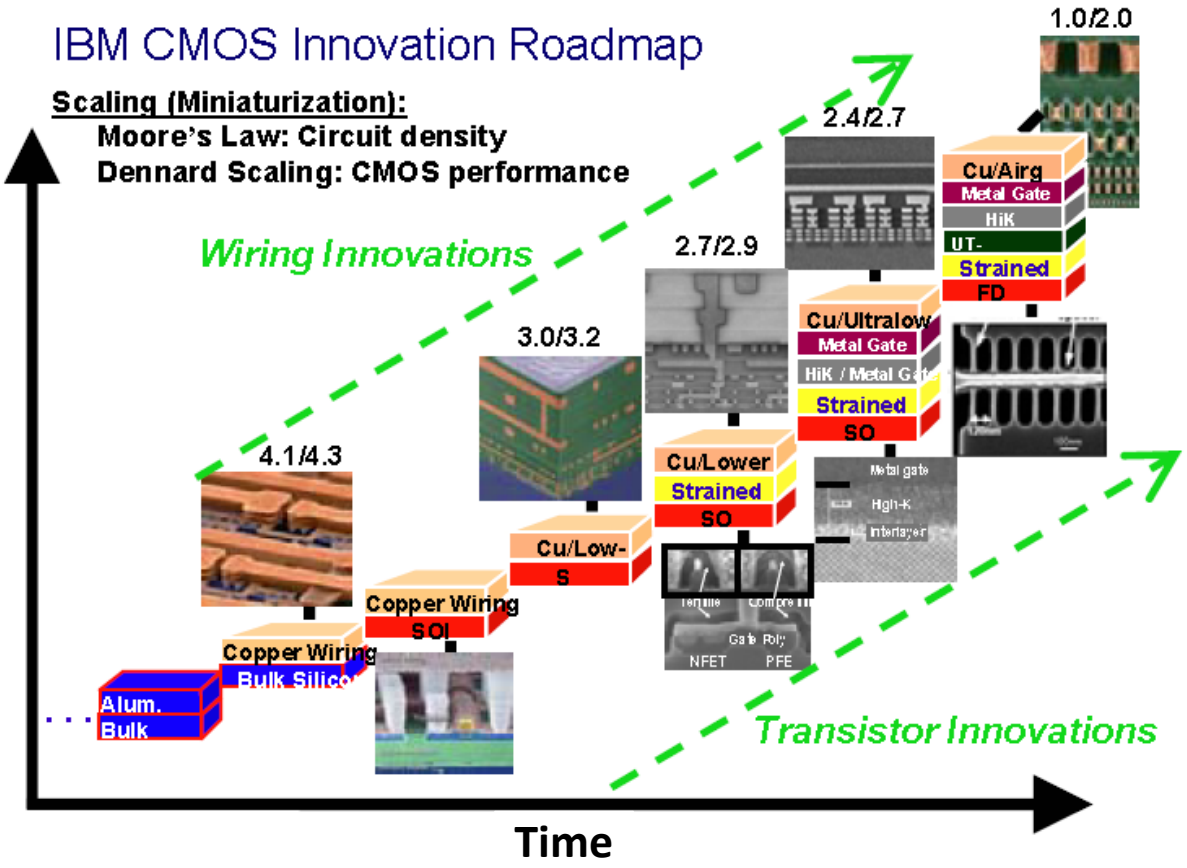
- **Integrated fabrication process**

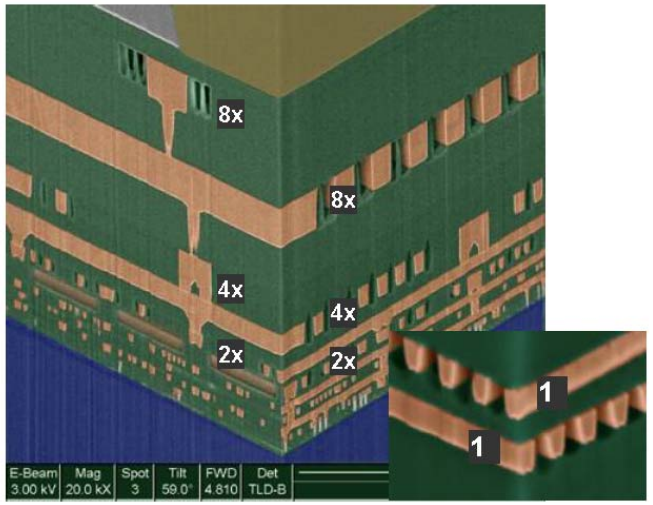


J. J.-Q. Lu *et al.*, *Future Fab Int'l*, Issue 23, 2007

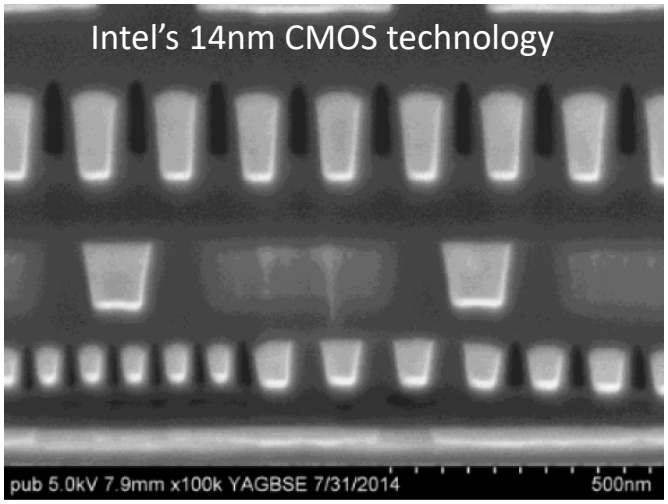
V. Pott *et al.*, *Proc. IEEE*, Vol. 98, 2010

IC Technology Advancement





D. C. Edelstein, *214th ECS Meeting*, Abstract #2073, 2008

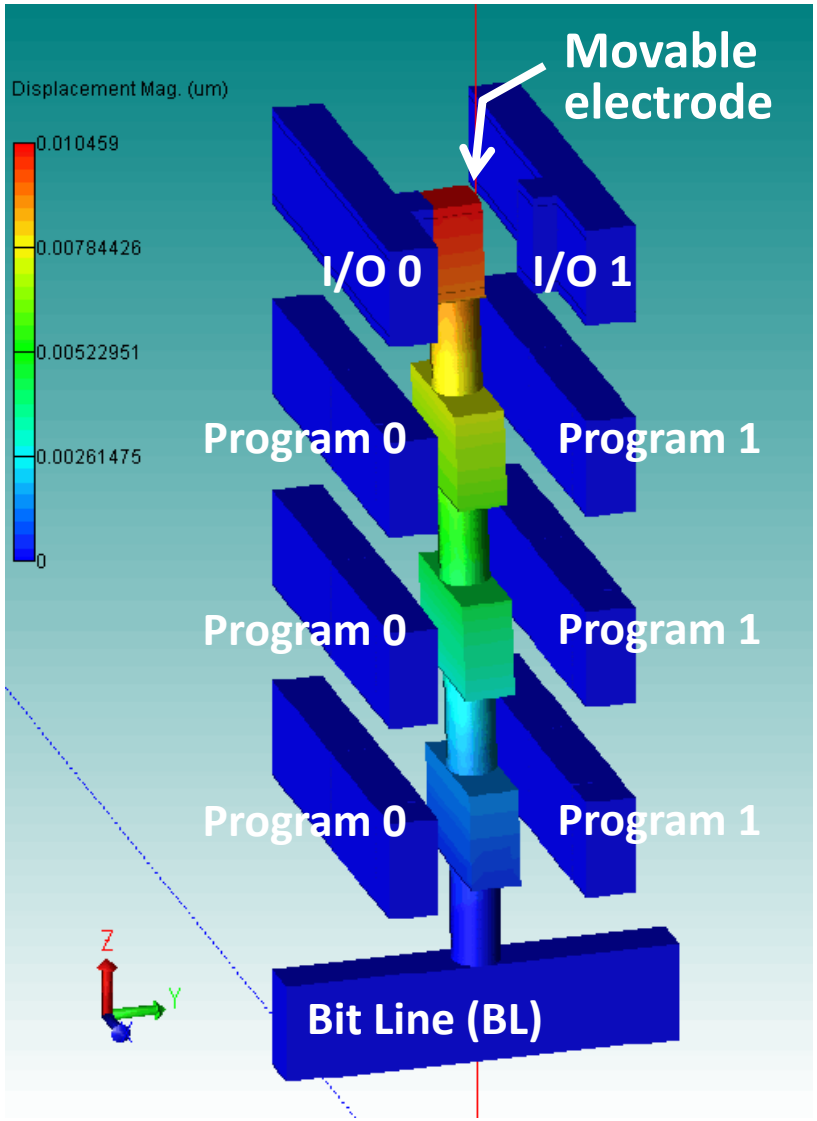


S. Natarajan *et al*. (Intel), *IEDM* 2014

- **Advanced back-end-of-line (BEOL) processes have air-gapped interconnects**

Reconfigurable Interconnect

K. Kato *et al.*, *IEEE Electron Device Letters*, vol. 37, no. 12, pp. 1563-1565, 2016.



- **A bi-stable switch is implemented using multiple metal layers**

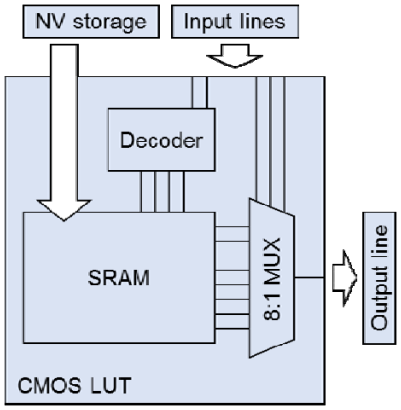
  Vias are for electrical connection and flexural elements for a more compliant electrode, for lower programming voltage.

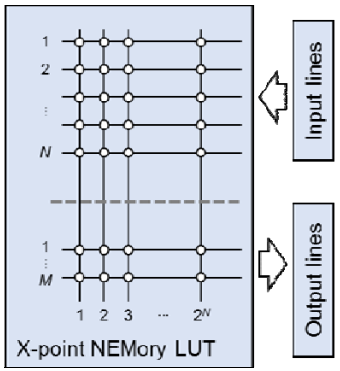
- **Small footprint due to vertically oriented movable electrode, and shared actuation and contacting electrodes across the array**

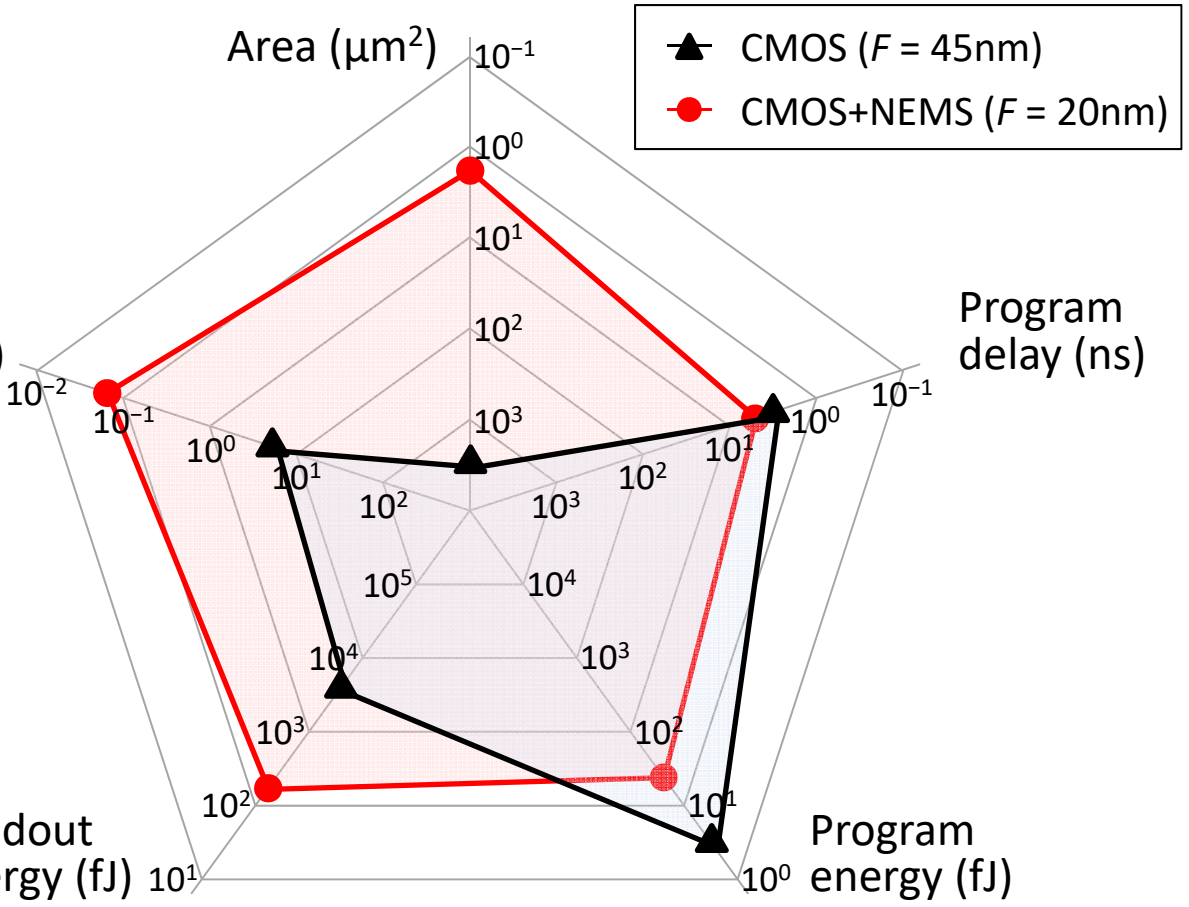
- **A non-linear device can be integrated to prevent sneak leakage current in a cross-point array**

LUT Performance Comparison

K. Kato *et al.*, *IEEE Electron Device Letters*, vol. 37, no. 12, pp. 1563-1565, 2016







✓ **More compact, faster, and energy-efficient than CMOS!**