NANOELECTRONICS AND PLASMA PROCESSING — THE NEXT 15 YEARS AND BEYOND

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OUTLINE

- The nanoelectronics revolution
- Dual frequency capacitive discharges
  – Standing waves and skin effects
- The next 15 years and beyond

W.P. Allis (1901–1999)
Co-founder of the GEC

THE NANOELECTRONICS REVOLUTION

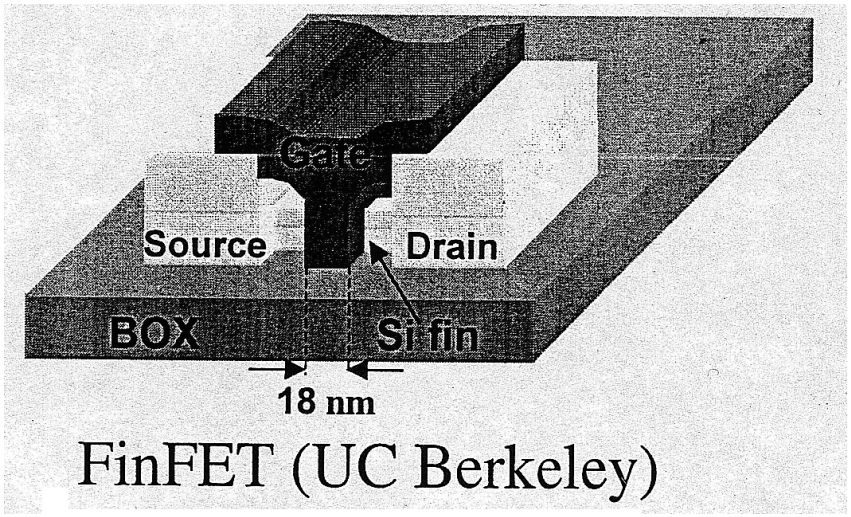
THE NANOELECTRONICS REVOLUTION

- Transistors/chip doubling every $1\frac{1}{2}$–2 years since 1959
- 1,000,000-fold decrease in cost for the same performance in the last 30 years

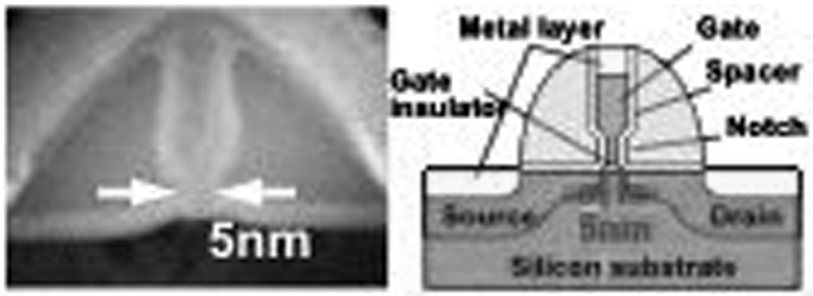
EQUIVALENT AUTOMOTIVE ADVANCE

- 60 million miles/hr
- 20 million miles/gal
- Throw away rather than pay parking fees
- 3 mm long $\times$ 1 mm wide
- Crash 3$\times$ a day

DOUBLE/TRI GATE TRANSISTORS



FinFET (UC Berkeley)

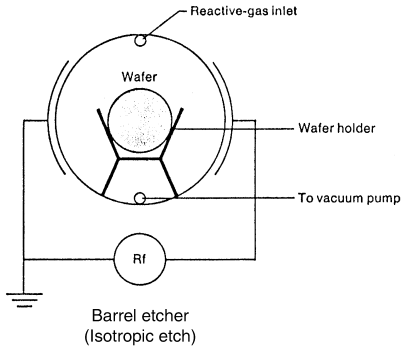


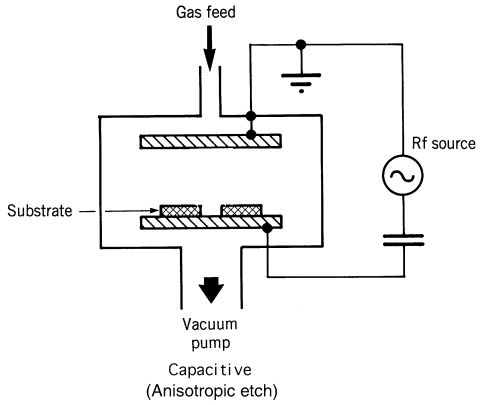
NEC 5 nm Gate

- Vertical structures can be built with current fabrication techniques
- CMOS can be scaled another 15 years
- State of the art (2005):
  - In manufacture:
    50 nm (200 atoms) gate length
    1.5 nm (5 atoms) gate oxide thickness
  - Smallest fabricated CMOS transistor (NEC):
    5 nm (20 atoms) gate length
  - Limiting gate length from simulations (desktop ic):
    4 nm (16 atoms) gate length

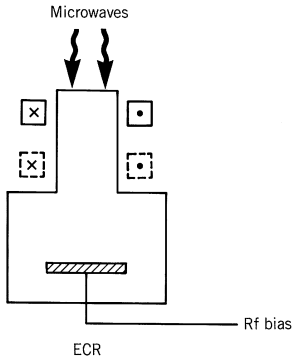
EVOLUTION OF ETCHING DISCHARGES

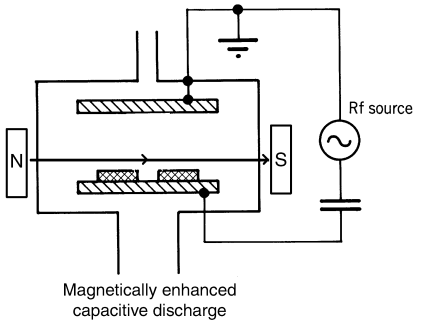
FIRST GENERATION

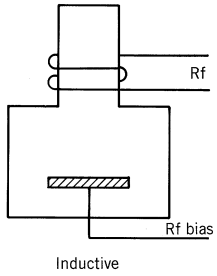




SECOND GENERATION

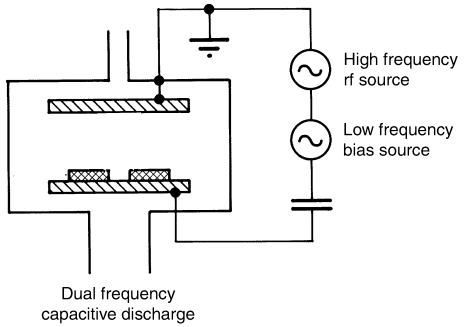






THIRD GENERATION

?



?

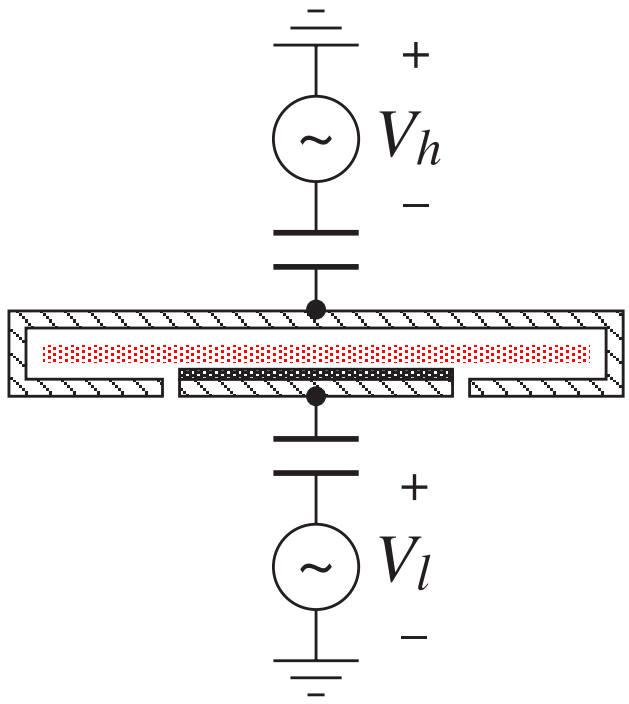
DUAL FREQUENCY CAPACITIVE DISCHARGES

WHY DUAL FREQUENCY CAPACITIVE DISCHARGES?

- In the year 2020
  — 6nm gate width, 6 billion transistors, 73 GHz on-chip clock
  — 14–18 wiring levels (dielectric layers) need to be etched
- Why capacitive discharge?
  — low surface area seen by plasma (inexpensive)
  — silicon upper electrode (control of F/CF_x ratio)
  — robust uniformity over wide pressure range
- Why dual frequency operation?
  — Independent control of ion flux and ion bombarding energy to the substrate

High frequency power controls ion flux Low frequency voltage controls ion energy

TYPICAL OPERATING CONDITIONS



$R \sim 15$–30 cm, $L \sim 1$–3 cm

$p \sim 30$–300 mTorr, $C_4F_8/O_2/Ar$ feedstock

High frequency $f_h \sim 27.1$–160 MHz, $V_h \sim 200$–500 V

Low frequency $f_l \sim 2$–13.56 MHz, $V_l \sim 500$–1500 V

Absorbed powers $P_h,\ P_l \sim 500$–3000 W

HIGH FREQUENCY ELECTROMAGNETIC EFFECTS

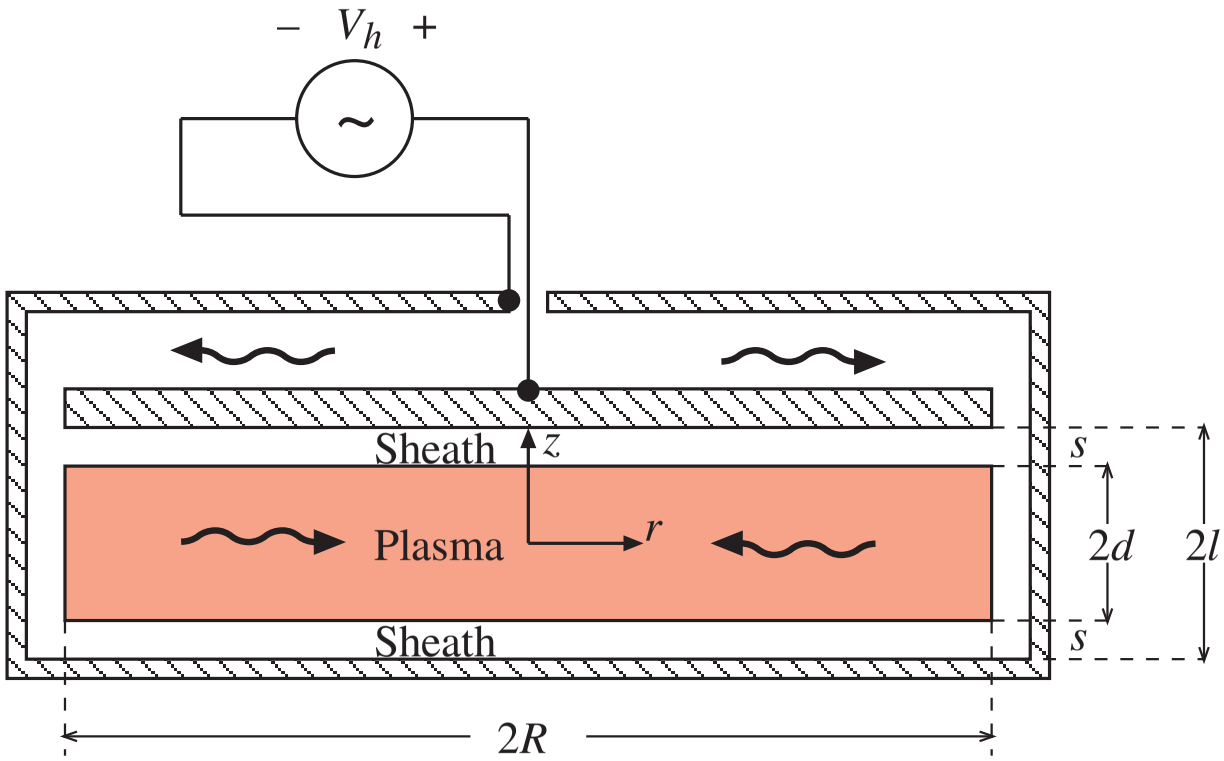
STANDING WAVES AND SKIN EFFECTS

- High frequency and large area ⇒ standing wave effects
- High frequency ⇒ high density ⇒ skin effects

1. M.A. Lieberman, J.P. Booth, P. Chabert, J.M. Rax, and M.M. Turner, *Plasma Sources Sci. Technol.* **11**, 283 (2002)
2. P. Chabert, *J. Phys. D: Appl. Phys.* **40**, R63 (2007)

CYLINDRICAL CAPACITIVE DISCHARGE

Consider only the high frequency source

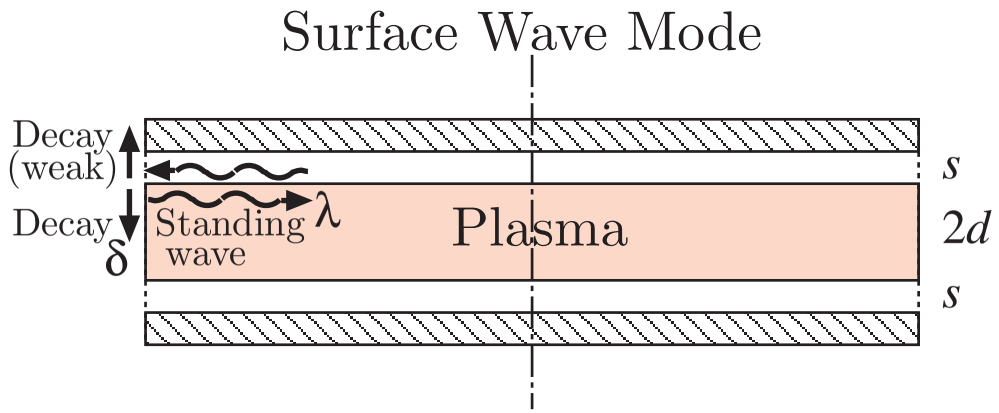


Fields cannot pass through metal plates

(1) V_s excites radially outward wave in top vacuum gap
(2) Outward wave excites radially inward wave in plasma

SURFACE WAVE MODE

- Power enters the plasma via a *surface wave mode:*



- Radial wavelength for surface wave (low density limit):

$$\boxed{\lambda \approx \frac{\lambda_0}{\sqrt{1+d/s}} \sim \frac{\lambda_0}{3}}$$

  with $\lambda_0 = c/f$ the free space wavelength

- Axial skin depth for surface wave:

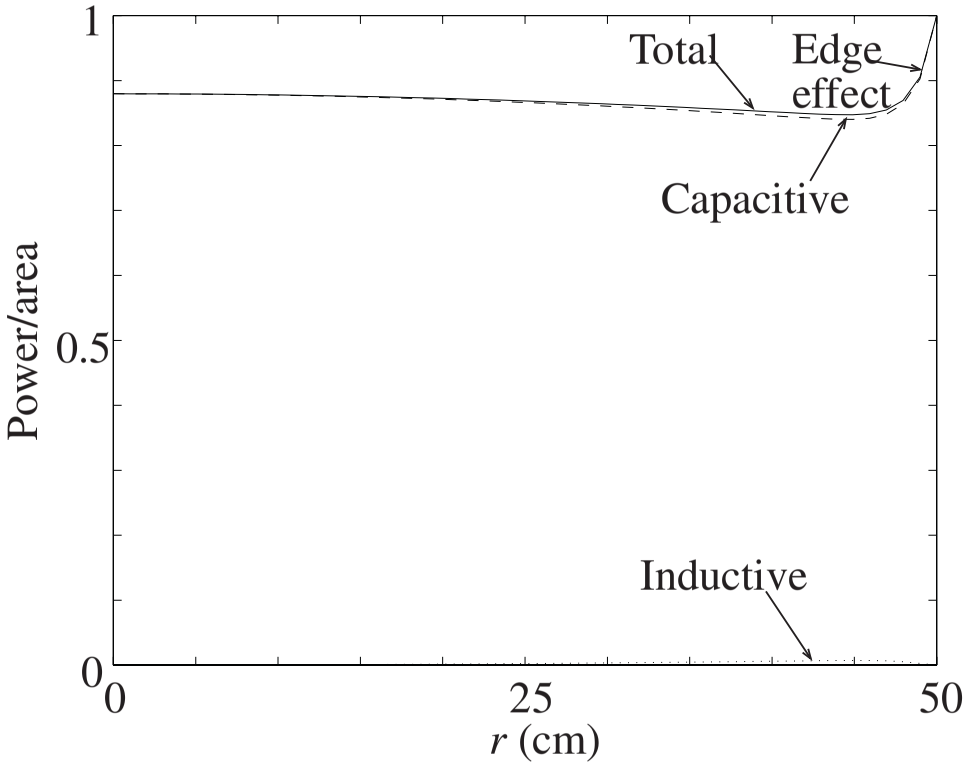
$$\boxed{\delta \sim \frac{c}{\omega_p}}$$

- There are also *evanescent modes* leading to edge effects near $r = R$

STANDING WAVE EFFECT

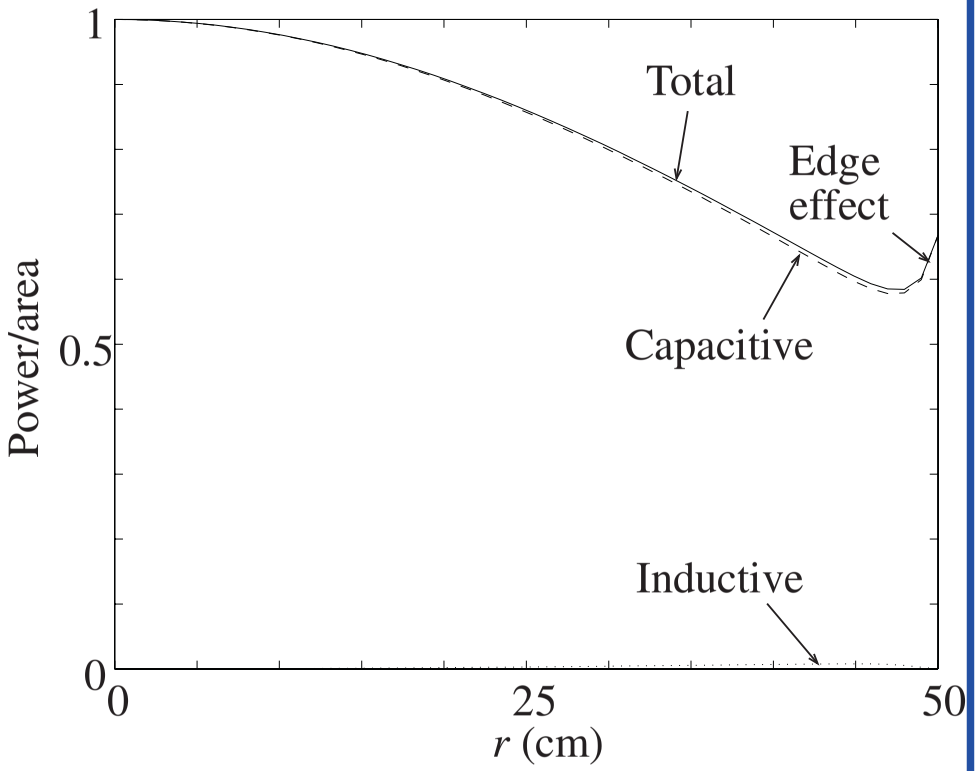
- $R = 50$ cm, $d = 2$ cm, $s = 0.4$ cm, $n_e = 10^9$ cm^{-3}, $\delta \approx 16$ cm
- $P_{\rm cap}$ (dash), $P_{\rm ind}$ (dot) and $P_{\rm tot}$ (solid) as a function of r

13.56 MHz ($\lambda \approx 9$–10 m)



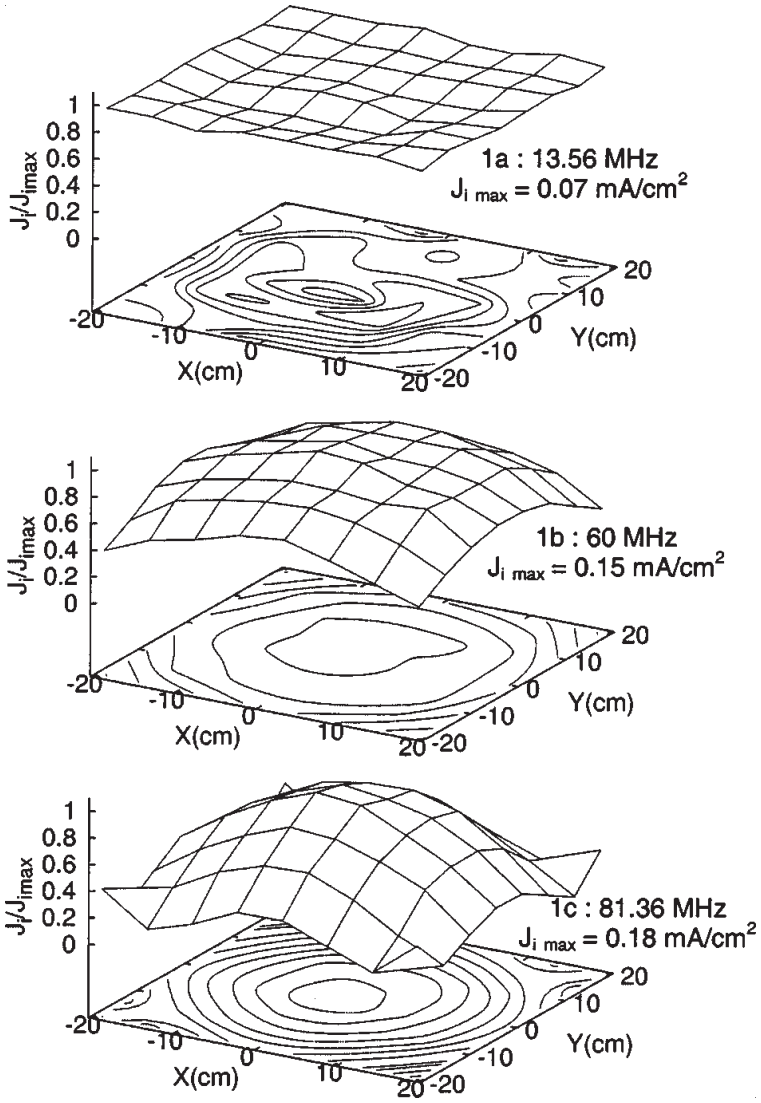
Small standing wave and skin effects

40.7 MHz ($\lambda \approx 3$ m)



Large standing wave effect; center-high profile

EXPERIMENTAL RESULTS FOR STANDING WAVES



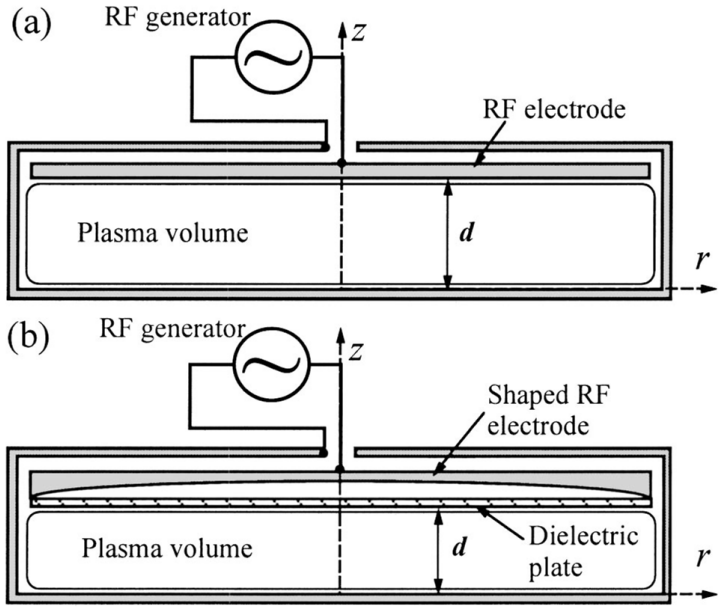
20×20 cm discharge
$p = 150$ mTorr
50 W rf power

The standing wave effect is seen at 60 MHz and is more pronounced at 81.36 MHz

(A. Perret, P. Chabert, J-P Booth, J. Jolly, J. Guillon and Ph. Auvray, *Appl. Phys. Lett.* **83**, 243, 2003)

SUPPRESSION OF STANDING WAVE EFFECTS

- Shaped electrode (and diel plate) eliminate standing wave effects



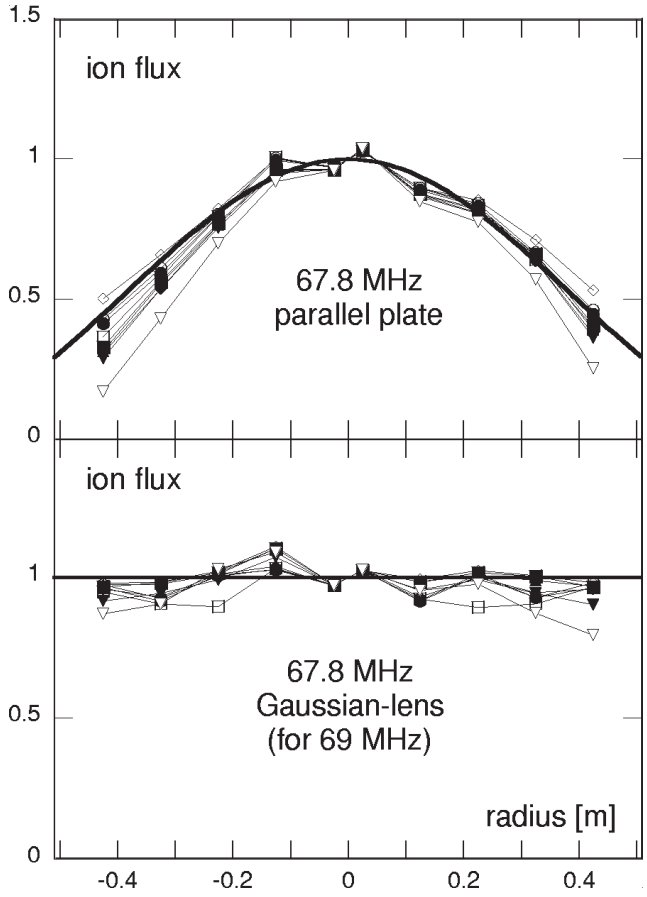
- Increased overall thickness in center compared to edge keeps voltage across discharge section constant
- The electrode shape is a Gaussian, independent of the plasma properties

L. Sansonnens and J. Schmitt, *Appl. Phys. Lett.* **82**, 182 (2003)

P. Chabert, J.L. Raimbault, J.M. Rax, and A. Perret, *Phys. Plasmas* **11**, 4081 (2004)

EXPERIMENTAL CONFIRMATION

- 5–250 mTorr argon, 50–300 W

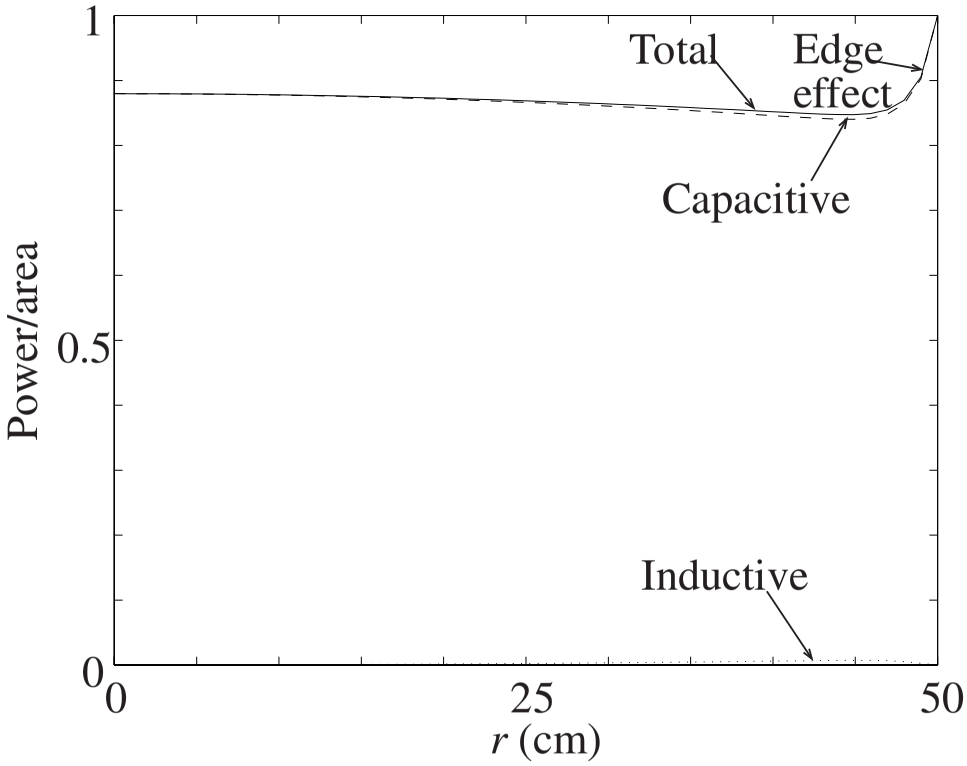


H. Schmitt et al, *J. Appl. Phys.* **95**, 4559 (2004)

SKIN EFFECTS

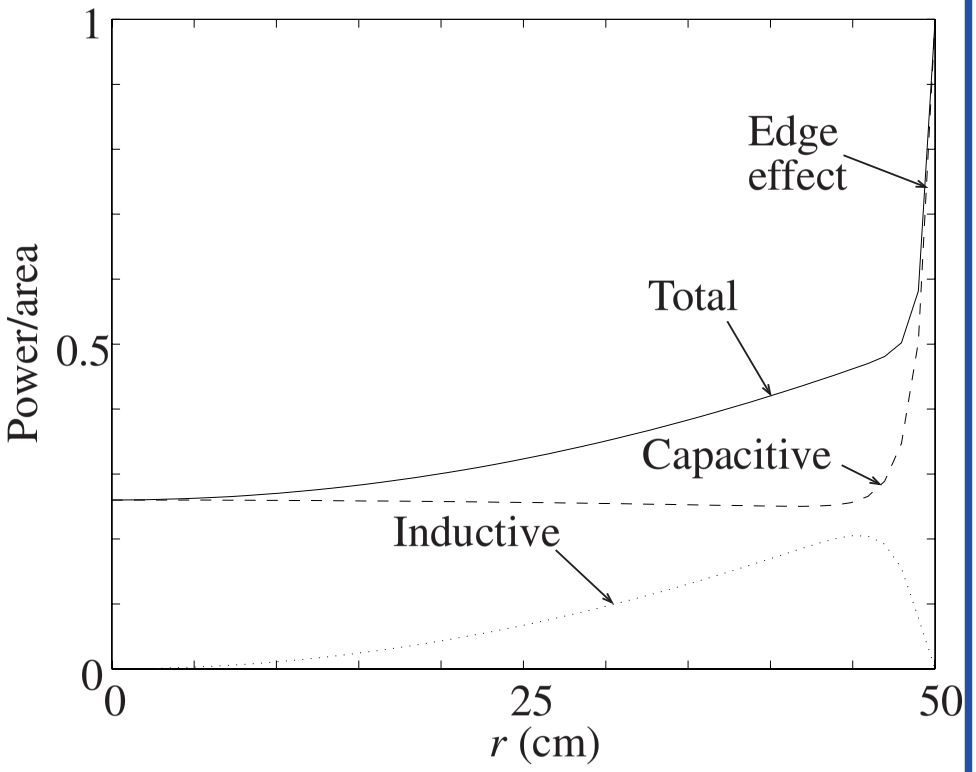
- $R = 50$ cm, $d = 2$ cm, $s = 0.4$ cm, $f = 13.56$ MHz, $\lambda \approx 9$ m
- $P_{\rm cap}$ (dash), $P_{\rm ind}$ (dot) and $P_{\rm tot}$ (solid) as a function of r

$n_e = 10^9$ cm^{-3} ($\delta = 16.7$ cm)



Small standing wave and skin effects

$n_e = 10^{10}$ cm^{-3} ($\delta = 5.3$ cm)



Large skin effects; center-low profile

SKIN EFFECTS

- Skin effects $\Longrightarrow$ radial nonuniformities at high densities when

$$\boxed{\delta \lesssim 0.45\sqrt{d\,R}}$$

$\delta \propto \dfrac{1}{\sqrt{n}}$ = collisional or collisionless skin depth

d = bulk plasma half-thickness

R = discharge radius

- Use 1D transmission line analysis + global (low pressure) or local (high pressure) power balance

$$\boxed{\Longrightarrow \text{self-consistent standing wave/skin effects}}$$

(P. Chabert, J.L. Raimbault, P. Levif, J.M. Rax, and M.A. Lieberman, *Plasma Sources: Sci. Technol.* **15,** S130, 2006)

THE NEXT 15 YEARS AND BEYOND

THE EXPERTS SPEAK[†]

- "There is not the slightest indication that [nuclear] energy will ever be obtained" — *Albert Einstein, 1932*
- "Anyone who expects a source of power from the transformation of these atoms is talking moonshine." — *Ernest Rutherford, 1933*
- "A few decades hence, [when controlled fusion is achieved], energy will be free — just like the unmetered air." — *John von Neumann, 1956*
- "Radio has no future." — *Lord Kelvin, 1897*
- "I think there is a world market for about five computers." — *Thomas J. Watson, 1943*
- Where a calculator like ENIAC is equipped with 18,000 vacuum tubes and weighs 30 tons, computers in the future may have only 1,000 vacuum tubes and perhaps only weigh $1\frac{1}{2}$ tons." — *Popular Mechanics, March 1949*
- "640k ought to be enough for anybody." — *Bill Gates, 1981*

[†] C. Cerf and V. Navasky, Villard, New York, 1998

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS 2005)

Year	2006	2009	2011	2013	2015	2017	2020
Half-pitch (nm)	70	50	40	32	25	20	14
Gate length (nm)	28	20	16	13	10	8	6

- Above limits imposed by thermodynamics and quantum mechanics
- Major issues are transistor physics, materials limitations, and power dissipation
  - Doping profiles, silicon-on-insulator, FinFET's, tri-gate structures
  - High-κ gate dielectrics, metal gates, strained Si, Si-Ge, low-κ interconnect dielectrics
  - Passive heat sunk power limitation of around 200 W/cm^2
- Formidable manufacturing issues remain; eg, lithography, metrology

"You can scale CMOS down another 10–15 years; nothing touches the economics of it." — Intel CEO Craig Barrett

BEYOND 2020

- Moore's law (miniaturization) ends, but products improve for many years
- MOS-FET's continue for fast switches

  Vertical CMOS transistors → silicon/carbon nanowires/nanotubes?
- Copper/low-κ dielectric layers continue for interconnects

  Copper → carbon nanotubes? Optical interconnects?
- CMOS memory migrates to compatible magnetic memory

"Spintronics:" electron charge → electron spin

  Flash (slow) and DRAM (volatile) → MRAM (fast, non-volatile)?

  ⇒ 1st product in 2006: Freescale MRAM (4 Mb, 35 ns)

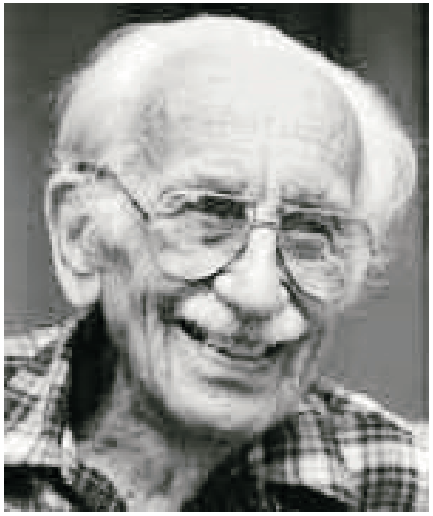
PIE IN THE SKY†

- "3D chips" (heat removal limit of 200 W/cm^2)
- "Single-molecule transistors" (not much smaller than CMOS transistors)
- "Single-electron transistors" (need low temperatures)
- "Cross-bar computing" (replace reliable CMOS switches with defect-prone nanowire switches)
- "Self-assembled, DNA-based computers" (we each own one already)
- "Quantum computing" (exponentially faster computation for niche applications; e.g. codebreaking)

† From a Joe Hill union song, *The Preacher and the Slave*, 1911

CONCLUSIONS

- CMOS scales to 24-atom gate lengths in 2020
- CMOS product improvements continue far beyond 2020
- Plasma reactor research and development will intensify to meet these needs
- Displacing CMOS beyond 2020 is unlikely; other technologies will be integrated into the CMOS platform



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