Joint Impact of Random Variations and RTN on Dynamic Writeability in 28nm Bulk and FDSOI SRAM

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***Abstract*—Improving SRAM minimum operating voltage (V_{min}) in scaled process nodes requires characterization of different failure mechanisms. Persistent errors caused by random variations and intermittent errors caused by random telegraph noise (RTN) both contribute to bitcell failure. Random V_{th} shift was measured for 32,000 in-situ SRAM cells in both 28nm bulk and FDSOI processes due to both random variations and RTN, and dynamic writeability was measured by two different write modes that accentuate different RTN behaviour. Measured distribution parameters of both random variation and RTN were used to calibrate an accelerated Monte Carlo simulation that predicts a V_{min} difference due to RTN. Measurements show that while FDSOI technology reduces random variation by approximately 27% compared to bulk, similar RTN amplitudes slightly increase bitcell susceptibility to failures caused by RTN.**

I. Introduction

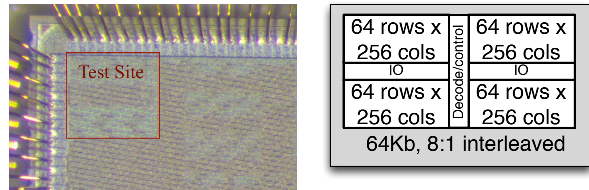
Accurate characterization of cell failures at SRAM V_{min} requires Monte Carlo simulation of devices with calibrated variation models, and simulation predicts that cells with a parametric shift beyond an Nx6-dimensional failure contour will have persistent failures, where each of the N dimensions represents a varying quantity in the cell. Additionally, random telegraph noise (RTN) can cause intermittent failures of usually functional cells, and it has been postulated that scaling will make RTN a more significant source of error [1]. However, the joint effect of RTN and random variation on SRAM failure is still not well understood. This work investigates the validity of the failure contour, and explores the interaction between persistent and intermittent causes of SRAM bitcell failures. Measurements are taken from cells within an SRAM array, not padded-out cells, which enables more sample points and increases certainty that the results will be applicable for production SRAM arrays.

II. Characterization Setup

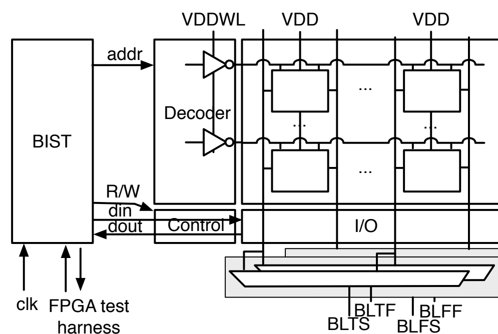
The study is applied to an array of 32k $0.120\mu m^2$ bitcells in a pre-production HKMG 28nm process [2]. Both bulk and FDSOI wafers were manufactured using the same mask set to provide a unique opportunity for comparison between FDSOI and bulk. Bulk and FDSOI have different gate stacks to adjust V_{th}. Figure 1 shows the chip photograph, physical organization, and characterization architecture. A programmable BIST enables dynamic measurements, and separated supplies, combined with a bitline mux, enable static IV measurements similar to [3].

III. Measurement of Random Variations

Threshold voltage variation is measured for every transistor in the SRAM array by using a modification of the direct bit



(a) Chip photo and organization.



(b) Characterization system architecture.

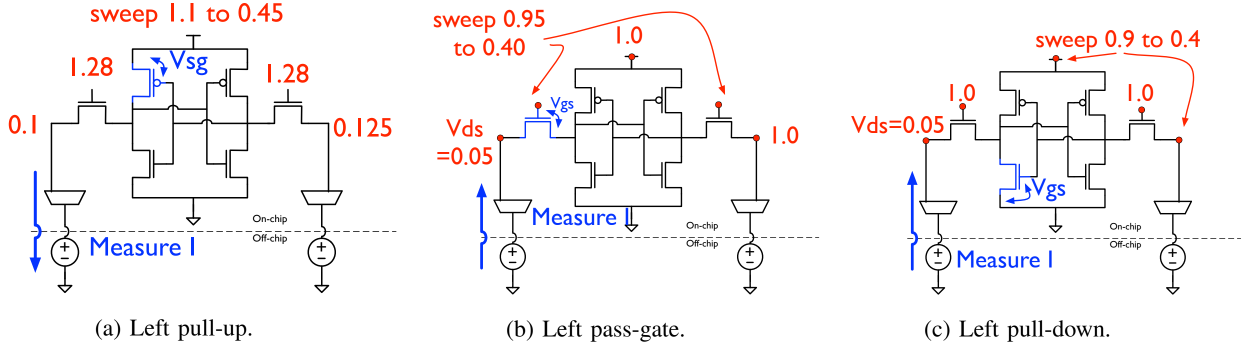
Fig. 1: 28nm characterization testchip details.

transistor access scheme (DBTA) [3]. The exact measurement setup is depicted in Figure 2. Multiplexed bitlines and separated wordline and cell voltages enable IV measurements of every cell in the array.

Figure 3 shows the Gaussian distribution of V_{th} for the pull-up, pass-gate, and pull-down transistors of 32,000 cells. FDSOI devices have approximately 27%, 26%, and 28% lower standard deviation of V_{th} than bulk devices for the pull-up, pass-gate, and pull-down respectively. Because IV measurements are not performed on isolated devices, a transient simulation is performed to provide confidence that the V_{th} measurement of a single transistor is not affected by other transistors in the cell. The simulation netlist represents the actual V_{th} measurement scheme and uses cell V_{th} shifts annotated from actual measured data, and Figure 4 plots the distribution of simulated measurement error of the DBTA scheme.

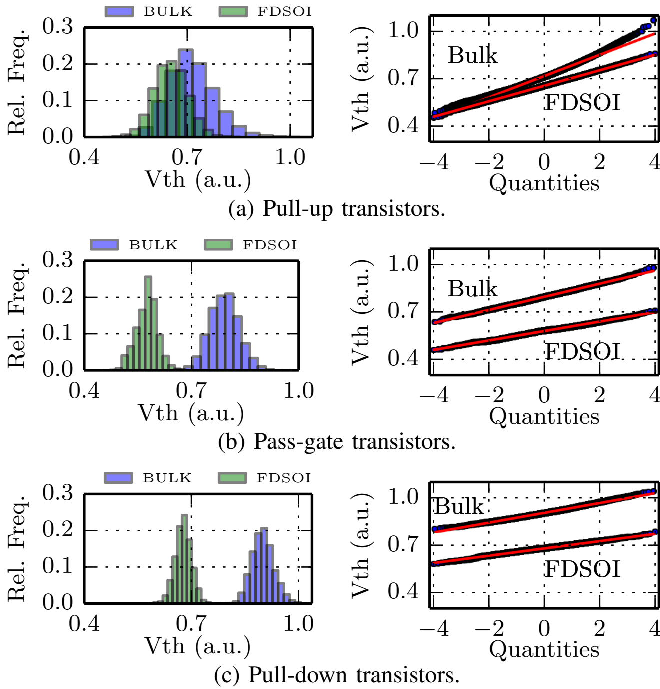
IV. Measurement of Random Telegraph Noise

RTN was measured using the alternating bias technique [4]. Figure 5 provides procedure details, and shows example waveforms of the alternating bias technique versus a traditional RTN measurement. Traditional schemes can find trap emission and capture time constants as a function of gate voltage, but



(a) Left pull-up. (b) Left pass-gate. (c) Left pull-down.

Fig. 2: Scheme used to measure V_{th} of each transistor in the SRAM array.



(a) Pull-up transistors.

(b) Pass-gate transistors.

(c) Pull-down transistors.

Fig. 3: Histogram and normal QQ plots of measured V_{th} distribution for 32k cells from both FDSOI and bulk chips.

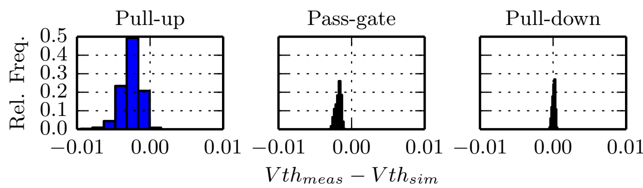


Fig. 4: V_{th} measurement difference between measured V_{th} and simulated scheme using transistor V_{th} shifts from measurement.

require sweeping the gate voltage and long measurement times. The alternating bias technique speeds up the procedure by alternately turning on and off the gate before measurement, which attempts to force either emission or capture before the testing period. While this technique emphasizes worst-case RTN effects, it closely emulates the real operating conditions of a cell, where devices are either turned on or off immediately before an access. The measured amplitude distribution in Figure 6 shows RTN-induced changes in drain current around

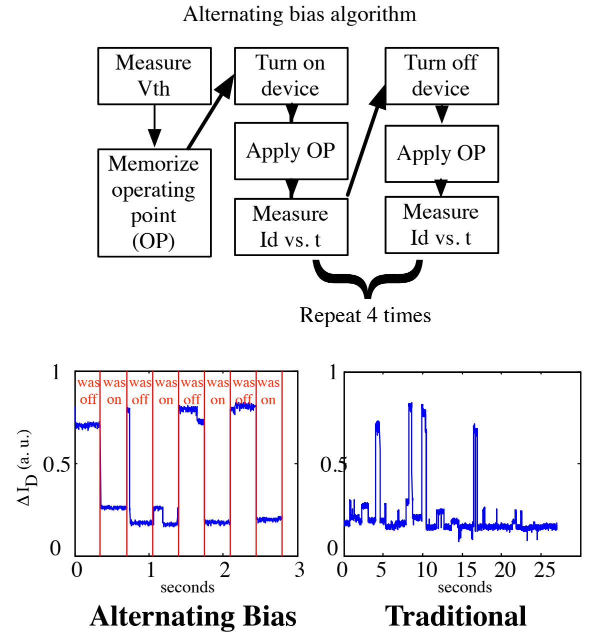


Fig. 5: Alternating bias versus traditional RTN measurement scheme.

the threshold voltage follow a lognormal distribution with a long tail. Both pull-down and pass-gate NMOS devices show similar RTN amplitudes, but for the pull-up PMOS devices, RTN amplitude is slightly higher in FDSOI than in bulk.

V. Simulation-based Writeability Analysis

Monte-Carlo-based measurements can be used to predict the joint effect of random variation and RTN on writeability. To accelerate Monte Carlo analysis of rare events, an importance-sampling based simulation methodology is used [5]. V_{th} shift for each device is equal to the sum of random variation sampled from a normal distribution and RTN sampled from a log-normal distribution. The parameters of these distributions are taken from measured results.

Using the notation in Figure 7, failures to write-1 are caused by weak PDR, PUL, PGL, and PGR combined with strong PDL and PUR. RTN is assumed to only decrease V_{th}, so the best-case RTN effect can be estimated by applying an RTN-induced negative V_{th} shift to PDR, PUL, PGL, and PGR while masking RTN in PDL and PUR. Conversely, the worst case

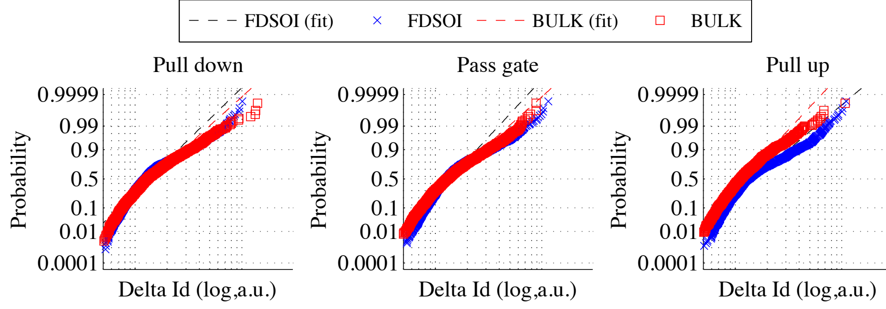


Fig. 6: Lognormal probability plot of RTN-induced current differences at cell V_{th} using the alternating bias technique.

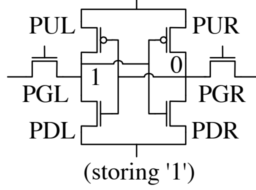


Fig. 7: Transistor naming convention.

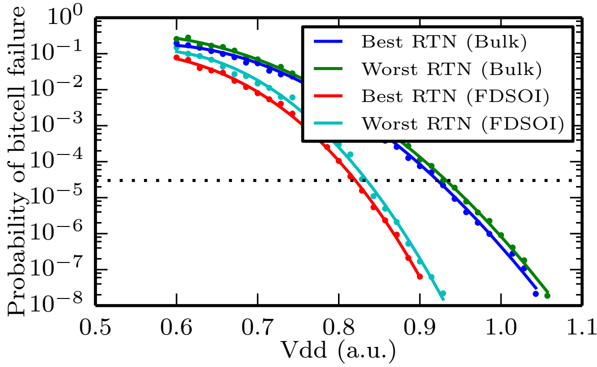


Fig. 8: Simulation of bitcell write failure probability for best and worst case RTN using importance sampling methodology.

RTN effect can be estimated by applying RTN effects to PDL and PUR while masking the other devices. This measure will overestimate RTN effects, because RTN in multiple devices can help and hurt a cell at the same time. While RTN-induced current shift is only measured at cell V_{th}, this strategy assumes that current differences at other voltages are caused by the resulting threshold voltage shift of the device. Figure 8 plots the resulting probability of bitcell failure versus supply voltage from this study. While the decreased random variation standard deviation in FDSOI is the primary influence on V_{min}, RTN causes a small but measurable difference in bitcell V_{min}.

VI. Measurement-based writeability analysis

Measurement results confirm that writeability failures are caused by V_{th} shifts induced by both random variations and RTN. Writeability is measured by initializing a value in a cell at a safe Vdd, writing the opposite value at the test Vdd, then checking for a correct write at a safe Vdd. The ability to write both values is measured for the entire array at decreasing voltages. Figure 9 shows the V_{th} shifts of the first 12 failing cells with arrows indicating the V_{th} shift direction

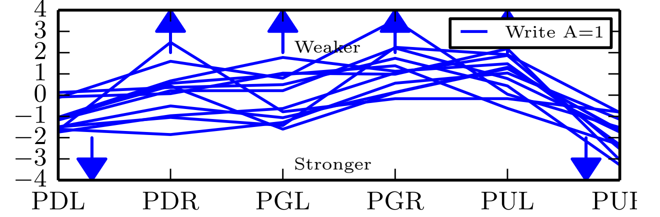


Fig. 9: V_{th} shift vector for cells failing to write 1. Arrows indicate worsening ability to write A=1.

that worsens writeability for each device. Only writeability failures are analyzed, and cells that are unstable at target Vdd are filtered (to avoid simultaneous measurement of a cell's ability to write A without flipping back to $\bar{A}$ during a half-select).

The effect of RTN on dynamic writeability can be measured by applying two different write schemes with opposite resting values that expose different RTN behaviour, as shown in Figure 10 [6]. The dynamic write patterns are exactly the same, so without RTN V_{min} should be exactly the same. However, different resting values force different trap occupancy immediately before the writeability test, which exposes the effect of RTN on writeability. The difference in V_{min} between the single write (SW) mode and write-after-write (WAW) mode will be referred to as V_{diff}. This effect can cause problems for production BIST tests at low voltage, because failures at a specific voltage depend on trap occupancy. Therefore, understanding V_{diff} is required to accurately margin BIST measurements of V_{min}.

Figure 12 shows how RTN causes a V_{min} difference between the two write modes for writing a 1 to a specific bitcell. Random-variation-induced V_{th} shift weakens the cell. Alternating-bias RTN measurements show that when the PDL is left off, it will have a higher current than when it is left on. For the WAW mode, Figure 11 shows that the bitcell holds a 1 for a long period and the PDL is off, so RTN will cause higher current and therefore lower V_{th}, which makes failure in the WAW mode more likely than the SW mode.

The distribution of V_{diff} values for the first 25 failing cells in bulk and FDSOI is shown in Figure 13. Larger V_{min} differences in FDSOI suggest that while RTN ΔI_D amplitude is similar between FDSOI and bulk, the lower standard deviation of the random variation in FDSOI increases RTN's impact on cell failures.

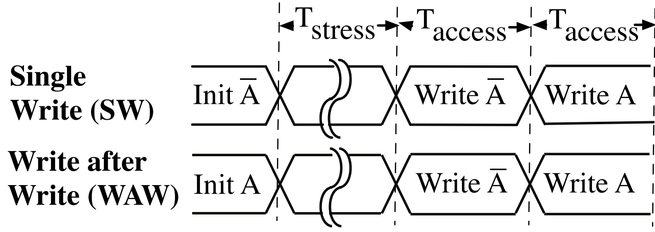


Fig. 10: BIST waveforms of two different writeability tests that expose RTN, where $T_{stress} = 1s$ and $T_{access} = 300ns$ with a 50% duty cycle.

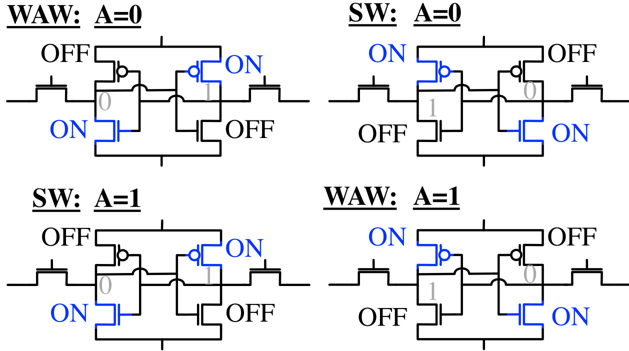


Fig. 11: Transistor stress state for different write modes and values.

The effect of V_{diff} on overall chip V_{min} can be evaluated by counting the number of cells that fail at each voltage for both SW and WAW (no RTN effect) versus the number that fail for either SW or WAW (including RTN). Figure 14 plots the V_{min} difference due to RTN for six different chips normalized to the same voltage. Note that the effect of RTN is suppressed for the entire array because the cells with the largest RTN effect are not necessarily the cells that limit array V_{min}.

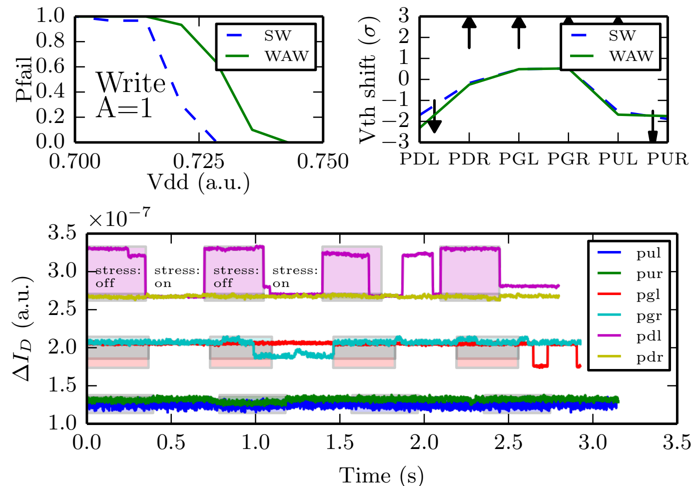


Fig. 12: Example measured effect of RTN on V_{diff} for a specific bitcell.

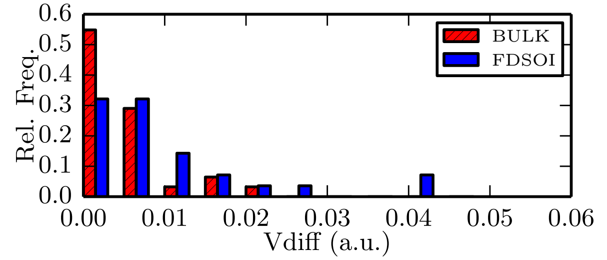


Fig. 13: Distribution of V_{min} difference between write modes.

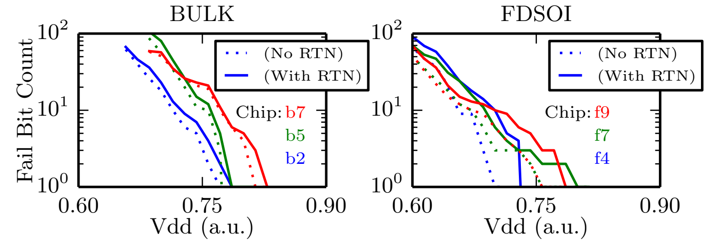


Fig. 14: Difference in V_{min} for six different chips.

VII. Conclusion

Measurement of transistor threshold voltage in 32,000 bitcells shows that FDSOI technology reduces threshold variation due to random variations by 27% compared to bulk. The alternating bias technique reveals similar threshold variation due to RTN in bulk and FDSOI for NMOS devices, and slightly increased RTN amplitude in FDSOI for PMOS devices. Dynamic measurement of writeability in both FDSOI and bulk shows that the decreased random variation in FDSOI enables an approximately 7% reduction in V_{min}, but also exacerbates the effect of RTN on minimum operating voltage failures, suggesting that even as intrinsic channel devices reduce the relative amount of random variation, RTN will emerge as an obstacle to future voltage scaling and increase voltage margins for BIST results.

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