

## **Chenming Hu**

TSMC Distinguished Professor of Microelectronics  
University of California, Berkeley

### **Professional Experiences**

- 1976-Present, Professor of Electrical Engineering, University of California, Berkeley
- 2001-2004, Chief Technology Officer, TSMC (Taiwan Semiconductor Manufacturing Co)
- 1973-1976, Assistant Professor, Massachusetts Institute of Technology

### **Honors and Awards**

- Member, US National Academy of Engineering, 1997-.
- Member, Academia Sinica, Taiwan, 2004-.
- IEEE Jack Morton Award (for contributions to IC reliability physics), 1997.
- IEEE Solid State Circuits Award (for developing world standard transistor model), 2002.
- Berkeley Distinguished Teaching Award (Berkeley's highest honor for teaching), 1999.
- Chancellor's Professor Chair, University of California, Berkeley, 1998-2001.
- TSMC Distinguished Professor Chair, Univ. of California, Berkeley, 2001-present.
- Life Honorary Professor, Chinese Academy of Science, China, 1990-.
- Honorary Professor, National Chiao Tung University, Taiwan, 2001-.
- Fellow, Institute of Electrical and Electronics Engineers, 1989-.
- Fellow, Institute of Physics, 1998-.
- Sigma Xi Moni Ferst Award (for encouragement of research through education), 1998.
- W.Y. Pan Foundation Award (for Distinguished Research), 1999.
- DARPA Most Outstanding Technical Accomplishment Award (for FinFET), 2000.
- R&D100 Award (for BSIM3 as one of the most significant new technologies), 1998.
- IEEE Paul Rappaport Award (best paper in all Electron Devices Society journals), 2003.
- Semiconductor Research Corporation Outstanding Research Award, 1994.
- ISSCC Beatrice Winner Award, 2000.

### **Research Highlights**

Led the development of transistor model, BSIM, which is the international industry standard for circuit simulation and is used in the design of most ICs worldwide with cumulative value of several hundred billion dollars. Contributed widely used IC reliability models (oxide, hot carrier, AC electromigration) and the first IC reliability simulator. Co-developed the FinFET transistor structure, which has set the record of transistor miniaturization and is expected to enable the scaling of transistors through 10nm-gate length. Supervised over 60 Ph.D. theses.

### **Publications**

3 books, 800 research articles, conference keynote or invited talks.

### **Education**

B.S., EE, National Taiwan University, 1968

M.S. and Ph.D., EECS, University of California, Berkeley, 1970 and 1973

### **More Information**

<http://www.eecs.berkeley.edu/~hu/>