Elad Alon

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University of California, Berkeley
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ACADEMIC POSITIONS

7/12 – present ***Associate Professor*** – University of California, Berkeley, CA
Department of Electrical engineering and Computer Sciences

1/07 – 6/12 ***Assistant Professor*** – University of California, Berkeley, CA
Department of Electrical Engineering and Computer Sciences

8/07 – present ***Co-Director*** – Berkeley Wireless Research Center

Research Interests

Summary: Design, optimization, and implementation of energy-efficient integrated systems, including the circuit, device, communications, and optimization techniques used to realize them.
Current projects: nano/micromechanical relay-based circuit design; multi-gigabit-per-second mobile 60GHz wireless transceivers; on-chip power conversion and management; digital RF power amplifiers and transmitters; circuit and system requirements for alternative energy-efficient switching devices; analog/mixed-signal design methodologies; >60Gb/s electrical links; fully integrated mm-wave transceivers for chip-to-chip communications; neural interface circuitry; bio-powered implantable electronic interfaces, electronic wallpaper

Teaching

- *EE141* – Introduction to Digital Integrated Circuits (Fall 07, Fall 08, Fall 09, Fall 10)
- *CS150* – Components and Design Techniques for Digital Systems (Fall 11)
- *EE240* – Advanced Analog Integrated Circuits (Spr 08, Spr 09, Spr 10, Spr 12)
- *EE290C* – High-Speed Electrical Interface Circuit Design (Spr 11)
- *EE301* – Teaching Techniques for Electrical Engineering (Spr 10)

EDUCATION

6/02 – 12/06 **Ph.D.** in Electrical Engineering, Stanford University
9/00 – 6/02 **M.S.** in Electrical Engineering, Stanford University
9/97 – 6/01 **B.S.** with Distinction in Electrical Engineering, Stanford University

PAST EXPERIENCE AND EMPLOYMENT

6/12 – present ***Consultant –*** Cadence Inc., San Jose, CA
Circuit/link architecture definition for 8-10Gb/s SerDes.

3/11 – present ***Consultant –*** Xilinx Inc., San Jose, CA
Design reviews and circuit/link architecture definition for 1-30Gb/s SerDes.

9/10 – present ***Consultant –*** Wilocity, Caesarea, Israel
Design reviews for WiGig multi-Gb/s 65nm CMOS 60GHz phased array transceiver chipset and system. Architecture and technology guidance for future products.

11/08 – present ***Visiting Professor*** – Sun Labs/Oracle Labs, Menlo Park/Redwood Shores, CA
Signaling/clocking circuit architectures and design reviews for ultra-low power, integrated 5-15Gb/s photonic links (DAPRA UNIC program).

5/10 – present ***Consultant –*** Applied Science and Technology Research Institute (ASTRI), Hong Kong, China
Definition, design, and review of clocking circuits and architectures for a 65nm 54GS/s ADC.

SELECTED AWARDS

- IEEE Symposium on VLSI Circuits Best Student Paper Award (2011)
- IEEE International Solid-State Circuits Conference Jack Raper Award for Outstanding Technology Directions Paper (2010)
- Electrical Engineering Division Outstanding Teaching Award (2010)
- Hellman Family Faculty Fund Award (2009)
- IBM Faculty Award (2008)

PUBLICATIONS

Next-Generation Wireless Communications

1. L. Kong and **E. Alon**, "A 21.5mW 10+Gb/s mm-Wave Phased-Array Transmitter in 65nm CMOS," *IEEE Symposium on VLSI Circuits*, Jun. 2012.
2. J.-D. Park, S. Kang, S. Thyagrajan, **E. Alon**, and A. M. Niknejad, "A 260GHz Fully Integrated CMOS Transceiver for Wireless Chip-to-Chip Communication," *IEEE Symposium on VLSI Circuits*, Jun. 2012.
3. D. Yeager, W. Biederman, N. Narevsky, **E. Alon**, and J. Rabaey, "A Fully-Integrated 10.5μW Miniaturized (0.125mm^2) Wireless Neural Sensor," *IEEE Symposium on VLSI Circuits*, Jun. 2012.
4. C. Thakkar, L. Kong, K. Jung, A. Frappe, and **E. Alon**, "A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS," *IEEE Journal of Solid-State Circuits*, Apr. 2012.
5. S. Gambini, J. Crossley, **E. Alon**, and J. Rabaey, "A Fully Integrated, 290pJ/bit UWB Dual-Mode Transceiver for cm-Range Wireless Interconnects," *IEEE Journal of Solid-State Circuits*, Mar. 2012.
6. M. Tabesh, J. Chen, C. Marcu, L.-K. Kong, S. Kang, A. M. Niknejad, and **E. Alon**, "A 65nm CMOS 4-Element Sub-34mW/Element 60GHz Phased-Array Transceiver," *IEEE Journal of Solid-State Circuits*, Dec. 2011.
7. S. Gambini, L. De Nardis, **E. Alon**, and J. Rabaey, "Interference Robust Self-Mixing UWB Systems Using Phase-Domain Spreading," *IEEE International Conference on Ultra Wideband*, Sept. 2011.
8. C. Thakkar, L. Kong, K. Jung, A. Frappe, and **E. Alon**, "A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS," *IEEE Symposium on VLSI Circuits*, Jun. 2011.
   Best Student Paper Award
9. M. Tabesh, J. Chen, C. Marcu, L.-K. Kong, S. Kang, **E. Alon**, and A. M. Niknejad, "A 65nm CMOS 4-Element Sub-34mW/Element 60GHz Phased Array Transceiver," *IEEE International Solid-State Circuits Conference*, Feb. 2011.
10. S. Gambini, J. Crossley, **E. Alon**, and J. Rabaey, "A Fully Integrated, 300pJ/bit, Dual Mode 65nm CMOS Transceiver for cm-Range Wireless Links," *IEEE Symposium on VLSI Circuits*, Jun. 2010.
11. C. Marcu, D. Chowdhury, C. Thakkar, J. Park, L. Kong, M. Tabesh, Y. Wang, A. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, **E. Alon**, and A. M. Niknejad, "A 90nm CMOS Low-Power 60GHz Transceiver with Integrated Baseband Circuitry," *IEEE Journal of Solid-State Circuits*, Dec. 2009.
12. C. Marcu, D. Chowdhury, C. Thakkar, L. Kong, M. Tabesh, J. Park, Y. Wang, A. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, A. M. Niknejad, and **E. Alon**, "A 90nm CMOS Low-Power 60GHz Transceiver with Integrated Baseband Circuitry," *IEEE International Solid-State Circuits Conference*, Feb. 2009.

Nano-Electro-Mechanical Integrated Circuits

13. T.-J. King Liu, L. Hutin, I.-R. Chen, R. Nathanael, Y. Chen, M. Spencer, and **E. Alon**, "Recent Progress and Challenges for Relay Logic Switch Technology," *IEEE Symposium on VLSI Technology*, Jun. 2012.
14. J. Jeon, L. Hutin, R. Jetvic, N. Liu, Y. Chen, R. Nathanael, W. Kwon, M. Spencer, **E. Alon**, B. Nikolic, and T.-J. King Liu, "Multiple-Input Relay Design for More Compact Implementation of Digital Logic Circuits," *IEEE Electron Device Letters*, Feb. 2012.
15. Y. Lin, T. Riekkinen, W.-C. Li, **E. Alon**, and C. T.-C. Nguyen, "A Metal Micromechanical Resonant Switch for On-Chip Power Applications," *IEEE International Electron Devices Meeting*, Dec. 2011.
16. H. Kam, T.-J. King Liu, V. Stojanovic, D. Markovic, and **E. Alon**, "Design, Optimization, and Scaling of MEM Relays for Ultra-Low Power Digital Logic," *IEEE Transactions on Electron Devices*, Jan. 2011.

17. M. Spencer, F. Chen, C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. King Liu, D. Markovic, **E. Alon**, and V. Stojanovic, "Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications," *IEEE Journal of Solid-State Circuits*, Jan. 2011.
18. H. Kam, **E. Alon**, and T.-J. King Liu, "A Predictive Contact Reliability Model for MEM Logic Switches," *IEEE International Electron Devices Meeting*, Dec. 2010.
19. T.-J. King Liu, J. Jeon, R. Nathanael, H. Kam, V. Pott, and **E. Alon**, "Prospects for MEM Logic Switch Technology," *IEEE International Electron Devices Meeting*, Dec. 2010.
20. V. Pott, H. Kam, R. Nathanael, J. Jeon, **E. Alon**, and T.-J. King Liu, "Mechanical Computing Redux: Relays for Integrated Circuit Applications," *Proceedings of the IEEE*, Dec. 2010.
21. H. Fariborzi, M. Spencer, V. Karkare, J. Jeon, R. Nathanael, C. Wang, F. Chen, H. Kam, V. Pott, T.-J. King Liu, **E. Alon**, V. Stojanovic, and D. Markovic, "Analysis and Demonstration of MEM-Relay Power Gating," *IEEE Custom Integrated Circuits Conference*, Sept. 2010.
22. J. Jeon, V. Pott, H. Kam, R. Nathanael, **E. Alon**, and T.-J. King Liu, "Seesaw Relay Logic and Memory Circuits," *IEEE Journal of Microelectromechanical Systems*, Aug. 2010.
23. R. Nathanael, V. Pott, H. Kam, J. Jeon, **E. Alon**, and T.-J. King Liu, "Four-Terminal-Relay Body Biasing Schemes for Complementary Logic Circuits," *IEEE Electron Device Letters*, Aug. 2010.
24. J. Jeon, V. Pott, H. Kam, R. Nathanael, **E. Alon**, and T.-J. King Liu, "Perfectly Complementary Relay Design for Digital Logic Applications," *IEEE Electron Device Letters*, Apr. 2010.
25. F. Chen, M. Spencer, R. Nathanael, C. Wang, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. King Liu, D. Markovic, V. Stojanović, and **E. Alon**, "Demonstration of Integrated Micro-Electro-Mechanical (MEM) Switch Circuits for VLSI Applications," *IEEE International Solid-State Circuits Conference*, Feb. 2010.
Jack Raper Award for Outstanding Technology Directions Paper
26. H. Kam, V. Pott, R. Nathanael, J. Jeon, **E. Alon**, and T.-J. King Liu, "Design and Reliability of a Micro-Relay Technology for Zero-Standby Power Digital Logic Applications," *IEEE International Electron Devices Meeting*¸ Dec. 2009.
27. F. Chen, H. Kam, D. Markovic, T.-J. King Liu, V. Stojanović, and **E. Alon**, "Integrated Circuit Design with NEM Relays," *IEEE International Conference on Computer-Aided Design*, Nov. 2008.

Mixed-Signal Building Blocks

28. W. Biederman, D. Yeager, **E. Alon**, and J. Rabaey, "A CMOS Switched-Capacitor Bandgap Reference," *IEEE Custom Integrated Circuits Conference*, Sept. 2012.
29. D. Chowdhury, S. Thyagarajan, L. Ye, **E. Alon**, and A. M. Niknejad, "A Fully Integrated Efficient CMOS Inverse Class-D Power Amplifier for Digital Polar Transmitters," *IEEE Journal of Solid-State Circuits*, May 2012.
30. T. Naing, T. O. Rocheleau, Z. Ren, **E. Alon**, and C. T.-C. Nguyen, "Vibration-Insensitive 61-MHz Micromechanical Disk Reference Oscillator," *IEEE International Frequency Control Symposium*, May 2012.
31. L. Kong, Y. Lu, and **E. Alon**, "A Multi-GHz Area-Efficient Comparator with Dynamic Offset Cancellation," *IEEE Custom Integrated Circuits Conference*, Sept. 2011.
32. D. Chowdhury, L. Ye, **E. Alon**, and A. M. Niknejad, "An Efficient Mixed-Signal 2.4GHz Polar Power Amplifier in 65nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, Aug. 2011.
33. D. Chowdhury, S. V. Thyagarajan, L. Ye, **E. Alon**, and A. M. Niknejad, "A Fully-Integrated Efficient CMOS Inverse Class-D Power Amplifier for Digital Polar Transmitters," *IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2011.
34. J. Crossley, E. Naviasky, and **E. Alon**, "An Energy-Efficient Ring-Oscillator Digital PLL," *IEEE Custom Integrated Circuits Conference*, Sept. 2010.
35. D. Chowdhury, L. Ye, **E. Alon**, and A. M. Niknejad, "A 2.4GHz Mixed-Signal Polar Power Amplifier with Low-Power Integrated Filtering in 65nm CMOS," *IEEE Custom Integrated Circuits Conference*, Sept. 2010.
36. **E. Alon**, J. Kim, S. Pamarti, K. Chang, and M. Horowitz, "Replica Compensated Linear Regulators for Supply-Regulated Phase-Locked Loops," *IEEE Journal of Solid-State Circuits*, Feb. 2006.

Power Delivery and Integrated Regulation

37. H.-P. Le, S. Sanders, and **E. Alon**, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," *IEEE Journal of Solid-State Circuits*, Sept. 2011.
38. M. Seeman, V. Ng, H.-P. Le, M. John, **E. Alon**, and S. Sanders, "A Comparative Analysis of Switched-Capacitor and Inductor-Based DC-DC Conversion Technologies," *IEEE Workshop on Control and Modeling for Power Electronics*¸ Jun. 2010.
39. H.-P. Le, M. Seeman, S. Sanders, V. Sathe, S. Naffziger, and **E. Alon**, "A 32nm Fully-Integrated Reconfigurable Switched-Capacitor DC-DC Converter Delivering 0.55W/mm^2 at 81% Efficiency," *IEEE International Solid-State Circuits Conference*, Feb. 2010.
40. **E. Alon**, V. Abramzon, B. Nezamfar, and M. Horowitz, "On-Die Power Supply Noise Measurement Techniques," *IEEE Transactions on Advanced Packaging*, May 2009.
41. **E. Alon** and M. Horowitz, "Integrated Regulation for Energy-Efficient Digital Circuits," *IEEE Journal of Solid-State Circuits*, Aug. 2008.
42. **E. Alon** and M. Horowitz, "Integrated Regulation for Energy-Efficient Digital Circuits," *IEEE Custom Integrated Circuits Conference*, Sept. 2007.
43. S. Naffziger, B. Stackhouse, T. Grutkowski, D. Josephson, J. Desai, **E. Alon**, and M. Horowitz, "The Implementation of a 2-core, Multi-Threaded Itanium Family Processor," *IEEE Journal of Solid-State Circuits*, Jan. 2006.
44. V. Abramzon, **E. Alon**, B. Nezamfar, and M. Horowitz, "Scalable Circuits for Supply Noise Measurement," *IEEE European Solid-State Circuits Conference*, Sept. 2005.
45. **E. Alon**, V. Stojanovic, and M. A. Horowitz, "Circuits and Techniques for High-Resolution Measurement of On-Chip Power Supply Noise," *IEEE Journal of Solid-State Circuits*, April 2005.
46. **E. Alon**, V. Stojanovic, and M. Horowitz, "Circuits and Techniques for High-Resolution Measurement of On-chip Power Supply Noise," *IEEE Symposium on VLSI Circuits*, June 2004.

Circuit and System Requirements for Alternative Switching Devices

47. H. Kam, T.-J. King Liu, and **E. Alon**, "Design Requirements for Steeply Switching Logic Devices," *IEEE Transactions on Electron Devices*, Feb. 2012.
48. H. Kam, T.-J. King Liu, **E. Alon**, and M. Horowitz, "Circuit-Driven Requirements for MOSFET-Replacement Devices," *IEEE International Electron Devices Meeting*¸ Dec. 2008.

High-Speed Electrical and Optical Links

49. Y. Lu, K. Jung, Y. Hidaka, and **E. Alon**, "A 10Gb/s 10mW 2-Tap Reconfigurable Pre-Emphasis Transmitter in 65nm CMOS," *IEEE Custom Integrated Circuits Conference*, Sept. 2012.
50. F. Liu, D. Patil, J. Lexau, P. Amberg, J. Gainsley, H. F. Moghadam, X. Zheng, J. E. Cunningham, A. V. Krishnamoorthy, **E. Alon**, and R. Ho, "10 Gbps, 5.3mW Optical Transceiver Circuits in 40nm CMOS," *IEEE Journal of Solid-State Circuits*, Sept. 2012.
51. J. Savoj, K. Hsieh, P. Upadhyaya, F.-T. An, A. Bekele, S. Chen, X. Jiang, K. W. Lai, C.-F. Poon, A. Sewani, D. Turker, K. Venna, D. Wu, B. Xu, **E. Alon**, and K. Chang, "A Wide Common-Mode Fully-Adaptive Multi-Standard 12.5Gb/s Backplane Transceiver in 28nm CMOS," *IEEE Symposium on VLSI Circuits*, Jun. 2012
52. P. Amberg, F. Liu, M. Dayringer, J. Lexau, D. Patil, J. Gainsley, H. F. Moghadam, **E. Alon**, X. Zheng, J. E. Cunningham, A. V. Krishnamoorthy, R. Ho, "Digitally-Assisted Analog Circuits for a 10Gbps, 395fJ/b Optical Receiver in 40nm CMOS," *IEEE Asian Solid-State Circuits Conference*, Nov. 2011
53. K. Jung, Y. Lu, and **E. Alon**, "Power Analysis and Optimization for High-Speed I/O Transceivers," *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 2011.
54. F. Liu, D. Patil, J. Lexau, P. Amberg, M. Dayringer, J. Gainsley, H. Moghadam, X. Zheng, J. Cunningham, A. Krishnamoorthy, **E. Alon**, and R. Ho, "10Gbps, 530fJ/bit Optical Transceiver Circuits in 40nm CMOS," *IEEE Symposium on VLSI Circuits*, Jun. 2011.
55. X. Zheng, D. Patil, J. Lexau, F. Liu, G. Li, H. Thacker, Y. Luo, I. Shubin, J. Li, J. Yao, P. Dong, D. Feng, M. Asghari, T. Pinguet, A. Mekis, P. Amberg, M. Dayringer, J. Gainsley, H. Moghadam, **E. Alon**, K. Raj, R. Ho, J. Cunningham, A. Krishnamoorthy, "Ultra-Efficient 10Gb/s Hybrid Integrated Silicon Photonic Transmitter and Receiver," *Optics Express*, vol. 19, no. 6, Mar. 2011.

56. T. Ali, D. Patil, F. Liu, **E. Alon**, J. Lexau, C.-K. K. Yang, and R. Ho, "Clocking Links in Multi-Chip Packages: A Case Study," *IEEE Symposium on High Performance Interconnects (HOTI)*, Aug. 2010.
57. R. Ho, F. Liu, D. Patil, X. Zheng, G. Li, I. Shubin, **E. Alon**, J. Lexau, H. Schwetman, and J. Cunningham, "Optical Interconnect for High-End Computer Systems," *IEEE Design and Test of Computers*, Jul. 2010.
58. X. Zheng, F. Liu, D. Patil, H. Thacker, Y. Luo, T. Pinguet, A. Mekis, J. Yao, G. Li, J. Shi, K. Raj, J. Lexau, **E. Alon**, R. Ho, J. Cunningham, A. Krishnamoorthy, "A Sub-Picojoule-per-Bit CMOS Photonic Receiver for Densely Integrated Systems," *Optics Express*, vol. 18, no. 1, Jan. 2010.
59. R. Ho, J. Lexau, F. Liu, D. Patil, R. Hopkins, **E. Alon**, N. Pinckney, P. Amberg, X. Zheng, J. Cunningham, and A. Krishnamoorthy, "Circuits for Silicon Photonics on a Macrochip," *IEEE Asian Solid-State Circuits Conference*, Nov. 2009.
60. C. Werner, C. Høyer, A. Ho, M. Jeeradit, F. Chen, B. Garlepp, W. Stonecypher, S. Li, A. Bansal, A. Agarwal, **E. Alon**, V. Stojanovic, and J. Zerbe, "Modeling, Simulation, and Design of a Multi-Mode 2-10 Gb/sec Fully Adaptive Serial Link System," *IEEE Custom Integrated Circuits Conference*, Sept. 2005.
61. V. Stojanovic, A. Ho, B. Garlepp, F. Chen, J. Wei, G. Tsang, **E. Alon**, R. Kollipara, C. Werner, J. Zerbe, and M. A. Horowitz, "Autonomous Dual-Mode (PAM2/4) Serial Link Transceiver with Adaptive Equalization and Data Recovery," *IEEE Journal of Solid-State Circuits*, April 2005.
62. K. Chang, S. Pamarti, K. Kaviani, **E. Alon**, X. Shi, T. Shin, J. Shen, G. Yip, C. Madden, R. Schmitt, C. Yuan, F. Assaderaghi, and M. Horowitz, "Clocking and Circuit Design for a Parallel I/O on a First Generation CELL Processor," *IEEE International Solid-State Circuits Conference*, Feb. 2005.
63. V. Stojanovic, A. Ho, B. Garlepp, F. Chen, J. Wei, **E. Alon**, C. Werner, J. Zerbe, and M. A. Horowitz, "Adaptive Equalization and Data Recovery in a Dual-Mode (PAM2/4) Serial Link Transceiver," *IEEE Symposium on VLSI Circuits*, June 2004.
64. A. Ho, V. Stojanovic, F. Chen, C. Werner, G. Tsang, **E. Alon**, R. Kollipara, J. Zerbe, and M. A. Horowitz, "Common-mode Backchannel Signaling System for Differential High-speed Links," *IEEE Symposium on VLSI Circuits*, June 2004.

Miscellaneous

65. B. Nezamfar, **E. Alon**, and M. Horowitz, "Energy-Performance Tunable Logic," *IEEE Journal of Solid-State Circuits*, Sept. 2009.
66. M. Horowitz, D. Stark, and **E. Alon**, "Digital Circuit Design Trends," *IEEE Journal of Solid-State Circuits*, Apr. 2008.
67. M. Horowitz, **E. Alon**, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, "Scaling, Power, and the Future of CMOS," *IEEE International Electron Devices Meeting*, Dec. 2005.
68. K. Mai, R. Ho, **E. Alon**, D. Liu, Y. Kim, D. Patil, and M. Horowitz, "Architecture and Circuit Techniques for a 1.1GHz 16Kb Reconfigurable Memory in 0.18μm CMOS," *IEEE Journal of Solid-State Circuits*, Jan. 2005.
69. **E. Alon**, V. Stojanovic, J. M. Kahn, S. Boyd, and M. Horowitz, "Equalization of Modal Dispersion in Multimode Fiber Using Spatial Light Modulators," *IEEE Global Telecommunications Conference*, Nov. 2004.
70. K. Mai, R. Ho, **E. Alon**, D. Liu, Y. Kim, D. Patil, and M. Horowitz, "Architecture and Circuit Techniques for a Reconfigurable Memory Block," *IEEE International Solid-State Circuits Conference*, Feb. 2004.

GRADUATE STUDENT AND POST-DOCTORAL SCHOLAR SUPERVISION

Current

- Artemy Baxansky, Ph.D. in EECS (2011 – present)
- Jethro Beekman, Ph.D. in EECS (2011 – present)
- John Crossley, Ph.D. in EECS (2007 – present)
- Yida Duan, Ph.D. in EECS (2007 – present), co-advised with Prof. Bernhard Boser
- Jaeduk Han, Ph.D. in EECS (2012 – present)
- Kwangmo Jung, Ph.D. in EECS (2008 – present)
- Lingkai Kong, Ph.D. in EECS (2007 – present)
- Hanh-Phuc Le, Ph.D. in EECS (2007 – present), co-advised with Prof. Seth Sanders
- Yue Lu, Ph.D. in EECS (2008 – present)
- Thura Naing, Ph.D. in EECS (2008 – present), co-advised with Prof. Clark Nguyen

- Rachel Nancollas, Ph.D. in EECS (2011 – present)
- Hoai Chau Nguyen Van, Ph.D. in EECS (2011 – present)
- Dongjin Seo, Ph.D. in EECS (2011 – present)
- Matthew Spencer, Ph.D. in EECS (2008 – present)
- Chintan Thakkar, Ph.D. in EECS (2007 – present, completed M.S. Dec. 2010)
- Bonjern Yang, Ph.D. in EECS (2012 – present)

Former
- Antoine Frappe, post-doctoral scholar (2008 – 2009), now Associate Professor at Univ. of Lille
- Abhinav Gupta, M.S. in EECS (graduated May 2009), now with Microsoft
- Robert Kong, M.S. in EECS (graduated Aug. 2010), now with Xilinx
- Kyoohyun Noh, M.S. in EECS (graduated May 2010), now with Texas A&M

PROFESSIONAL ACTIVITES

Editorial Boards and Conference Committees

- *Member*, Technical Program Committee, Wireline Sub-Committee – IEEE International Solid-State Circuits Conference (2013)
- *General Co-Chair* – IEEE Frontiers in Analog Circuit (FAC) Synthesis and Verification (2013)
- *Member*, Organizing and Technical Program Committees, International Workshop on Power-Supply-on-Chip (2012)
- *Associate Editor* – IEEE Transactions on Very Large Scale Integration Systems (Jan. 2011 – present)
- *Member*, Technical Program Committee, Wireline Sub-Committee – IEEE Custom Integrated Circuits Conference (2011, 2012)
- *Organizer*, "Package Scale Power Management" Tutorial – IEEE HotChips (2011)
- *Member*, Technical Program Committee – IEEE International Symposium on Low Power Electronics and Design (2009, 2010, 2011)
- *Program Co-Chair* – IEEE Workshop on Interconnections within High Speed Digital Systems (2009)
- *Member*, Technical Program Committee – IEEE International Conference on Computer Aided Design (2008)

Reviewing Activities (Journals and Conferences)

IEEE Journal of Solid-State Circuits; IEEE Transactions on Very Large Scale Integration Systems; IEEE Transactions on Circuits and Systems I and II; IEEE Transactions on Electron Devices; IEEE Transactions on Advanced Packaging; IEEE Transactions on Nanotechnology; IET Circuits, Devices, and Systems, IEEE International Solid-State Circuits Conference, IEEE Symposium on VLSI Circuits, IEEE Custom Integrated Circuits Conference, ACM Journal of Emerging Computing Technologies

Other Professional Society Service

Representative for the IEEE Solid-State Circuits Society AdCom to the Nanotechnology Council (2009 – present)