UPDATE Problem 4: R_s changed!

Midterm Practice (optional, similar problems will be on the midterm). Solutions available in office hours and on bspace 10/17/2012.

Midterm:

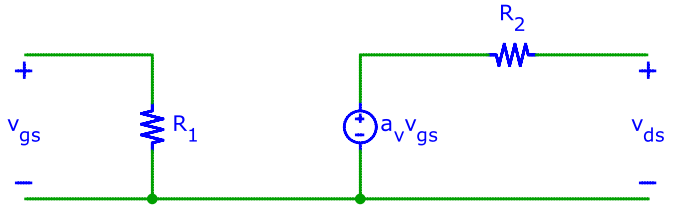
- Open-book, one 8.5 by 11 inch page of handwritten notes (two sided)
- Write all your work and answers on the exam sheet
- Clearly mark results with a box around them
- Show your work (large and small-signal circuit diagrams, design equations)
- ~~Cross out incorrect answers.~~ If you present two or more inconsistent answers we invariably grade the wrong one.
- All problems have equal weight.
- Notation: $V_x = V_X + v_x$, where V_X is the large signal bias and v_x is the small signal value.
- The math is trivial for all problems on the midterm, if approached correctly. This is not a course about complicated algebra and calculus!

Use the following parameters in all problems, unless otherwise specified:

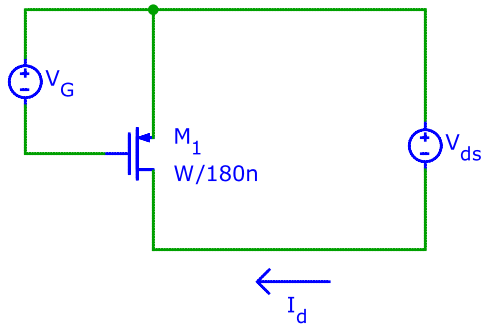
Device	Parameter values
BJT	$I_s = 1\,\text{fA}$, $\beta = 100$, and $V_A = 100\,\text{V}$
NMOS	$\lvert V_{TH}\rvert = 400\,\text{mV}$, $\mu_n C_{ox} = 200\,\mu\text{A/V}^2$, $\lambda = 0.02\,\text{V}^{-1}$, $\gamma = 0\,\text{V}$.
PMOS	$\lvert V_{TH}\rvert = 400\,\text{mV}$, $\mu_p C_{ox} = \mathbf{100}\,\mu\text{A/V}^2$, $\lambda = 0.02\,\text{V}^{-1}$, $\gamma = 0\,\text{V}$.

Unless otherwise specified, assume room temperature and $V_t = 25\,\text{mV}$.

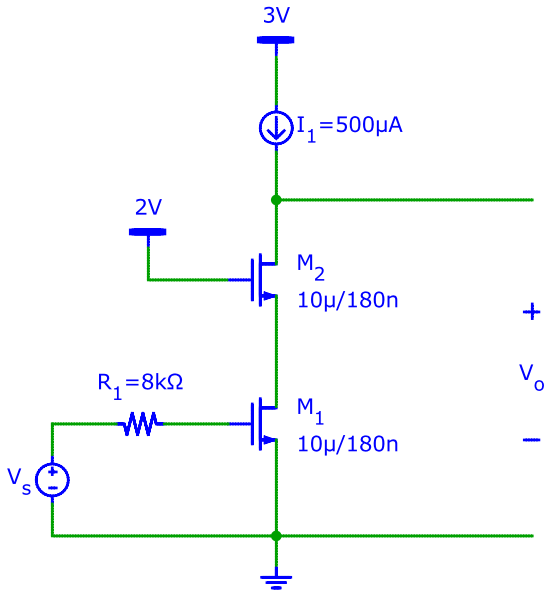
1. The circuit below shows a proposed small-signal model for an MOS transistor biased in the linear (triode) region. Determine all component values from the large signal parameters (I_D, V_{DS}, ...) and transistor characteristics.



2. MOS transitors can be (and often are!) used as resistors. Determine W such that the large-signal channel resistance $R_{DS} = |V_{DS}/I_D| = 10\,\text{k}\Omega$ for $V_{DS} = 1\,\text{V}$ and $V_{GS} = 3\,\text{V}$. What is the value of the small-signal channel resistance $r_{ds} = |v_{ds}/i_d|$?



3. Calculate the small-signal voltage gain $a_v = v_o/v_s$ and small-signal output resistance at port V_o of the circuit below.



4. Design a circuit such that $a_v = v_o/v_s = 1\,(\pm 2\,\%)$ using a single NPN transistor and as many resistors and (ideal) bias sources (current or voltage) as you like (fewer is better and helps avoid mistakes). The value of R_s varies in the range $1 \ldots 6\,\mathrm{k\Omega}$ and $R_L = 5\,\mathrm{k\Omega}$. Stay close to the minimum power dissipation (not more than 2x).

   Use the following sequence (you may need to iterate):

   a) Determine the type of amplifier configuration (CE, CB, CC) best suited for this problem.
   b) Draw a prototype large signal model including all biasing elements. You may need to iterate, e.g. modify or add biasing elements during the design process.
   c) Draw the small-signal diagram and determine the small-signal parameters required to meet the specifications.
   d) Calculate the large signal parameters including the values of all bias sources.
   e) Verify that your circuit meets the specifications.