Due in the "EE 105 box" near 125 Cory Hall by 5pm on Friday 10/5/2012.

Attention: If an assignment (like this one) asks for simulations, you will receive no credit for the entire homework if you do not turn in simulation results.

1. Do the Exercise after Example 5.10 in B. Razavi: Fundamentals of Microelectronics.

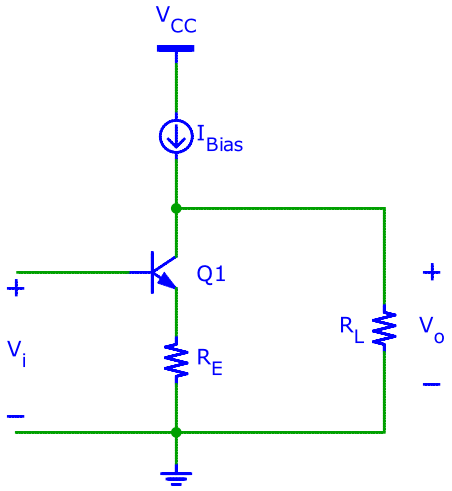
2. Do the Exercise after Example 5.13 in B. Razavi: Fundamentals of Microelectronics.

3. Do the Exercise after Example 5.24 in B. Razavi: Fundamentals of Microelectronics.

4. Do the Exercise after Example 5.46 in B. Razavi: Fundamentals of Microelectronics.

5. a) Calculate the small signal voltage gain $a_v = v_o/v_i$, input resistance R_i, and output resistance R_o for the circuit below. Assume the circuit is biased such that $V_O = V_{cc}/2$.
   Note: since $R_L \to \infty$ in this example, the approximation $r_o \gg R_L$ does not hold! See the textbook or posting "Approximations" on the course web for more on this.
   b) Verify your result with a circuit simulator. Submit a printout of the schematic diagram (or netlist), the output from the operating point analysis (mark the bias point values with a red box), and the output from the DC transfer function analysis. Comment on any discrepancies in excess of 10 % between your hand analysis and the simulation.
   Suggestions: Model I_{Bias} with an ideal current source and check "models an active current source" under the advanced tab. This prevents V_o from reaching kV during the DC sweep analysis. The the LTSpice document on the course website shows an example of a DC transfer function analysis.

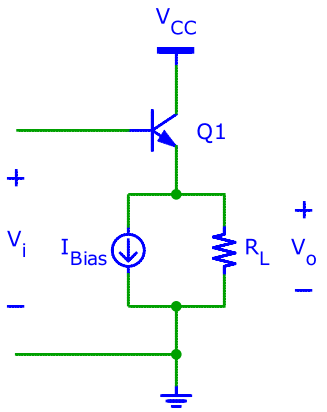
   Use $V_{cc} = 5\,\text{V}$, $I_{Bias} = 100\,\mu\text{A}$, $R_E = 2\,\text{k}\Omega$, $R_L \to \infty$, $I_s = 1\,\text{fA}$, $\beta = 100$, and $V_A = 100\,\text{V}$.



6. Problem 5.70 in B. Razavi: Fundamentals of Microelectronics.

7. The circuit below is called a common-collector stage. It is also known as emitter-follower. After solving the problem, the second name will make sense.
   a) Derive analytical expressions for the small-signal input resistance R_i at port V_i and the small signal voltage gain $a_v = v_o/v_i$ as a function of R_L, g_m, and r_π (assume $r_o \to \infty$).
   b) Design a buffer amplifier with $a_v \geq 0.99$ for $R_L = 10\,\text{k}\Omega$ that dissipates minimum power. Determine g_m, then calculate the corresponding values of I_C, and R_i.
   In the context of circuit design specifications, greater or equal means: the specification (i.e. equality) must be met under all circumstances, but you don't get credit for exceeding it. In fact, often you will be punished (i.e. your competitor gets all the sales or you get points taken off) if you exceed specification e.g. if your circuit dissipates more power than required since it exceeds the specification.
   In this assignment you simply try not to overdesign by a large margin. Keep in mind that getting within 10 … 20 % of the minimum power dissipation is usually acceptable (e.g. in this assignment). In practice you would have to overdesign a bit to allow for tempeature and other variations. Determining the level of overdesign required to meet all these variations can be quite laborious; we leave this for later.
   c) Compare emitter follower and common-emitter amplifer (optionally with degeneration). When do you use which? Can you think of a situation where you would use both? How?

   Use $I_s = 1\,\text{fA}$, $\beta = 100$, and $V_A = 100\,\text{V}$.



8. a) Calculate the small-signal transresistance $r_x = v_o/i_i$ of the circuit below.
   b) Verify your answer with a circuit simulator (e.g. LTSpice). Turn in a printout of the schematic captured in SPICE (or the netlist) and a plot of r_x versus I_i.

   Use $V_{cc} = 10\,\text{V}$, $V_B = 5\,\text{V}$, $I_I = 100\,\mu\text{A}$, $R_s = 5\,\text{k}\Omega$, $R_L = 1\,\text{k}\Omega$, $I_s = 1\,\text{fA}$, $\beta = 100$, and $V_A = 100\,\text{V}$.
   Nomenclature: $I_i = I_I + i_i$, where I_I is the bias and i_i is the small signal input current.